Lecture 25: CS, CD and CG circuits

Prof J. S. Smith

Context

In today's lecture, we will discuss the various ways that a transistor can be used as a component in active linear circuits, to amplify, act an impedance buffer, and so on.

These simple circuits will then be used as building blocks for building more complex circuits.

Reading

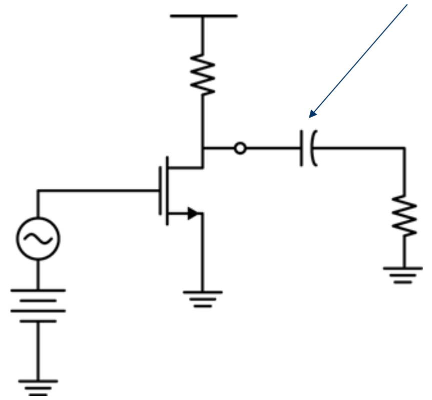
For about a week, we will continue with chapter 8 in the text, single stage amplifiers. We will focus primarily on FET circuits, Common Source(CS) , Common Gate (CG), and Common Drain(CD), sections: 8.1,8.3, 8.4, 8.5, 8.8, 8.9

Following single transistor configurations, we will start discussing multistage and cascaded circuits, which are in chapter 9 of the text.

Lecture Outline

- MOS Common Source Amp
- Current Source Active Load
- Common Gate Amp
- Common Drain Amp

Common-Source Amplifier



EECS 105 Spring 2004, Lecture 25
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Configurations (CS)

- Since the transistor is a three terminal device, we can make a two port device (input and output) but one of the terminals is going to have to be used for both the input and the output ports. The terminology follows…
- Common Source (CS)
  - Provides current and voltage gain
  - Example: an NMOS device with the source grounded, the input being a voltage between the gate and ground, and the output being a voltage between the drain and ground.

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CD

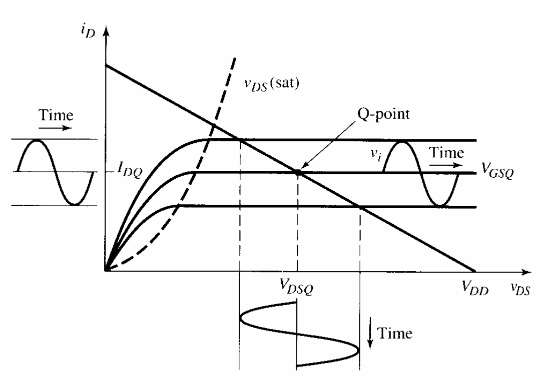
- Common Drain (CD): high impedance input and low impedance output. Low voltage gain
- Example: An NMOS transistor with its Drain at +rail, with an input applied between the gate and (ground/+rail, the same for small signal analysis), and the output taken from the source with reference to ground.
- Example: A PMOS transistor with its Drain at ground, the input applied between the gate and ground, and the output taken from the source with reference to ground

CG

- Common Gate, provides a low impedance input, and a high impedance output. (converts a weak current source to a strong current source)
- The gate is held at small signal ground, while the input is applied at the source, and the output is taken at the drain.
- Low current gain

Common source

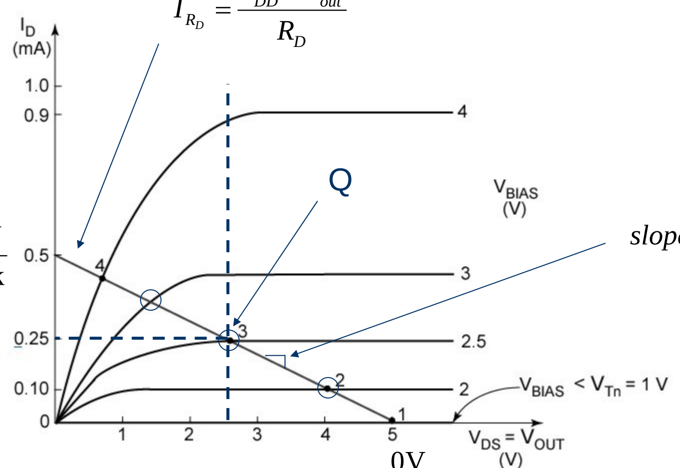
- In the common source amplifier, the input is used to modulate the GS voltage, and the DS voltage is the output, giving a voltage gain depending on the load line:



Load-Line Analysis to find *Q*

$$I_{R_D} = \frac{V_{DD} - V_{out}}{R_D}$$

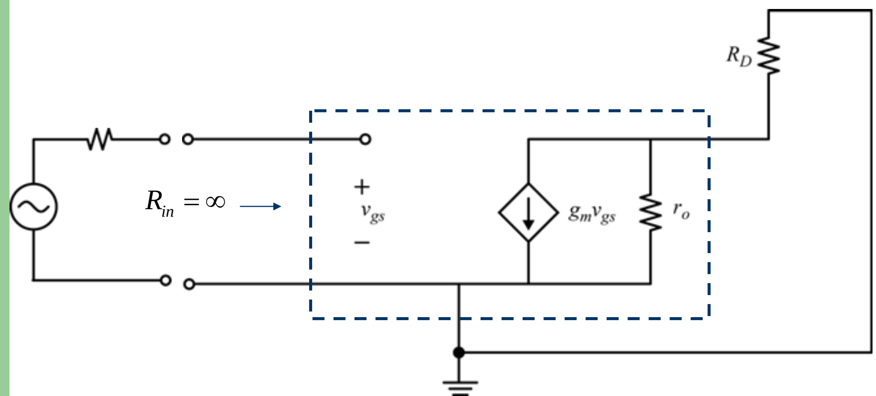
$$I_D = \frac{5\text{V}}{10\text{k}}$$



$$slope = \frac{1}{10\text{k}}$$

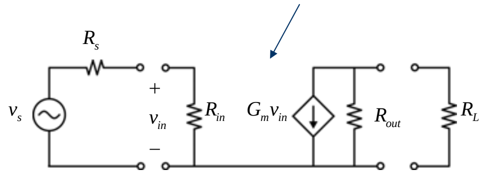
$$I_D = \frac{0\text{V}}{10\text{k}}$$

Small-Signal Analysis

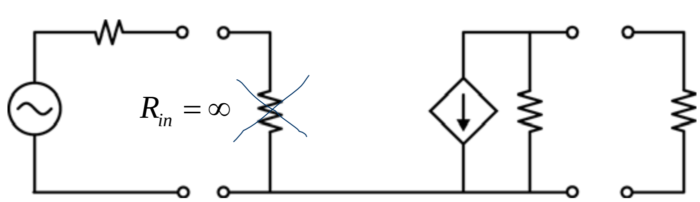


Two-Port Parameters:

Generic Transconductance Amp



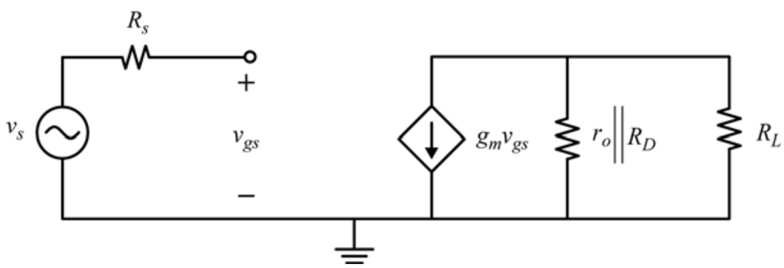
Find R_{in}, R_{out}, G_m



$G_m = g_m \quad R_{out} = r_o \,||\, R_D$

Two-Port CS Model

Reattach source and load one-ports:



Maximize Gain of CS Amp

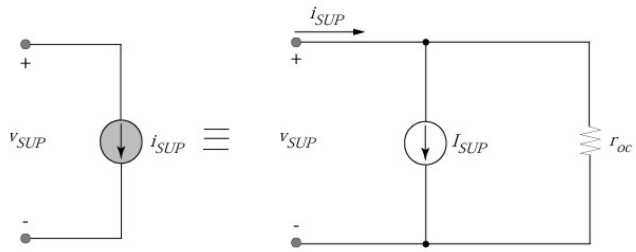
$$A_v = -g_m R_D \| r_o$$

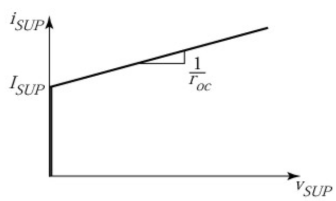
- Increase the g_m (more current)
- Increase R_D (free? Don't need to dissipate extra power)
- Limit: Must keep the device in saturation

$$V_{DS} = V_{DD} - I_D R_D > V_{DS,sat}$$

- For a fixed current, the load resistor can only be chosen so large
- To have good swing we'd also like to avoid getting to close to saturation

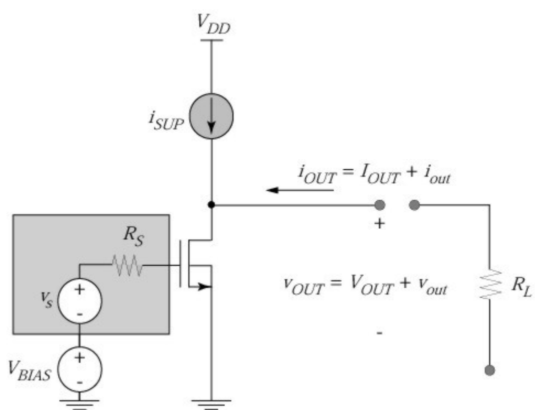
Current Source Supply



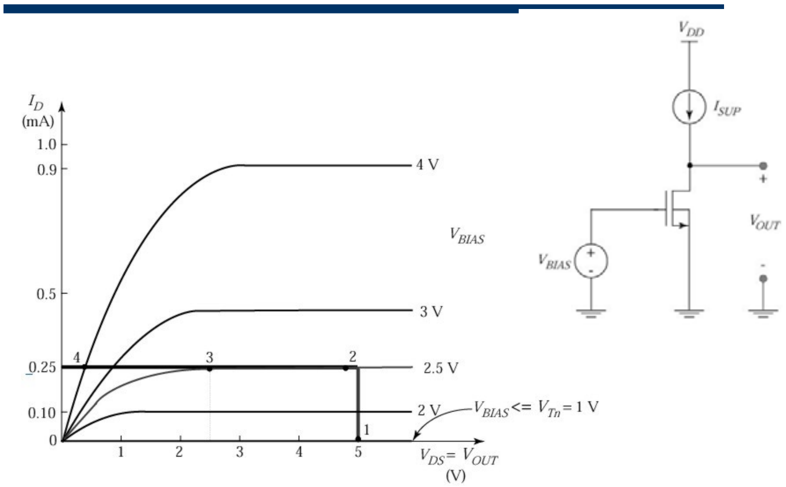


- Solution: Use a current source!
- Current independent of voltage for ideal source

CS Amp with Current Source Supply

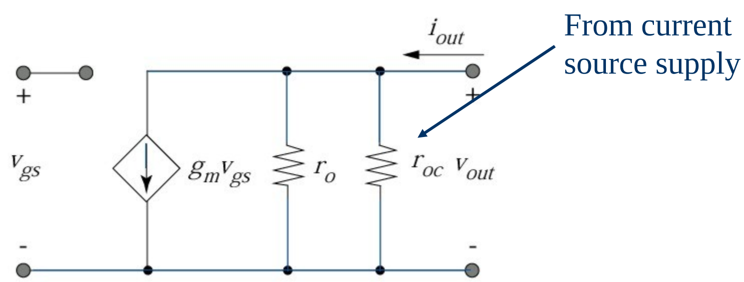


Load Line for DC Biasing



Both the I-source and the transistor are idealized for DC bias analysis

Two-Port Parameters

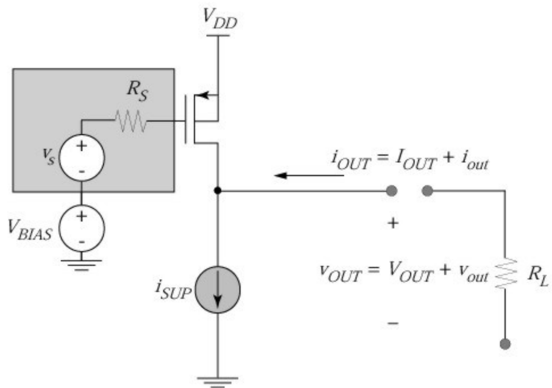


$$R_{in} = \infty$$

$$G_m = g_m$$

$$R_{out} = r_o \,||\, r_{oc}$$

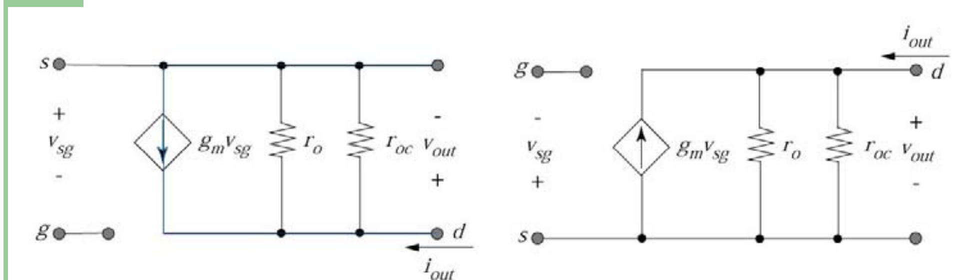
P-Channel CS Amplifier



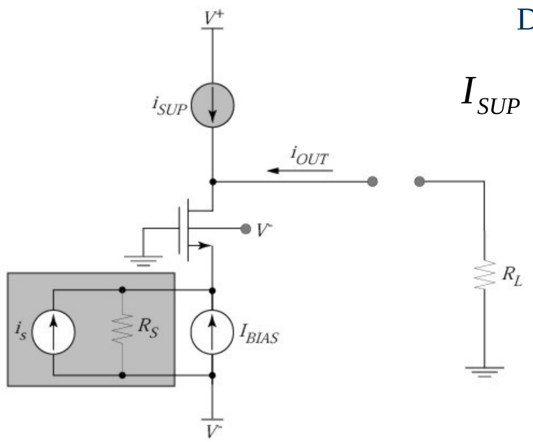
DC bias: $V_{SG} = V_{DD} – V_{BIAS}$ sets drain current $–I_{Dp} = I_{SUP}$

Two-Port Model Parameters

Small-signal model for PMOS and for rest of circuit



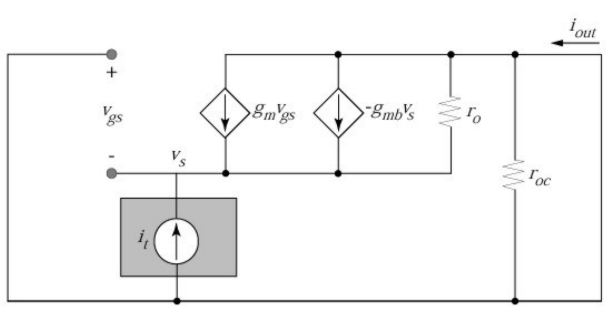
Common Gate Amplifier



DC bias:

$$I_{SUP} = I_{BIAS} = I_{DS}$$

CG as a Current Amplifier: Find A_i

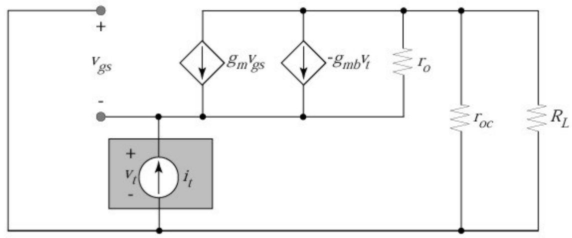


$$i_{out} = i_d = -i_t$$

$$A_i = -1$$

CG Input Resistance

$$v_{gs} = -v_t$$



At input: $$i_t = -g_m v_{gs} + g_{mb} v_t + \left(\frac{v_t - v_{out}}{r_o} \right)$$

Output voltage: $$v_{out} = -i_d (r_{oc} \parallel R_L) = i_t (r_{oc} \parallel R_L)$$

$$i_t = g_m v_t + g_{mb} v_t + \left(\frac{v_t - (r_{oc} \parallel R_L) i_t}{r_o} \right)$$

Approximations…

- We have this messy result

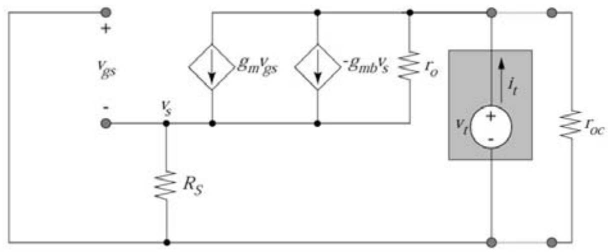
$$\frac{1}{R_{in}} = \frac{i_t}{v_t} = \frac{g_m + g_{mb} + \frac{1}{r_o}}{1 + \frac{r_{oc} \parallel R_L}{r_o}}$$

- But we don't need that much precision. Let's start approximating:

$$g_m + g_{mb} >> \frac{1}{r_o} \qquad r_{oc} \parallel R_L \approx R_L \qquad \frac{R_L}{r_o} \approx 0$$

$$R_{in} = \frac{1}{g_m + g_{mb}}$$

CG Output Resistance



$$\frac{v_s}{R_S} - g_m v_{gs} - (-g_{mb} v_s) + \frac{v_s - v_t}{r_o} = 0$$

$$v_s \left(\frac{1}{R_S} + g_m + g_{mb} + \frac{1}{r_o} \right) = \frac{v_t}{r_o}$$

CG Output Resistance

Substituting $v_s = i_t R_S$

$$i_t R_S \left(\frac{1}{R_S} + g_m + g_{mb} + \frac{1}{r_o} \right) = \frac{v_t}{r_o}$$

The output resistance is $(v_t / i_t) \| r_{oc}$

$$R_{out} = r_{oc} \, || \left(R_S \left(\frac{r_o}{R_S} + g_m r_o + g_{mb} r_o + 1 \right) \right)$$

Approximating the CG R_{out}

$$R_{out} = r_{oc} \,||\, [r_o + g_m r_o R_S + g_{mb} r_o R_S + R_S]$$

The exact result is complicated, so let's try to make it simpler:

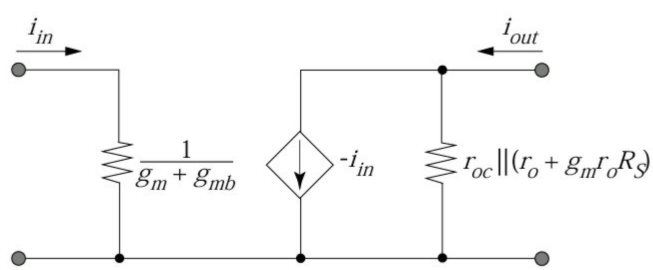
$$g_m \approx 500\mu S \quad g_{mb} \approx 50\mu S \quad r_o \approx 200k\Omega$$

$$R_{out} \cong r_{oc} \,||\, [r_o + g_m r_o R_S + R_S]$$

Assuming the source resistance is less than r_o,

$$R_{out} \approx r_{oc} \,||\, [r_o + g_m r_o R_S] = r_{oc} \,||\, [r_o(1 + g_m R_S)]$$

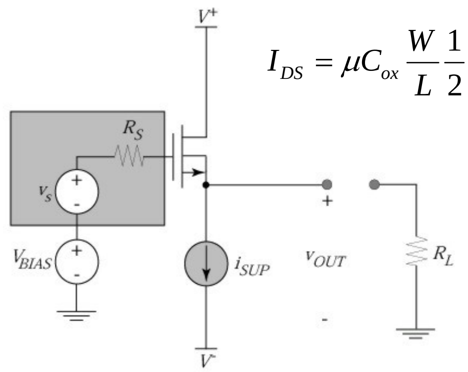
CG Two-Port Model



Function: a current buffer

- Low Input Impedance
- High Output Impedance

Common-Drain Amplifier

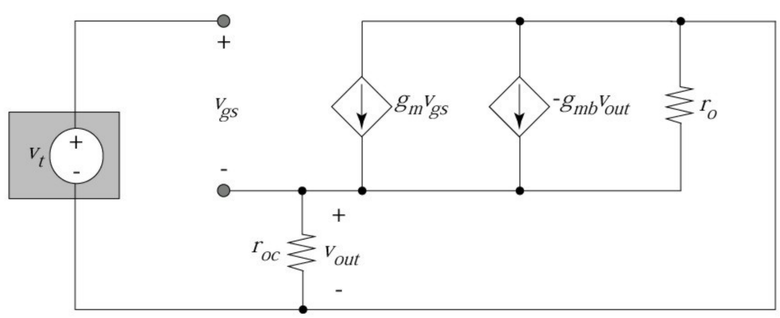


$$I_{DS} = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2$$

$$V_{GS} = V_T + \sqrt{\frac{2 I_{DS}}{\mu C_{ox} \frac{W}{L}}}$$

Weak I_{DS} dependence

CD Voltage Gain



Note $v_{gs} = v_t - v_{out}$

$$\frac{v_{out}}{r_{oc} \| r_o} = g_m v_{gs} - g_{mb} v_{out}$$

$$\frac{v_{out}}{r_{oc} \| r_o} = g_m \left(v_t - v_{out} \right) - g_{mb} v_{out}$$

CD Voltage Gain (Cont.)

KCL at source node: $$\frac{v_{out}}{r_{oc} \| r_o} = g_m(v_t - v_{out}) - g_{mb} v_{out}$$

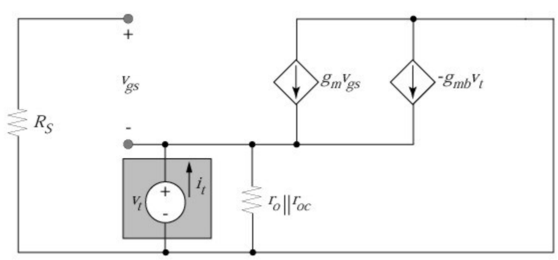
$$\left(\frac{1}{r_{oc} \| r_o} + g_{mb} + g_m\right) v_{out} = g_m v_t$$

Voltage gain (for v_{SB} not zero):

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{\cancel{\frac{1}{r_{oc} \| r_o}} + g_{mb} + g_m}$$

$$\frac{v_{out}}{v_{in}} \approx \frac{g_m}{g_{mb} + g_m} \approx 1$$

CD Output Resistance



Sum currents at output (source) node:

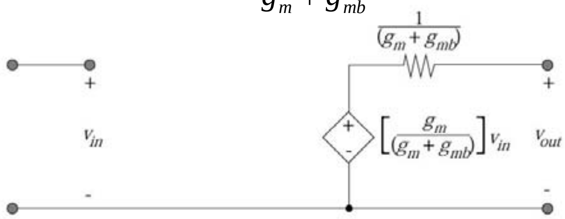
$$R_{out} = r_o \| r_{oc} \| \frac{v_t}{i_t} \qquad i_t = g_m v_t + g_{mb} v_t$$

$$R_{out} \approx \frac{1}{g_m + g_{mb}}$$

CD Output Resistance (Cont.)

$r_o \,||\, r_{oc}$ is much larger than the inverses of the transconductances → ignore

$$R_{out} \approx \frac{1}{g_m + g_{mb}}$$



Function: a voltage buffer

- High Input Impedance
- Low Output Impedance