Enhanced Multilevel Modular Converter with Reduced Number of Cells and Harmonic Content

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***Abstract*—This paper presents an alternative implementation of a modular multilevel converter (MMC) that generates a large number of voltage levels per phase with high resolution voltage steps from a reduced number of cells per arm. The presented MMC employs a half-bridge chain-link of medium-voltage cells and a full-bridge chain-link of low-voltage cells in each of its arms. The total blocking voltage of the full-bridge chain-link is equivalent to half that of the medium-voltage half-bridge cell. The use of half and full-bridge cells with two distinct rated voltages in each arm permits full exploitation of the full-bridge cells to generate high resolution multilevel voltage waveforms with fine stepped transitions between major voltage steps of the medium-voltage half-bridge cells. In this manner, errors in the synthesis of the common-mode voltages of the three phase legs due to switching of the cell capacitors in and out the power path are reduced. The nested multilevel operation of the proposed MMC results in a number of voltage levels which is related to the product, rather than the sum, of the numbers of half and full-bridge cells. Detailed comparisons with existing MMC implementations show that the proposed MMC implementation offers the best design trade-offs (superior AC and DC waveforms with reduced control and power circuit complexity). The validity of the proposed MMC implementation is confirmed using simulations and experimentally.**

***Index Terms*—HVDC, MMC, converter topology, hybrid converter**

I. Introduction

An efficient transmission technology is required for the reinforcement of weak AC networks and continuous increase in the growth of renewable energy production, especially from remote offshore wind farms [1]. Existing multilevel voltage source converter based HVDC transmission systems have received universal acceptance from the power industry [2], [3], because they satisfy the requirements of high efficiency and high power quality on both AC and DC sides, while providing internal fault management which is critical for ensuring continuous operation during cell failure [4], [5].

Two main competing realizations of the modular multilevel converter (MMC) exist. The first approach utilizes a large number of cells per arm, where the blocking capability of each cell is small and is defined by the rating of a single switching device (i.e. 1.6-3kV) [6]. The second approach adopts a reduced number of cells per arm, with each cell rated for high DC operating voltage, ranging between 16-20kV [7]. The latter approach requires the adoption of series-connected semiconductor devices. Reducing the number of MMC cells is attractive since it reduces both the size and complexity of the converter. However, AC and DC power quality are compromised when compared to converters with a high number of cells per arm.

Several derivatives of modular multilevel converters that employ unipolar, asymmetric and symmetric bipolar cells have been presented [8]–[19]. It has been shown that the use of unipolar cells such as half-bridge or three-level flying capacitor cells leads to MMC topologies that cannot retain control when the DC link voltages fall below the respective critical voltage, and which are unable to block DC faults [10], [11]. Asymmetric bipolar cells lead to MMCs that can remain under full control when operating with positive DC link voltages from zero to rated DC voltage, even when the DC voltage falls below the critical value [10]–[18]. They therefore offer DC fault blocking and active control of DC fault currents. The mixed cell modular multilevel converter (MC-MMC) is an example of an MMC that employs asymmetric bipolar cells [10], [11], [13], [20], [21]. Moreover, the use of symmetrical bipolar cells such as the full-bridge or five-level cross connected cells lead to MMCs that can operate with bipolar (positive and negative) DC voltage, including zero voltage, and can reverse the DC or active power by change of DC current or voltage polarities.

Besides the realization of MMCs employing either symmetrical or asymmetrical cells, further performance optimization is possible by mixing different types of the cells, resulting in hybrid multilevel converters. Most of the hybrid converters developed in the last decade were motivated by the trade-offs between DC fault ride-through, efficiency and footprint. Amongst the many hybrid converter topologies proposed in the open literature in recent years, the MC-MMC is the most attractive topology as it retains many of the attributes of the conventional MMC such as modularity and simple methods for bypassing faulted cells, while permitting delivery of customized features such as bespoke control range for a given level of semiconductor losses [20].

In the broader context, MMCs and hybrid converters that employ asymmetrical and symmetrical bipolar cells, or a mixture of different cells, achieve DC fault blocking and greater control flexibility at the expense of higher semiconductor losses compared to converters with unipolar cells. Additionally, other types of hybrid multilevel converters exist (such as the alternate arm converter and the hybrid cascaded two-level converter), that use symmetrical bipolar cells (e.g. full-bridge cells) and incorporate director switches that operate at extremely low-frequency to achieve DC fault blocking capability at reduced footprint and semiconductor losses [22], [23]. However, the aforementioned hybrid converters lack the power quality of an MMC and require filters, thereby making the claim of total converter station footprint reduction debatable.

This paper presents a novel MMC that utilizes both half-bridge (HB) and full-bridge (FB) chain-links in its arms. The HB chain-link is rated for full DC-link voltage and, with each HB cell being rated for medium voltage and therefore requiring series-connected devices, is used to synthesize an approximation to the fundamental sinusoidal output voltage with large (major) voltage steps. The FB chain-link, with total blocking voltage equivalent to half that of an HB cell, is used to generate additional voltage levels with small (minor) voltage steps to smooth the transitions between the large voltage steps generated by the HB cells so that the MMC provides high-quality sinusoidal output. In this way, the proposed MMC has the potential to eliminate both AC and DC side filters despite having a reduced number of cells. The proposed MMC also exhibits a new, unique multiplication feature where the number of voltage levels per arm is approximately equal to the product of the numbers of HB and FB cells, whilst the output voltage step amplitude is equal to that of the FB cell voltage. These characteristics contribute to significant improvement in the quality of the AC and DC side waveforms generated by the proposed MMC.

The paper is organized as follows: Section II explains the main motivation for the proposed MMC. Section III describes the theoretical principles that underpin the operation and modulation of the proposed MMC. Section IV presents illustrative simulation and experimental results to corroborate the theoretical discussions presented in Section III. Section V discusses the scalability of the proposed MMC, and Section VI presents the conclusions, where the main findings of this research are summarized.

II. Motivation

The MMC synthesizes AC voltage by inserting and by-passing cells in the upper and lower arms such that the blocking voltage of the inserted cells in both arms is slightly larger or smaller than the imposed DC link voltage [24]. In MMC with large numbers of cells per arm, where each cell is rated for a small voltage ranging from 1.6-2.5kV, the nearest voltage level modulation (NLM) scheme synthesizes high quality AC and DC side waveforms. In contrast, in MMC with relatively small numbers of cells per arm, where the rated voltage per cell ranges from 15-20kV, pulse width modulation (PWM) is widely used to facilitate accurate synthesis of the output AC and DC voltages. The use of series-connected switching devices in the high-voltage cells of an MMC with a reduced number of cells, e.g. 40 for a 640kV HVDC converter, introduces significant errors to the output AC and common-mode voltages of the three MMC legs, and high-frequency components in the arm currents as shown in Fig. 1(a) and (b). To satisfy the harmonic requirements specified by the Grid Code, an AC filter is required to reject the high-frequency PWM harmonics [25]. A DC filter is required to remove the voltage mismatch that may cause ripple resulting from transitions between the different voltages, as depicted in Fig. 1. Under fast-acting current interruption, i.e. DC circuit breakers with operating times in the range 2-5ms, over-sizing of the arm inductors is unnecessary [26]. Increased voltage error due to

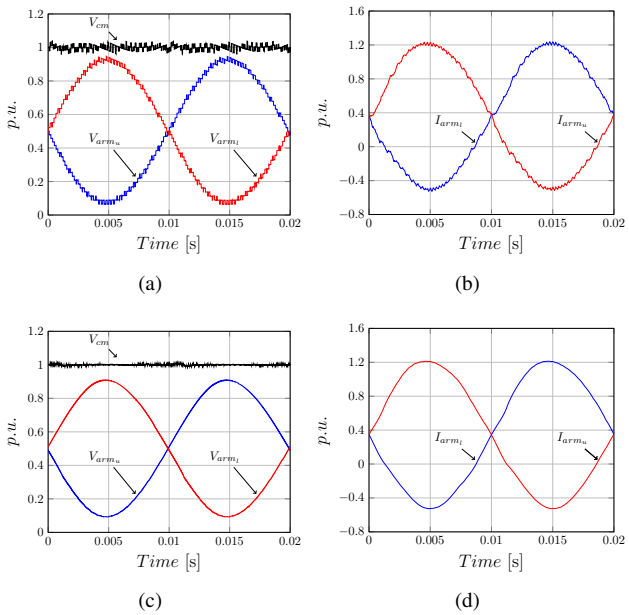


Fig. 1. MMC (P: 1000MW, V_{DC}: 640kV, L_{arm}: 0.05p.u.) common-mode voltage, arm voltages and currents (a)-(b) 40 cells, (c)-(d) 400 cells.

the use of large switching voltages increases the magnitudes of the high-frequency currents and voltages to be injected into the DC side. Relatively large arm inductors are therefore required to suppress the high-frequency components of the circulating currents. Thus, an increased number of levels with smaller switching voltages improves the power quality of the AC and DC side waveforms, as well as the arm waveforms, and eliminates or minimizes passive filtering requirements.

It should be stressed that DC fault blocking is not one of the motivations of the proposed topology, especially as the maximum negative voltage its FB chain-link produces is negligible and insufficient to facilitate DC fault blocking. Instead the proposed topology is an enhancement that applies to half or full-bridge MMCs that employ medium-voltage cells, predominantly to improve the quality of the AC and DC side waveforms. However, only improvement of the half-bridge MMC is pursued in this paper due to space limitations.

III. Proposed Topology

In this section, the proposed topology is described in the context of cell placement design, fundamental operation, modulation strategies and power losses.

A. Converter design

Fig. 2 shows one phase leg of the proposed Enhanced MMC (EMMC) topology. Each arm of the EMMC consists of two types of chain-link: the half-bridge (HB) chain-link and the full-bridge (FB) chain-link. The total blocking voltage of the FB chain-link is equivalent to half the rated voltage of an HB cell. If suffixes hb and fb signify the variables and parameters relating to the HB and FB chain-links respectively, the HB and FB cell voltages are described as:

$$V_{cell-hb} = \frac{V_{DC}}{N_{hb}} \tag{1}$$

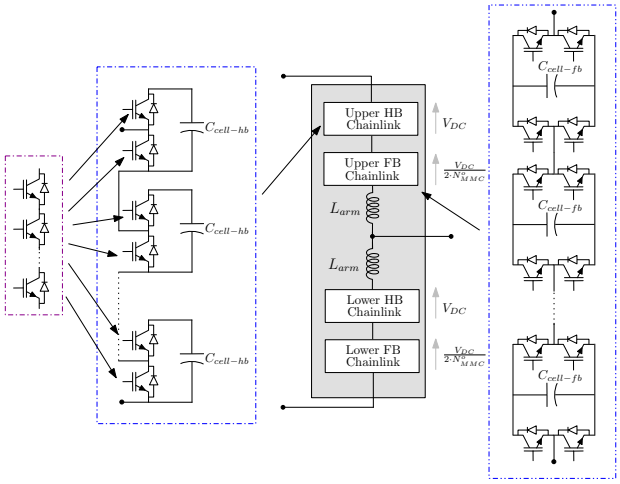


Fig. 2. Phase representation of EMMC topology.

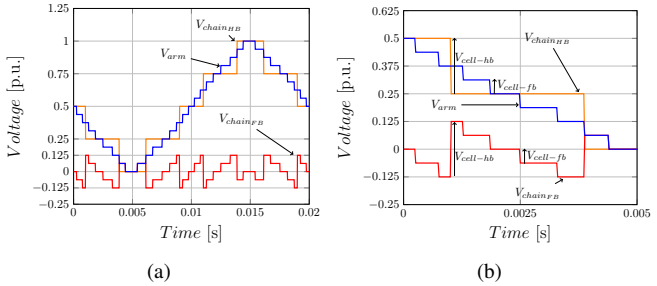


Fig. 3. EMMC internal synthesized voltages: (a) Generated voltage waveforms, (b) Detailed view of voltage waveforms

where $V_{cell-hb}$ is the voltage across an HB cell, N_{hb} is the number of cells in the HB chain-link, and V_{DC} is the pole-to-pole DC voltage.

$$V_{cell-fb} = \frac{V_{cell-hb}}{2N_{fb}} \tag{2}$$

where $V_{cell-fb}$ is the voltage across an FB cell and N_{fb} is the number of cells in the FB chain-link of each arm. Each arm will have a total number of cells N, defined in (3).

$$N = N_{hb} + N_{fb} \tag{3}$$

The conventional MMC with N_{hb} cells per arm generates $N_{hb}+1$ voltage levels per arm, while the EMMC generates $2N_{hb} \cdot N_{fb} + 1$ voltage levels per arm. This multiplication effect enables the EMMC to generate an increased number of voltage levels when compared to the conventional MMC with an equivalent number of cells, as shown in (4) and (5).

$$N^o_{MMC} = N + 1 \tag{4}$$

where N^o_{MMC} represents the number voltage levels per arm of the conventional MMC.

$$N^o_{EMMC} = 2N_{hb} \cdot N_{fb} + 1 \tag{5}$$

Fig. 3 depicts the ideal synthesis of the total arm voltage and voltages of the HB and FB chain-links, assuming an illustrative EMMC with 4 HB cells and 2 FB cells per arm, with all voltages being normalized to DC voltage V_{DC}. Fig. 3(a) shows that the HB chain-link of each EMMC arm synthesizes a stepped approximation of the sinusoidal fundamental voltage $V_{chain_{hb}}$ with a major voltage step equal to 0.25p.u. ($V_{cell-hb} = \frac{1}{4}V_{DC} = \frac{V_{DC}}{N_{hb}}$), whilst the FB chain-link of each arm synthesizes a bipolar voltage $V_{chain_{fb}}$ with positive and negative peaks of $\pm 0.125 p.u.$ ($\pm\frac{1}{2} \cdot \frac{1}{4}V_{DC} = \pm\frac{1}{8}V_{DC} = \pm\frac{V_{DC}}{2N_{hb}} = \frac{1}{2}V_{cell-hb}$) and minor a voltage step of $\frac{0.125}{2} p.u.$ ($\frac{1}{2} \cdot \frac{1}{8}V_{DC} = \frac{1}{16}V_{DC} = \pm\frac{V_{DC}}{2N_{fb}} \cdot N_{hb} = \frac{V_{cell-hb}}{2N_{fb}}$). Observe that the total arm voltage V_{arm} is the algebraic sum of the voltages $V_{chain_{hb}}$ and $V_{chain_{fb}}$, synthesized by the HB and FB chain-links respectively. The minor voltage step seen in V_{arm} is derived directly from the voltage produced by a single FB cell ($\frac{V_{DC}}{2N_{hb}N_{fb}} = \frac{V_{cell-hb}}{2N_{fb}}$). The positive and negative peaks of $V_{chain_{fb}}$ in each arm are limited to $\pm\frac{1}{2}V_{cell-hb}$, which suggests that the minimum blocking voltage of the FB chain-link is $\frac{1}{2}V_{cell-hb}$. Based on Fig. 3, the illustrative EMMC consisting of 4 HB and 2 FB cells can generate 17 discrete voltage levels in each arm. The number of arm voltage levels generated can be expressed generically as in (5).

The HB cell capacitance may be expressed in terms of the arm equivalent capacitance $C_{arm-tot}$ as:

$$C_{cell-hb} = C_{arm-tot} \cdot N_{hb} \tag{6}$$

where $C_{cell-hb}$ is the cell capacitance for the HB chain-link.

Similarly the cell capacitance $C_{cell-fb}$ for the FB cell is expressed in terms of HB cell capacitance $C_{cell-hb}$ and the number of FB cells N_{fb} as:

$$C_{cell-fb} = C_{cell-hb} \cdot \frac{N_{fb}}{2} \tag{7}$$

The total capacitance of the FB chain-link is equal to half the total HB cell capacitance. This is achieved by increasing the FB cell capacitance as described in (7). In industry, cell capacitor sizing is based on stored energy criteria and considers volume and capacitor voltage ripple. Values in the range 30-40kJ/MW are commonly considered [7], and (6) and (7) guarantee that the cell capacitor voltage ripple will not exceed $\pm 10\%$ which is a commonly used design value in conventional MMC.

It should be noted that the FB cells of the EMMC are not intended to facilitate DC fault blocking or reduced DC link operation. The proposed concept of incorporating FB chain-links with minor voltage steps could be extended to other MMC variants, such as the mixed-cell and FB-MMC.

B. Operating principle

The EMMC uses the HB chain-link rated at full pole-to-pole DC voltage to synthesize the fundamental voltage with major voltage steps, $\frac{V_{DC}}{N_{hb}}$, as shown in Fig. 4(a). The FB chain-link, with combined blocking voltage equivalent to half that of an HB cell, acts as an active power filter (APF) and generates a multilevel waveform with minor voltage steps, $\frac{V_{DC}}{2N_{hb} \cdot N_{fb}}$. Thus, the FB chain-link facilitates smooth transition between the major voltage levels through intermediate voltage levels separated by minor voltage steps. Since the HB chain-link synthesizes the fundamental component of the arm voltage,

the continuous modulating signal m_{hb} is used to estimate the number of HB cells to be inserted and bypassed in each arm on a discrete basis, as shown in Fig. 4(a). Equally, the FB chain-link is required to inject voltage harmonics into each arm, thus the modulating signal of the FB chain-link is extracted as an error between the target fundamental voltage and its switched equivalent, as shown in Fig. 4(b). Thus, the modulating signals for the HB and FB chain-links are:

$$m_{hb} = M \cdot cos(\omega t + \delta) \tag{8}$$

$$m_{hb_{NLM}} = round(m_{hb} \cdot N_{hb}) \tag{9}$$

$$m_{fb} = m_{hb} \cdot N_{hb} - m_{hb} \tag{10}$$

$$m_{fb_{NLM}} = round(m_{fb} \cdot N_{fb}) \tag{11}$$

where M represents modulation index amplitude.

Equations (8)-(11) show that the FB and HB cell modulation indexes are created from the same reference. Fig. 4 shows that the HB chain link of each arm generates a staircase voltage with $N_{hb}+1$ levels, with a pre-defined major voltage step, defined in (1), between two consecutive voltage levels. In contrast, the FB chain link of each arm generates a bipolar voltage consisting of $2N_{fb}+1$ levels, with a step voltage of $V_{cell-fb}$ defined in (2). The FB cells are switched to produce positive and negative output voltage steps around an artificial zero voltage level that is synchronized with the edges of $m_{hb_{NLM}}$. Fig. 4(c) shows the ideal modulating signals of the HB and FB chain-links normalized for the synthesis of the minor voltage levels between two successive major voltage levels.

Conventional capacitor voltage balancing techniques, such as the sorting, tolerance band and cell reference modulation methods [27], [28], can be applied to both chain-links of the EMMC.

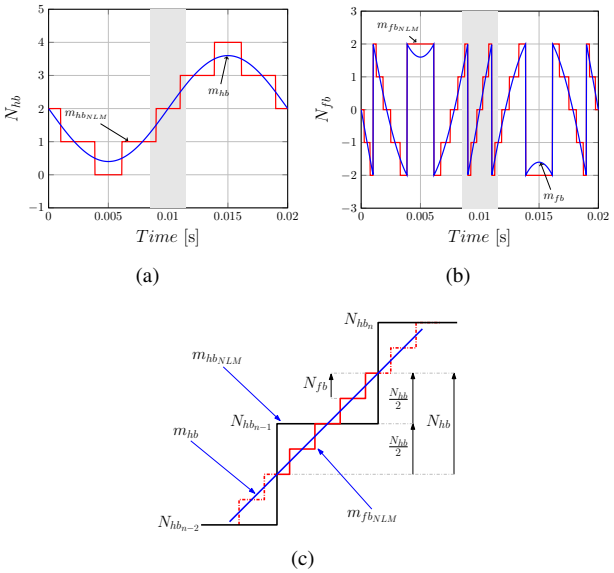


Fig. 4. Modulation signals: (a) HB chain-link, (b) FB chain-link, (c) Detailed illustration of modulation signals.

C. Converter analysis

In the following analysis of the proposed EMMC, subscript j defines the phase index (i.e. $j = a, b, c$) and k defines the upper and lower position of the arm (i.e. $k = u$ for the upper arm and $k = l$ for the lower arm). The FB and HB cell capacitor currents can be described in terms of arm currents and their switching functions (S_{cell}) as:

$$m_{hb} \cong \sum_{i=1}^{N_{hb}} \left[S_{cell-hb_{N_{hb},j,k}} \right] \tag{12}$$

$$m_{fb} \cong \sum_{i=1}^{N_{fb}} \left[S_{cell-fb_{N_{fb},j,k}} \right] \tag{13}$$

$$i_{cell-hb_{N_{hb},j,k}} = S_{cell-hb_{N_{hb},j,k}} \cdot i_{j,k} \tag{14}$$

$$i_{cell-fb_{N_{fb},j,k}} = S_{cell-fb_{N_{fb},j,k}} \cdot i_{j,k} \tag{15}$$

Each arm voltage $v_{arm_{j,k}}$ is formed by the summation of individual cell voltages $v_{cell-hb_{N_{hb},j,k}}(t)$ and $v_{cell-fb_{N_{hb},j,k}}(t)$ as described in (16) to (19):

$$v_{cell-hb_{N_{hb},j,k}}(t) = \frac{1}{C_{cell-hb}} \cdot \int \left(i_{cell-hb_{N_{hb},j,k}}(t) \right) dt \tag{16}$$

$$v_{cell-fb_{N_{fb},j,k}}(t) = \frac{1}{C_{cell-fb}} \cdot \int \left(i_{cell-fb_{N_{fb},j,k}}(t) \right) dt \tag{17}$$

$$\begin{aligned} v_{arm_{j,k}} = & \sum_{y=1}^{N_{hb}} \left[s_{cell-hb_{N_{hb},j,k}} \cdot v_{cell-hb_{N_{hb},j,k}} \right] \\ & + \sum_{y=1}^{N_{fb}} \left[s_{cell-fb_{N_{fb},j,k}} \cdot v_{cell-fb_{N_{fb},j,k}} \right] \end{aligned} \tag{18}$$

or

$$v_{arm_{j,k}} = V_{chain_{HB_{j,k}}} + V_{chain_{FB_{j,k}}} \tag{19}$$

The instantaneous common-mode voltage the MMC phase legs present at its DC terminals can be expressed in terms of the instantaneous upper and lower arm voltages ($v_{arm_{j,u}}$, $v_{arm_{j,l}}$) as:

$$V_{cm} = v_{arm_{j,u}} + v_{arm_{j,l}} = V_{DC} \pm dV \tag{20}$$

where dV represents the DC voltage drops across the internal resistance of the arm reactors and switching devices of the upper and lower arms. Synthesis of the AC voltage, as well as the AC, common-mode and circulating currents, is similar to that in the conventional MMC [24]. Fundamentally, the necessary condition for cell capacitor voltage balancing is that the energy exchange between the cell capacitors of the HB and FB chain-links, and both chain-links with the AC side, must be zero as described in (21) and (22).

$$E_{HB_{j,k}} = \int_0^T \left(m_{hb} \cdot i_{arm_{j,k}}(t) \right) dt = 0 \tag{21}$$

$$E_{FB_{j,k}} = \int_0^T \left(m_{fb} \cdot i_{arm_{j,k}}(t) \right) dt = 0 \tag{22}$$

It should be noted that incorporation of the very limited number of FB cells into each arm of the proposed EMMC may affect the magnitudes of the low-order characteristic harmonics and the high-frequency harmonics of the circulating currents. The DC offset of the modulating signal m_{fb} of the FB chain-link is manipulated in order to ensure that the FB chain-link exchanges zero net energy or active power with the FB chain-link and AC side. Modulation index m_{fb} is adjusted according to the FB cell energy as described in (23).

$$W_{fb_{j,k}} = \frac{1}{N_{fb}} \sum_{i=1}^{N_{fb}} \frac{C_{cell-fb} \cdot v^2_{cell-fb_{N_{fb},j,k}}}{2} \tag{23}$$

Fig. 5 shows the overall controller structure of the proposed EMMC. The horizontal and vertical energy balance controllers, and the outer and inner current controllers, define the modulation index for the HB chain-link. The vertical (arm balancing) controller is responsible for ensuring that the DC voltages across the upper and lower arms of all three phases are equal (zero differential voltage or energy). The horizontal (average capacitor voltage or energy) controller is responsible for ensuring that the three phase legs have the same DC voltage to prevent DC circulating currents between the phase legs. The FB chain-link energy controller ensures that the energy stored in the upper and lower arm FB chain-links is balanced. This is achieved by injecting a small DC component into the modulation index of the FB chain-links. Also, the circulating current suppression controller modifies the FB chain-link modulation index in order to reduce the switching instances of the HB cells, and hence switching losses.

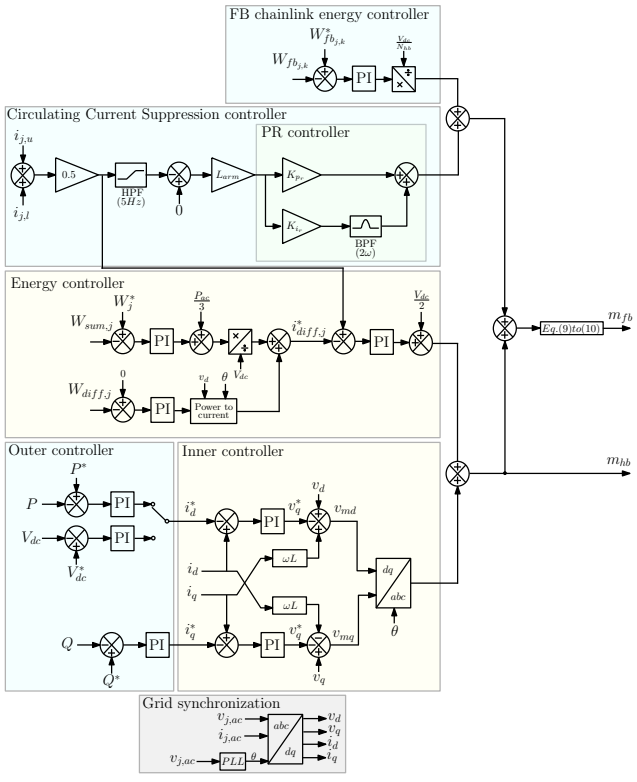


Fig. 5. EMMC control structure

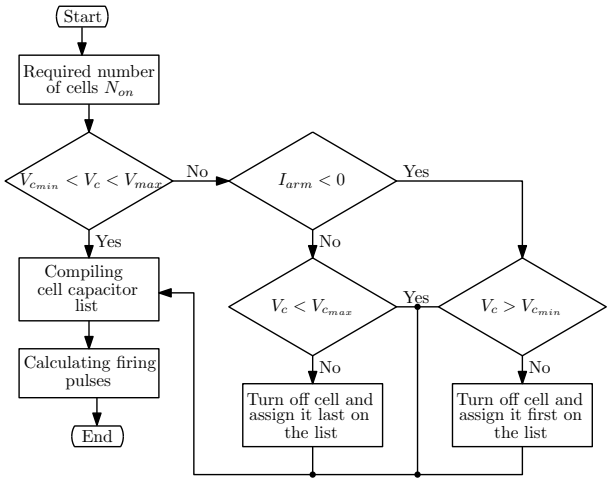


Fig. 6. Flowchart of the tolerance band cell voltage balancing algorithm

If HB cells are used in place of FB cells, the NLM algorithm must be modified accordingly, i.e. replacement of the $round$ function in (9) and (11). Additionally, twice as many HB cells will be required, leading to increased cell capacitance without any additional benefit. Also instead of the previously described DC offset manipulation, distributed capacitor voltage balancing [29] in the FB cells could be used to prevent departure of the cell voltage from its nominal value.

The cell capacitor voltages of the HB and FB chain-link in each arm of the EMMC are balanced using two independent tolerance band capacitor voltage balancing methods [27], illustrated in Fig. 6.

D. Modulation schemes

Table I lists a number of hybrid modulation techniques which are applicable for controlling the EMMC HB and FB chain-links. The first scheme is well-suited to the low number of HB and FB cells. Application of PWM to the HB chain-link with major voltage steps permits accurate synthesis of the fundamental voltage over the full modulation index linear range. FB cell balancing is therefore readily achievable over the full modulation range as the FB chain-links will not be forced to produce fundamental voltage (or exchange non-zero active power). This scheme is not however preferred due to the increased complexity of the implementation, difficulty in synchronizing two high-frequency modulations, and switching loss concerns. By incorporating selective harmonic elimination (SHE), the second scheme in Table I offers similar attributes to the first scheme for low numbers of HB and FB cells, including operation over the full modulation index range. Its extension to MMC with large numbers of HB cells is, however, problematic with regard to calculation of switching angles and implementation, particularly at high modulation indexes where several angles will be indistinguishable. The third scheme in Table I inherently has all the features of the second scheme when it is applied to MMC with large numbers of HB cells. When it is applied to MMC with reduced numbers of HB cells, its inability to accurately synthesize the required fundamental

voltage during operation at low modulation indexes increases the risk of voltage imbalance in the FB cells, as the FB chain-link will be required to contribute fundamental voltage. The fourth scheme is well suited to MMC with large numbers of HB and FB cells. Thus, it is able to operate over the full modulation index and power factor range.

TABLE I
MODULATION SCHEMES

Scheme	HB Chain-link	FB Chain-link
1	PWM	PWM
2	SHE	PWM
3	NLM	PWM
4	NLM	NLM

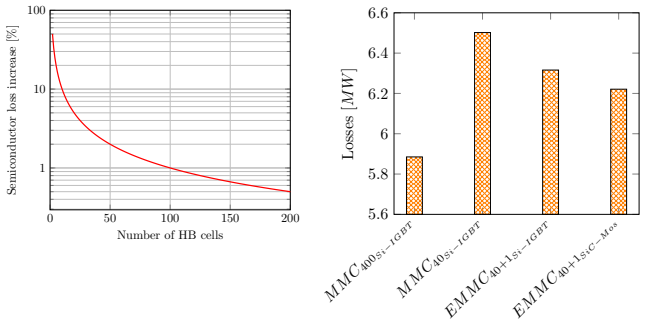
E. Converter power losses

The increased semiconductor losses in the EMMC when compared to the conventional MMC are highly dependent on the proportional relationship between the HB cell voltage and the DC link voltage. When NLM is applied to an HB chain-link which is subjected to high voltage and switching frequency ranging from 150-300Hz, the switching loss is expected to be slightly lower than that which could be achieved with PWM. However, due to FB cell operation, the additional conduction losses are equivalent to those of one HB cell and, as a result, the FB losses will be a small proportion of the total arm losses, as show in (24). The total switching losses may be reduced as the HB cells switch less frequently, while FB cells switch at lower voltage. Additionally, as the voltage requirement of FB cells is low more efficient semiconductors, such as SiC MOSFETs which have lower conduction and switching losses when compared to similarly rated IGBTs, may be employed.

$$P_{EMMC_{cond}} = \frac{N_{hb}+1}{N_{hb}} \cdot P_{MMC_{cond}} \tag{24}$$

Fig. 7(a) shows the correlation between the number of HB cells and the increase in total semiconductor losses, but does not consider the potential reduction in switching and passive filter losses. As the number of HB cells increases the incremental semiconductor losses decrease.

Fig. 7(b) and Table II present a semiconductor loss comparison between the conventional MMC implementations (40-cell MMC and 400-cell MMC) and the EMMC. Table II and Fig. 7(b) display semiconductor losses for the 400-cell HB-MMC that uses silicon IGBTs ($MMC_{400_{Si-IGBT}}$), the 40-cell HB-MMC that uses silicon IGBTs ($MMC_{40_{Si-IGBT}}$), the EMMC with 40 HB cells and 5 FB cells, where both HB and FB cells employ silicon IGBTs ($EMMC_{40+1_{Si-IGBT}}$), and the EMMC with 40 HB cells and 5 FB cells, where the HB cells use Silicon IGBTs and the FB cells employ silicon carbide (SiC) MOSFETs ($EMMC_{40+1_{SiC-Mos}}$). The semiconductor losses displayed are computed from a detailed power loss model [25] which accounts for junction temperature, IGBT and diode threshold voltages, on-state resistance, turn-on and turn-off energy, and diode recovery energy.



(a) (b)

Fig. 7. Semiconductor loss estimation: (a) Semiconductor loss increase versus the number of HB cells, (b) Semiconductor loss comparison between conventional MMC and EMMC with Si-IGBTs and SiC-MOSFETs.

Fig. 7(b) and Table II show that the EMMC has marginally higher conduction loss compared to the conventional MMC with 40 and 400 cells per arm, when all MMCs being compared employ the same silicon IGBTs. Amongst the silicon IGBT MMCs, the 400-cell MMC exhibits the lowest switching loss, followed by the proposed EMMC, while the conventional 40-cell MMC exhibits the highest switching loss. As a result, the overall semiconductor loss of the EMMC is slightly lower than that of the conventional 40-cell MMC, with the conventional 400-cell MMC exhibiting the lowest overall semiconductor loss. Additionally, the results in Fig. 7(b) and Table II show further reduction in semiconductor loss of the EMMC is possible by adopting wide-band-gap switching devices such as silicon carbide MOSFETs.

Based on the basic design presented, the EMMC increases semiconductor count by 2.5%, which can be offset by other design considerations such as cell redundancy.

TABLE II
SEMICONDUCTOR LOSS COMPARISON BETWEEN MMC AND EMMC

Losses	Conduction [MW]	Switching [MW]	Total [MW]
$MMC_{400_{Si-IGBT}}$	4.75	1.14	5.89
$MMC_{40_{Si-IGBT}}$	4.75	1.75	6.50
$EMMC_{40+1_{Si-IGBT}}$	4.87	1.14	6.32
$EMMC_{40+1_{SiC-Mos}}$	4.87	1.35	6.22

IV. TOPOLOGY VALIDATION

This section presents simulation and experimental validation of the EMMC. Table III shows the simulation and experimental test rig parameters used to substantiate the viability of the EMMC. In both simulation and experimental studies, the HB chain-link is controlled using NLM, whilst the FB chain-link is controlled using high-frequency PWM with 2.5kHz level-shifted carriers (one carrier per FB cell). Both chains adopt sorting based capacitor voltage balance. The sizing of the HB cell capacitance is derived from a scaled system with inertia

of 40kJ/MVA (equivalent to 40ms). On a similar basis, the arm inductance is calculated to be 0.2p.u.

TABLE III
CONVERTER SPECIFICATION

V_{DC} [V]	300
R_{LOAD} [Ω]	17
N_{hb} / N_{fb}	4/4
f_S [kHz]	2.5
L_{arm} [mH]	5
C_{hb} / C_{fb} / C_f [mF]	2.2 / 4.4 / 5

A. Simulation study

Simulation results where one phase of the EMMC operates under open-loop control with a modulation index of 0.85 and a resistive load of 17Ω are shown in Fig. 8. Fig. 8(a) shows the low-frequency modulation of the HB chain-link voltage waveform using NLM, while Fig. 8(b) shows the high-frequency modulation of the FB chain-link using PWM as described earlier. Observe that the synthesized switched voltage, which is a step approximation of a sinusoidal waveform by the FB chain-link, occupies the full DC-link voltage range of V_{DC}, whilst the FB chain-link occupies a voltage range equivalent to half that of an HB cell, and is a small fraction of V_{DC} according to (2). Fig. 8(a)-(d) indicate that the voltages across the cell capacitors of the HB and FB chain-links, and consequently the voltages across the switching devices of both chain links, are tightly regulated around the desired steady-state values. Fig. 8(e) shows the total upper and lower arm voltages, which are synthesized by HB chain-links comprising four HB cells each and providing large step voltage transitions, and FB chain-links which consist of four FB cells providing small step voltage transitions. Observe that the upper and lower arm voltages in Fig. 8(e) exhibit a substantial increase in the number of voltage levels, amounting to $2N_{hb}{\cdot}N_{fb}$+1 as described earlier. Although this illustrative simulation uses only four HB cells and four FB cells, the arm voltage of the EMMC accurately reflects the modulating signal of a conventional MMC with 32 cells per arm. Fig. 8(f) shows that the common-mode voltage (or instantaneous sum of the upper and lower arm voltages) that the EMMC presents at its DC terminals exhibits some high-frequency content due to switching edge mismatch. Fig. 8(g) and (h) show that the EMMC produces high-quality sinusoidal output phase voltage and current waveforms even though it is feeding a purely resistive load.

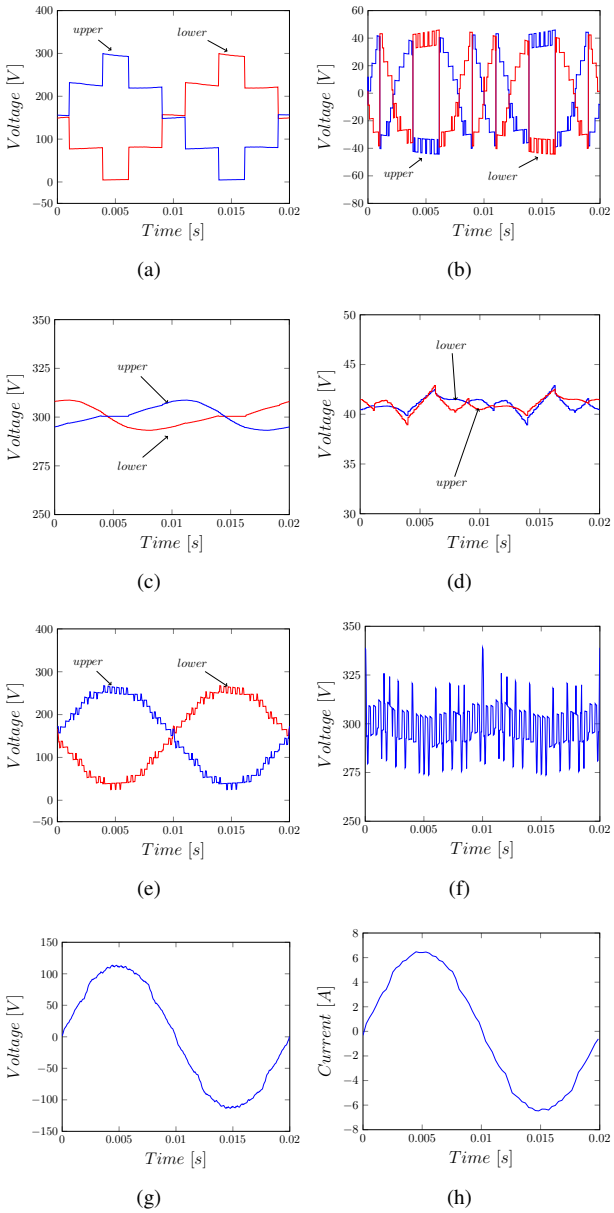


Fig. 8. EMMC simulation results: (a) HB chain-link voltage, (b) FB chain-link voltage, (c) HB chain-link total capacitor voltage, (d) FB chain-link total capacitor voltage, (e) total arm voltage, (f) common-mode voltage, (g) output AC voltage, (h) output AC current.

B. Experimental study

This section presents experimental results for a prototype single phase of a EMMC, which is based on an existing four cell per arm conventional MMC test rig that was upgraded to the EMMC topology by the addition of FB chain links and the necessary control system, as shown in Fig. 9. A 50Hz sinusoidal reference (modulating) signal is generated externally and fed to Cypress Semiconductor 32-bit Arm® Cortex®-M3 PSoC® 5LP low-power micro-controller units MCU 1 and MCU 2. MCU 1 manages NLM and capacitor balancing of the upper and lower HB chain-links, whilst MCU 2 is dedicated to high-frequency level shifted PWM (f_s=2.5kHz) and capacitor voltage balancing of the upper and lower FB chain-links. This approach ensures that the fundamental voltage components generated by the upper and lower chain-links are synchronized and completely complementary so as to avoid any potential voltage mismatches between the arms which could be reflected in the AC and DC voltages. Moreover, the synchronization of each arm HB and FB chain-link is achieved from the reference, and does not need internal communication or clock-synchronization.

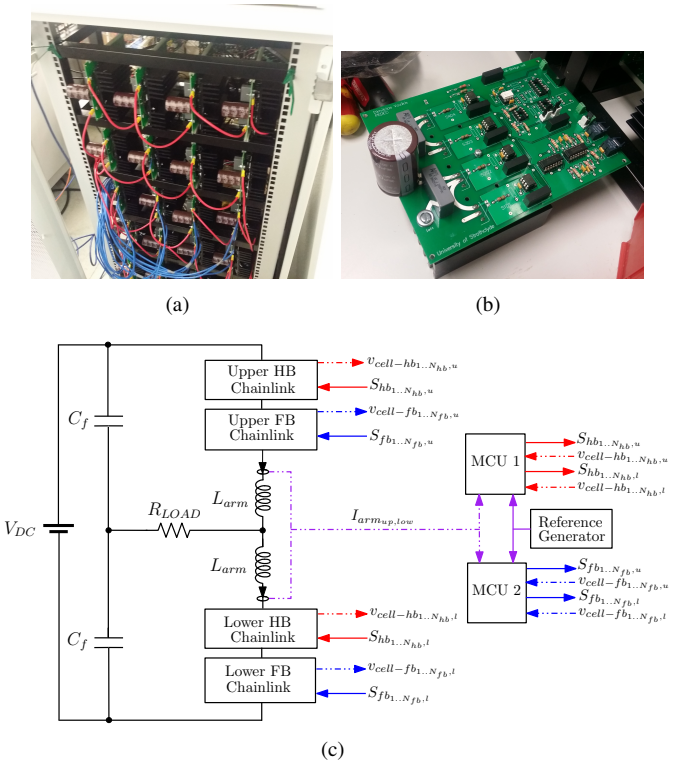


Fig. 9. Experimental configuration: (a) HB and FB chain-links, (b) converter cell, (c) schematic diagram.

As in the simulation, each HB and FB chain-link consists of four cells, and the capacitances of the HB and FB cells are 2.2mF and 4.4mF respectively. Two capacitors (C_f=5mF) with split mid-point are connected across the DC power supply, as shown in Fig. 9(c), to create a return path for the single-phase arrangement. A 17Ω resistive load is connected to the converter AC side. The experimental tests replicate the simulation study to enable direct comparison of the results. Fig. 10 shows that the experimental waveforms for the voltages across the HB and FB chain-links of the upper and lower arms, the HB and FB cell capacitor voltages, the upper and lower total arm voltages, the common-mode voltage, and the output phase voltage and current correspond well with the simulation waveforms illustrated in Fig. 8. The low-energy high-frequency voltage and current spikes in Fig. 10 (a), (b), (e), (f) and (g) are due to small switching mismatches introduced by factors such as dead-time, differences in the turn-on and turn-off times, rapid reference tracking and electromagnetic interference. The adverse impact of these factors is amplified in the experimental waveforms in Fig. 10 due to the relative size of the minor voltage steps of the FB cells compared to that of the major voltage steps of the HB cells. In a full-scale system where the ratio of the minor to major voltage steps will be of the order of 0.1 or less, these current spikes are expected to be attenuated by the arm inductors.

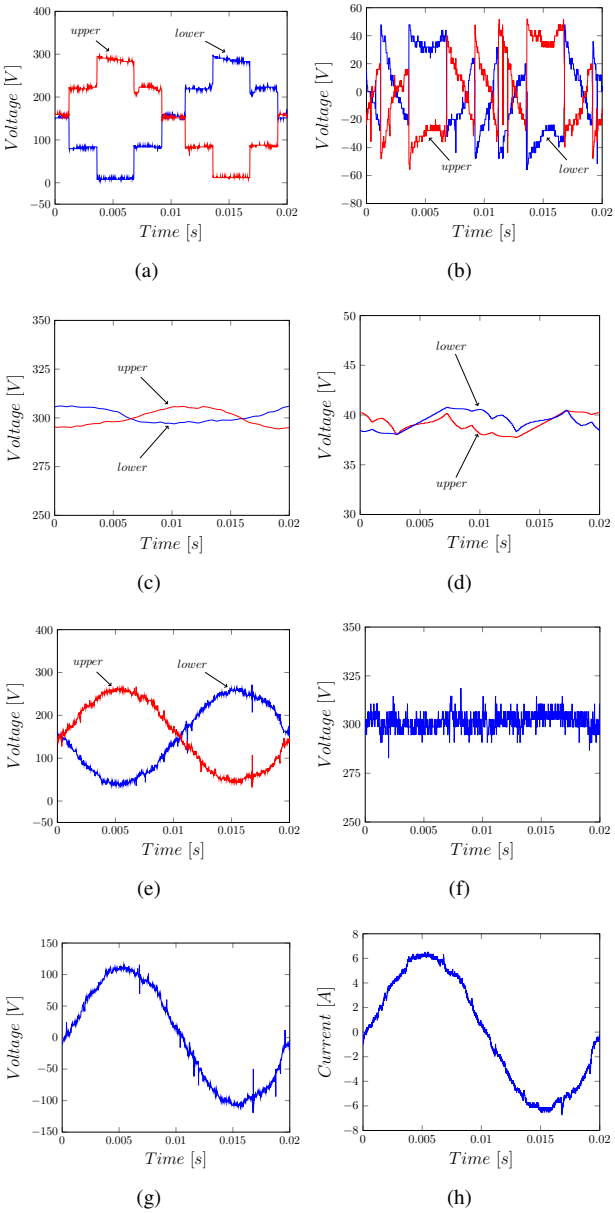


Fig. 10. EMMC experimental results: (a) HB chain-link voltage, (b) FB chain-link voltage, (c) HB chain-link total capacitor voltage, (d) FB chain-link total capacitor voltage, (e) total arm voltage, (f) common-mode voltage, (g) output AC voltage, (h) output AC current.

V. Detailed Quantitative Converter Comparisons

To complement the simulation and experimental validation presented in Section IV, this section demonstrates the scalability of the EMMC to high-voltage applications, using full-scale models developed in the EMTP-RV simulation environment, and considers a number of configurations and comparisons with the conventional MMC. Details of the various MMC configurations being compared are shown in Table IV. In these illustrative simulations, the conventional MMC with 40 medium-voltage cells uses PWM and that with 400 cells uses NLM, whilst the HB and FB chain-links of the EMMC use NLM. Fig. 11 shows simulation waveforms of the conventional MMC with 40 and 400 HB cells, and the EMMC with N_{hb}=40 and N_{fb}=5. The plots for output phase voltages and currents are illustrated in rows (a) and (b) of Fig. 11 and show that all converters being compared produce high quality output voltages. However, the proposed EMMC with 40 medium-voltage HB cells (each rated at 16kV) and 5 FB

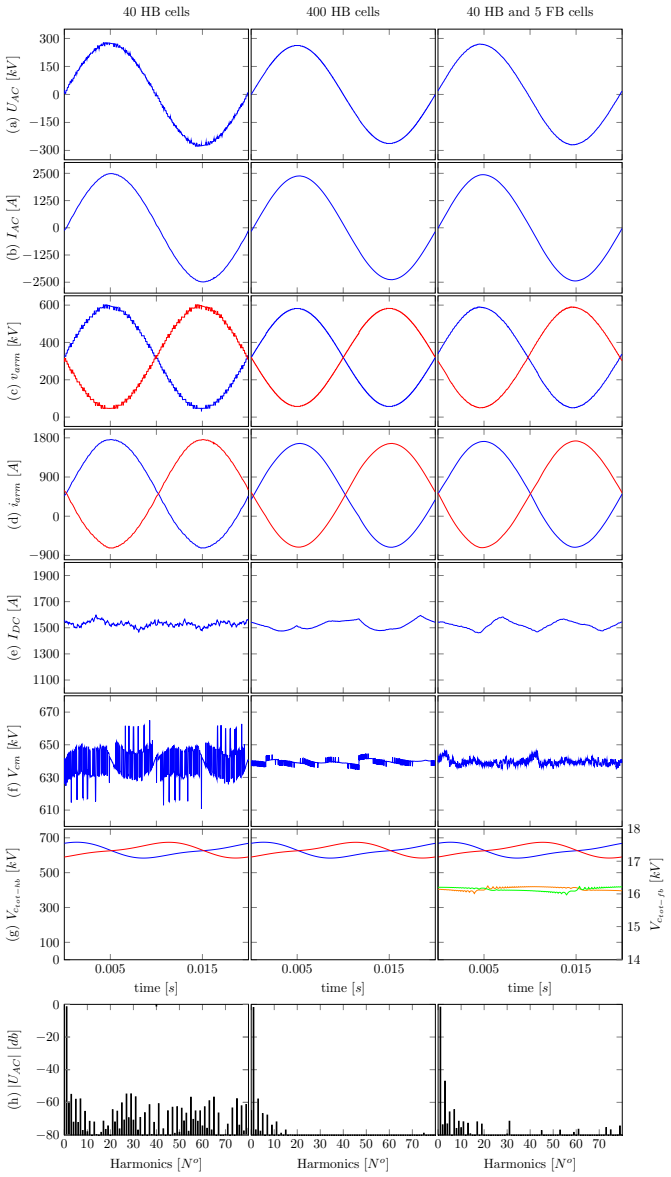


Fig. 11. Waveform comparison between an HB-MMC with 40 (left column) and 400 (middle column) cells, and an EMMC with 40 HB cells and 5 FB cells (right column).

cells (each rated at 1.6kV) produces an output phase voltage with identical quality (THD and dv/dt) to the MMC with 400 HB cells (each rated at 1.6kV). In both cases this performance is superior to that of the conventional MMC with 40 HB cells (THD of the output voltages of the conventional MMC with 40 and 400 HB cells, and the proposed EMMC with 40 HB cells and 5 FB cells are 1.47%, 1.32% and 1.28% respectively). The quality of the output phase currents of the three converters (Fig. 11 row (b)) is practically similar as the arm inductances are sufficiently large to filter out all the high-frequency components associated with MMC switching from the arm currents (Fig. 11 row (d)). The arm voltages of the three MMCs are displayed in Fig. 11 row (c) and confirm the ability of the EMMC with fewer medium-voltage HB cells to match the conventional MMC with a large number of low-voltage HB cells in terms of waveform quality and dv/dt to

TABLE IV
HVDC SPECIFICATIONS

N^o cells	N_{hb}=40	N_{hb}=400	N_{hb}=40 N_{fb}=5
HB chain-link modulation	PWM	NLM	NLM
FB chain-link modulation	-	-	NLM
HB cell voltage [kV]	16	1.6	16
FB cell voltage [kV]	-	-	0.8
HB cell capacitance [mF]	1.30	13.02	1.30
FB cell capacitance [mF]	-	-	6.51
P [MW]	1000		
V_{DC} [kV]	640		
L_{arm} [p.u.]	0.05		

which any AC-side equipment will be subjected. The DC link currents and common-mode voltages shown in Fig. 11 rows (e) and (f) reveal significant injection of high-frequency harmonic components into the DC side of the conventional MMC with 40 medium-voltage HB cells compared to the conventional MMC with 400 HB cells and the proposed EMMC (the DC link voltage ripples of the conventional MMCs with 40 and 400 HB cells per arm, and the EMMC with 40 HB and 5 FB cells per arm, are 5.18%, 0.22% and 0.25% respectively). This is because the large switching cell voltage of the conventional MMC with 40 medium-voltage HB cells (Vc_{hb}= 16kV) creates larger errors in the instantaneous magnitudes of the common-

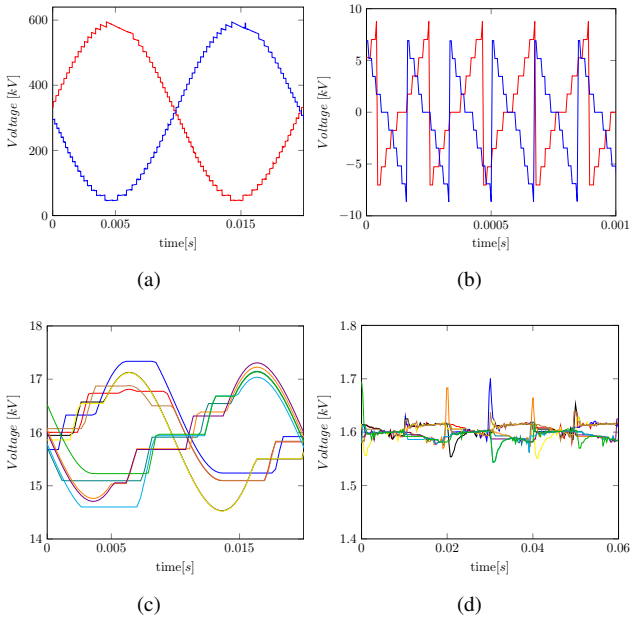


Fig. 12. Internal voltages of EMMC: (a) 40 HB chain-link, (b) 4 FB chain-link, (c) HB capacitor voltages, (d) FB capacitor voltages.

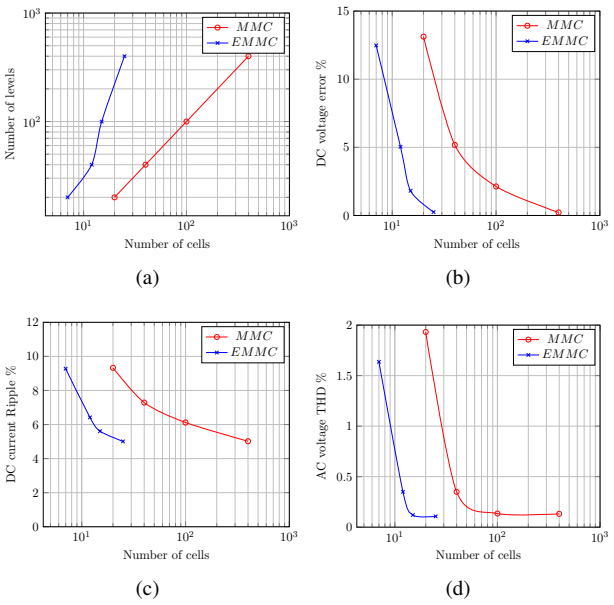


Fig. 13. Scalability of EMMC compared to conventional MMC for various numbers of cells: (a) correlation between number of cells and number of levels produced in each arm, (b) common-mode DC voltage error, (c) DC current ripple, (d) AC phase voltage THD.

mode voltage compared to an MMC with 400 HB cells (Vc_{hb}= 1.6kV) and the proposed EMMC. In practice, the DC link voltage ripple would be exacerbated in the MMC with 40 cells due to the dead-times and the significant mismatch between the turn-on and turn off timings of the series-connected IGBTs. Fig. 11 row (g) shows the total cell capacitor voltage for each of the three converters, and highlights that the total HB cell voltages are well regulated with identical ripple, whilst the total EMMC FB cell voltage is also well regulated and is only a small portion of the total HB cell voltage. Fig. 12 (a) and (b) show that the voltage stresses in the HB and FB cell capacitors and switching devices of the proposed EMMC are well regulated as described in Section III. Fig. 12 (c) and (d) show the voltages synthesized by the EMMC HB and FB chain-links that constitute the total arm voltage shown in the right-hand column of Fig. 11 row (c). These plots show that the FB chain-link voltage represents a small fraction of the total arm voltage, with switching pattern and timing that indicate any potential brief miss-synchronization of the switching instances of the HB and FB chain-links (typically of the order of a few μs) will create low-energy voltage spikes (where the worst case maximum voltage peak will be limited to one half of an HB cell voltage) in the arm voltage which will be absorbed instantly by the upper and lower arm inductances. Thus, no distortion will be observed in the output phase voltage. The spectra of the output voltages displayed in Fig. 11 row (i) confirm the improved harmonic performance of the EMMC compared to that of the conventional HB-MMC with 40 medium-voltage cells.

Fig. 13 shows that for a reduced number of cells, the EMMC can produce the same high-quality output AC voltage (THD, number of voltage levels and dv/dt), DC voltage and current ripple as a conventional MMC with large numbers of cells.

VI. Conclusions

This paper proposes an enhanced MMC topology with a significantly reduced number of cells per arm that generates high-quality AC and DC side waveforms, and a high number of output voltage levels to rival the performance of the conventional MMC with hundreds of cells per arm. This is achieved by incorporating low-voltage FB chain-links with blocking voltage equal to half that of an HB cell. The theoretical development, simulations and experimental results confirm that the EMMC offers reduced AC harmonics and DC voltage ripple with a low number of cells per arm when compared to conventional MMC. The main features of the EMMC are:

- Significant improvements in the power quality of the AC and DC side waveforms without significant increase in the power circuit and control complexity when compared to the conventional MMC.
- In comparison with a conventional MMC with the same number of cells, the EMMC has similar volume but eliminates the need for AC and DC side filters due to significantly improved output power quality.
- The proposed concept of the low-voltage FB chain-link can be integrated into existing, currently operational, low cell count MMC-based HVDC links with minimum modification, and can be implemented in FB-MMC and other hybrid topologies.
- Gains that are achieved in power quality outweigh the marginal increases in semiconductor losses and area due to integration of the low-voltage FB chain-links. These losses may however be reduced by using state-of-the-art semiconductors devices.

VII. Acknowledgement

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