# ROD2522S2H

The ROD2522S2H is a 24-hour holdover leading OCXO, featuring 0.5 ppb FvT stability and advanced self-learning ageing compensation. Operating in standard mode with the primary reference traceable clock input, the device adapts and understands its ageing behaviour.

Engineering with a theme mechanical design and incorporating unique control circuitry, this compact 25 x 22 mm SMD footprint OCXO excels in achieving a 24-hour (≤1.5 µs) holdover, even with a 4°C external temperature variation. The device's holdover mode is supported by frequency ageing compensation (0.004 ppb/day). The device accepts 1PPS input, delivering ultra-stable frequencies at 10, 12.8, or 20 MHz.

Leveraging Rakon's smart compensation and advanced design, the ROD2522S2H ensures precise stability, making it an ideal solution for applications demanding 24-hour holdover and highly accurate frequency stability. Status and commands are accessible through the I²C bus for seamless communication.

## Key specifications

- Frequency (Fn): 10, 12.8 or 20 MHz
- Holdover: 24-hour (≤1.5 µs, 4°C external temperature variation)
- Frequency stability (FvT): 0.5 ppb pk-pk
- Operating temperature: -40 to 85°C
- Compensated ageing: ±0.004 ppb/day
- Free running output: Squarewave with ageing compensation in holdover mode
- Voltage supply: 3.3 V
- I²C bus device status and commands

## Applications

- Edge grandmasters
- DU/CU/servers
- Cell-site routers
- Front-haul switches
- NIC time cards
- Test equipment
- GNSS modules

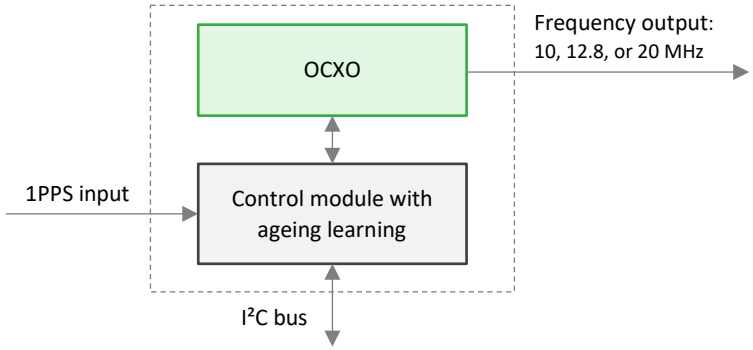
## 25.4 x 22.0 x 12.1 mm

Pb FREE

RoHS COMPLIANT


## Block Diagram – 1PPS Input and Free-running Frequency 10, 12.8 or 20 MHz

- 1PPS input
- Free-running frequency output



# ROD2522S2H

## 1.0 Absolute Maximum Rating[1]

| Parameter | Min. | Max. | Unit | Note |
|---|---|---|---|---|
| a. Storage temperature | -40 | +85 | °C | |
| b. Supply voltage ($V_{CC}$) | -0.3 | 3.6 | V | |
| c. Voltage on PPS input | -0.3 | $V_{CC}$ +0.3 | V | |
| d. Voltage at any digital interface pin with respect to GND | -0.3 | $V_{CC}$ +0.3 | V | |
| e. Load for HCMOS RF Output | | 45 | pF | |
| f. Continuous output current for HCMOS RF output | | ±40 | mA | |

## 2.0 Power Supply

| Parameter | Min. | Typ. | Max. | Unit | Test Condition / Description |
|---|---|---|---|---|---|
| a. Supply voltage ($V_{CC}$) | 3.135 | 3.30 | 3.465 | V | |
| b. Current consumption | | | 1 | A | During warm-up time |
| c. Current consumption | | | 300 | mA | In steady-state & still air at +25°C |
| d. Power-on recall voltage | 2.2 | | | V | Minimum $V_{CC}$ at which memory recall occurs |
| e. $V_{CC}$ ramp rate | 0.2 | | 100 | V/ms | |

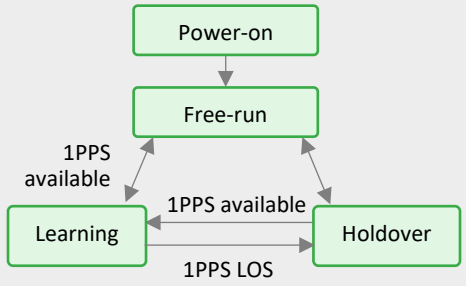
## 3.0 RF Signal Output – HCMOS

| Parameter | Min. | Typ. | Max. | Unit | Test Condition / Description |
|---|---|---|---|---|---|
| a. Low level output voltage ($V_{OL}$) | | | 0.4 | V | |
| b. High level output voltage ($V_{OH}$) | 2.4 | | | V | |
| c. Rise and fall times | | | 5 | ns | from 10% to 90% output levels, 15pF load |
| d. Duty cycle | 45 | | 55 | % | At 50% level |
| e. Load | | 15 | 45 | pF | |
| f. Spurious | | | -80 | dBc | |
| g. Sub-harmonics | | | -40 | dBc | |
| h. Start-up time | | | 1 | Sec | |

[1] Operating beyond this limit may result in change or permanent damage to the device.

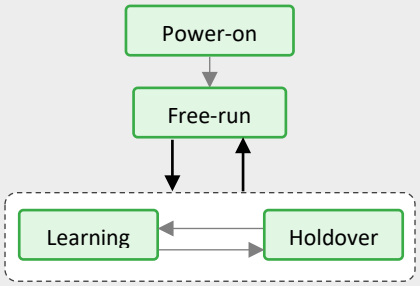
## 4.0 Device Operating States

Generic State Diagram




Default behaviour

Register Driven State Diagram




Some states can be forced through the I²C interface

| State | Condition/Description | Remarks |
|---|---|---|
| a. Power-on | This state corresponds to the initial operating state of the device.<br>Stabilisation steps and order of magnitude:<br>- Start-up time: 1 second after powering on the device; frequency signal output is delivered (valid clock pulses), within ppm of final frequency.<br>- Power consumption will stabilise within 3 minutes after powering on at +25°C; that stabilisation is dependent on ambient temperature at the start.<br>- Ageing slope will reach its final performance after recovery time (see 'Recovery' specification section) | Free-running |
| b. Free-run | No 1PPS input is available<br>Similar to a stand-alone OCXO delivering its intrinsic performances<br>(no ageing compensation in this state). | Free-running |
| c. Learning | 1pps input must be available to initiate the Learning state (OCXO ageing data)<br>Duration of Learning state should be at least twice that of the holdover period targeted. | Free-running |
| d. Holdover | When 1PPS input is unavailable, subsequent to the Learning state, the device goes into Holdover state. This state can also be forced through I²C command<br>• Frequency stability over operating temperature is guaranteed.<br>• After initial power-on, the system requires 3 days of continuous operation to meet specified holdover stability.<br>• The ageing compensation mechanism continuously corrects the frequency up to half of the cumulated locked time, with a limit of 24 hours.<br>• In the holdover state, if the 1PPS signal becomes available again then the module reverts into the learning state. | Ageing compensation applied |

## 5.0 Operating States

| Parameter | Free-run | Learning | Holdover |
|---|---|---|---|
| a. Frequency calibration | Table 1 | NA | NA |
| b. 10 years stability (overall) | Table 1 | NA | NA |
| c. Ageing | Table 1 | NA | NA |
| d. Frequency stability over operating temperature range | Table 1 | NA | Table 3 |
| e. Supply voltage stability | Table 1 | NA | Table 3 |
| f. Load sensitivity | Table 1 | NA | Table 3 |
| g. Acceleration sensitivity | Table 1 | NA | Table 3 |
| h. Warm-up time | Table 1 | NA | NA |
| i. Retrace | Table 1 | NA | NA |
| j. Phase noise | Table 1 | Table 2 | Table 3 |
| k. Short term stability | Table 1 | Table 2 | Table 3 |
| l. 1PPS input | NA | Table 2 | NA |
| m. TIE | NA | NA | Table 3 |

## 6.0 Free-run State – Table 1

| Parameter | | Min. | Typ. | Max. | Unit | Test Condition / Description |
|---|---|---|---|---|---|---|
| a. Nominal frequency | | | 10, 12.8, 20 | | MHz | |
| b. Frequency calibration (at +25°C ±2°C) | | | | ±100 | ppb | At time of shipment, reference to nominal frequency [2] |
| c. 10 years overall stability | | | | ±350 | ppb | After stabilisation of the device (14 days of continuous operation) |
| d. Ageing (at shipment/after recovery time) | | | | | | See § Recovery |
| | per day | | | ±0.2 | ppb | Measured before shipment |
| | per year | | | ±50 | ppb | Cumulated (extrapolation) |
| | 10 years | | | ±250 | ppb | Cumulated (extrapolation) |
| e. Frequency stability over operating temperature range | | | | 0.5 | ppb | Peak-to-peak |
| f. Hysteresis effect | | | | 0.3 | ppb | Over -40 to +85°C, gradient 0.5°C/minute |
| g. Supply voltage stability | | | | ±0.5 | ppb | Nominal $V_{CC}$ ± 5% variation |
| h. Load sensitivity | | | | ±0.5 | ppb | HCMOS: 15pF to 30pF load variation |
| i. Acceleration sensitivity | | | | ±3 | ppb/*g* | Vs. static orientation |
| j. Warm-up time (to ± 10ppb) at +25°C | | | | 3 | Minutes | Reference to frequency after 1 hour of continuous operation |
| k. Retrace vs. operating at ambient | | | | ±5 | ppb | 24h on, 24h off, 1h on |
| l. SSB phase noise (offsets, 20MHz) | | | | | | Static conditions |
| | 1Hz | | -94 | -84 | dBc/Hz | |
| | 10Hz | | -120 | -114 | dBc/Hz | |
| | 100Hz | | -140 | -134 | dBc/Hz | |
| | 1kHz | | -145 | -139 | dBc/Hz | |

[2] The characteristics of the OCXO may be temporarily affected by the processes of assembly, soldering & powered-off time. The frequency specifications apply 48 hours after assembly. Nominal conditions apply unless otherwise stated.

| | | | | | | |
|---|---|---|---|---|---|---|
| | 10kHz | | -150 | -144 | dBc/Hz | |
| m. Short term stability (ADEV) | | | | | | Static conditions |
| | 1s to 100s | | | 3 to 5 | ppt | |
| | 1,000s | | | 3 to 7 | ppt | |
| | 10,000s | | | 10 to 20 | ppt | |

## 7.0 Learning State – Table 2

| Parameter | Min. | Typ. | Max. | Unit | Test Condition / Description |
|---|---|---|---|---|---|
| a. Nominal frequency | | 10, 12.8, 20 | | MHz | |
| b. OCXO parameters – see Free-run State section | | | | | |
| c. 1PPS input | | | | | |
| Waveform compatibility | | | | | HCMOS |
| Low level input voltage ($V_{IL}$) | 0 | | 1.0 | V | |
| High level input voltage ($V_{IH}$) | 2.2 | | $V_{CC}$ | V | |
| Pulse width | 10 | | 10000 | µs | |
| Time deviation (TDEV)<br>Tau = 100s to 10,000s | | 20 | 90 | ns | |

## 8.0 Holdover Stage – Table 3

| Parameter | Min. | Typ. | Max. | Unit | Test Condition / Description |
|---|---|---|---|---|---|
| a. Nominal frequency | | 10, 12.8, 20 | | MHz | |
| b. OCXO parameters – see Free-run State section | | | | | |
| c. Compensated ageing<br>per day | | ±0.004 | | ppb | |
| d. 1.5µs holdover performance (with zero initial frequency and phase error)<br>with 4°C variation (symmetrical)<br>with 10°C variation (asymmetrical)<br>with 20°C variation (asymmetrical) | <br>24<br>8<br>6 | | | hour | With a gradient of 0.83°C/hour |

## 9.0 I²C Bus Interface

| Signal Name | Type | Function | Notes | Logic Levels |
|---|---|---|---|---|
| a. I²C data | Open drain | Serial data | Min 2kΩ external pull-up resistor, conforms to UM10204 NXP I²C bus specification | 2.1V < $V_{IH}$ (High) < 3.3V<br>$V_{IL}$ (Low) < 0.4V |
| b. I²C clock | Open drain | Serial clock | Min 2kΩ external pull-up resistor, conforms to UM10204 NXP I²C-bus specification | 2.1V < $V_{IH}$ (High) < 3.3V<br>$V_{IL}$ (Low) < 0.4V |
| c. Frequency | | | 100kBit/s min - 400kBit/s max | |

Note: At start up, the module performs a self-calibration process after it detects one pulse on 1PPS input. The self-calibration process may last 1 minute maximum. During this time the I²C is not available.

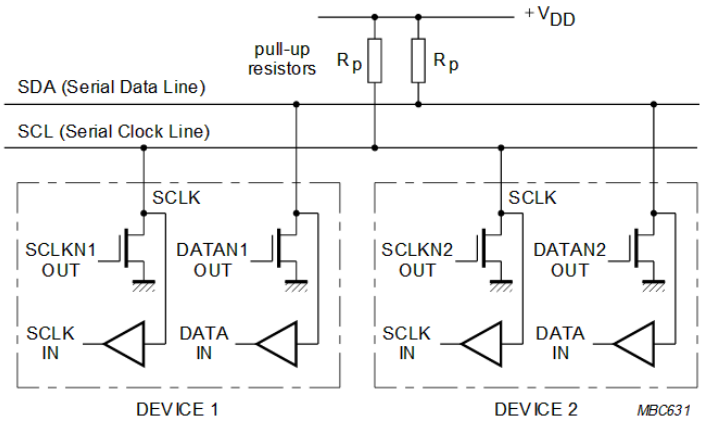
## 10.0 I²C Communication Conditions

I²C is not able to communicate in full-duplex mode, i.e. TX and RX are mutually exclusive. Rakon PPS Module acts as a slave in the communication setup, therefore they cannot initiate data transfers on their own. The host, which is always the master, provides the data clock (SCL), and the clock frequency is therefore not configurable on the slave.

The I²C module is compliant with the NXP Inter-IC bus (I²C bus) specification version 2.1. Fast mode up to 400 kbit/s. Fast-mode devices are downwards compatible i.e. they can be used in a 0 to 100 kbit/s Standard I²C bus system.

Only two bus lines and a ground reference are required; a serial data line (SDA) and a serial clock line (SCL). The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

The master must handle the clock stretching feature as stated in the NXP Inter-IC bus (I²C bus) specification version 2.1 as I²C data might be delayed in case of critical timing sensitive computation.

| | |
|---|---|
| Connection of standard and fast-mode devices to the I²C bus |  |

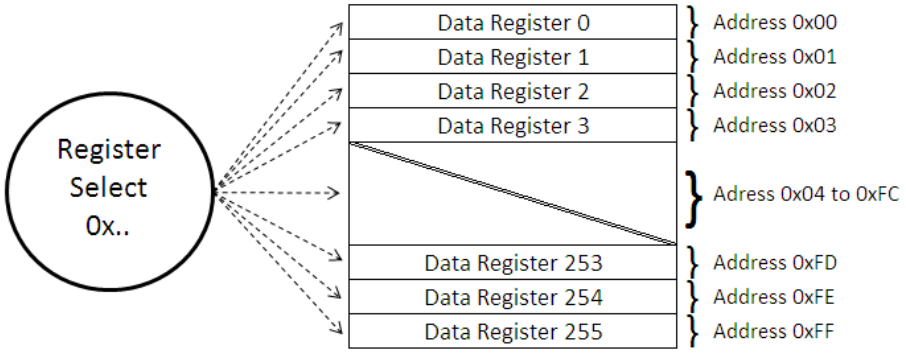
It is generally known that the I²C bus can hang if an I²C master is removed from the bus in the middle of a data read. This can occur because the I²C protocol does not mandate a minimum clock rate. Therefore, if a master is reset in the middle of a read while a slave is driving the data line low, the slave will continue driving the data line low while it waits for the next clock edge.

This prevents bus masters from initiating transfers. If this condition is detected, the following three steps will clear the bus hang condition:

1. An I²C master must generate up to 9 clock cycles.
2. After each clock cycle, the data pin must be observed to determine whether it has gone high while the clock is high.
3. As soon as the data pin is observed high, the master can initiate a start condition.

The receiver's I²C address is set to **0xE0** by default. This address can be changed on request.

The I²C interface allows 256 slave registers to be addressed. As shown in Figure *I²C Register Layout* only a few of these are currently implemented. Others are reserved for future uses or internal computation and must not be addressed.

| | |
|---|---|
| I²C bus register layout |  |

### Register Detail

The next section contains information about the Rakon module register.

| | |
|---|---|
| **Slave Register:** | Refers to the address that has to be sent after the I²C slave address to select the desired register. |
| **Description:** | Name and function of the register. |
| **Firmware:** | Details on the firmware revision the register is supported on. |
| **Comment:** | Additional information regarding the register or the data it represents. |
| **Message Info:** | Number of bytes to be read and data type of the data register. |

| Slave Register | **0x3E** | | |
|---|---|---|---|
| Description | Read Temperature Sensor | | |
| Firmware | 1.4+ | | |
| Comment | Represents an image of the external temperature seen by the module.<br>The value can vary from Ox0000 to Ox0FFF, negative slope | | |
| Message Info | # bytes | Datatype | |
| | 2 | U-Short | |

| Slave Register | **0x41** | | |
|---|---|---|---|
| Description | Read Frequency Control | | |
| Firmware | 1.4+ | | |
| Comment | Range can swing from Ox00000000 to Ox000C8320.<br>8E-13 typical frequency variation per step | | |
| Message Info | # bytes | Datatype | |
| | 4 | U-Long | |

| Slave Register | **0x42** | | |
|---|---|---|---|
| Description | Read Status | | |
| Firmware | 1.4+ | | |
| Comment | Gives information regarding the state of the module and other parameters.<br>Refer to Figure Status Details for more informations. | | |
| Message Info | # bytes | Datatype | |
| | 2 | Char | |

| Slave Register | **0x50** | | |
|---|---|---|---|
| Description | Read Product Identification | | |
| Firmware | 1.4+ | | |
| Comment | Product traceability information<br>ASCII format | | |
| Message Info | # bytes | Datatype | |
| | 64 | Char | |

| Slave Register | **0x51** | | |
|---|---|---|---|
| Description | Read firmware revision | | |
| Firmware | 1.4+ | | |
| Comment | Includes the name, version revision, release date and special parameters.<br>ASCII format | | |
| Message Info | # bytes | Datatype | |
| | 64 | Char | |

| Slave Register | **0x52** |
|---|---|
| Description | Read Relative Time Interval Error |
| Firmware | 1.4+ |
| Comment | Time Interval Error in nanosecond with an offset of +2000ns.<br>Only available when system is locked and phase measurement is available.<br>When there is no PPS measurement, system phase equivalent ageing is displayed.<br>Ox0000 to Ox0FFF |

| Message Info | # bytes | Datatype | |
|---|---|---|---|
| | 2 | U-Short | |

| Slave Register | **0x92** | | |
|---|---|---|---|
| Description | Read holdover override status | | |
| Firmware | 1.4+ | | |
| Comment | Either 0x0000 or 0x0001. | | |
| | If 0 then the system is in holdover even if PPS input is available. | | |
| Message Info | # bytes | Datatype | |
| | 2 | U-Short | |

## Status Detail

The status channel is a bitfield, as shown below:

| Byte MSB | | | | | | | | Byte LSB | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0** | **x** | Syst.F | **1** | HV | Lock Status | IsPPS |

MSB byte is always 0x00

| | | | | |
|---|---|---|---|---|
| **0** | Must be 0 for normal operation. | | | |
| **x** | Undefined | | | |
| Syst.F | System Fail check. If PPS has been provided. | | | |
| **1** | Must be 1 for normal operation. | | | |
| HV | 1 : Holdover state, no PPS detected.<br>0 : not in Holdover state, PPS detected | | | |
| Lock Status | | **PPS** | **Learning** | **RF Output** |
| | b00 | - | N/A | N/A |
| | b01 | OK | OK | Ageing compensation not available |
| | b10 | OK | OK | Ageing compensation available |
| IsPPS | Is there a valid PPS input? 0: No / 1: Yes | | | |

## Write Access

| Slave Register | **0x90** | |
|---|---|---|
| Description | Holdover override. | |
| Firmware | 1.4+ | |
| Comment | Force the part to go into holdover even if the PPS signal is present. | |
| | | |
| Message Info | # bytes | Datatype |
| | none | none |

| Slave Register | **0x91** | |
|---|---|---|
| Description | Disable the holdover override. | |
| Firmware | 1.4+ | |
| Comment | Force the part to go out of holdover and into free-run state even if the PPS signal is not available. | |
| | | |
| Message Info | # bytes | Datatype |
| | none | none |

| Slave Register | **0x96** | | |
|---|---|---|---|
| Description | Disable learning and force Free-run state | | |
| Firmware | 1.5+ | | |
| Comment | Disable learning feature even if PPS signal is present – Forces the part in Free-run state | | |
| Message Info | # bytes | # bytes | |
| | none | none | |

| Slave Register | **0x97** | | |
|---|---|---|---|
| Description | Enables learning | | |
| Firmware | 1.5+ | | |
| Comment | Clears the 'Disable learning' setting (see 0x96)<br>Enables learning feature – Device goes into relevant run state | | |
| Message Info | # bytes | # bytes | |
| | 2 | 2 | |

| Slave Register | **0x98** | | |
|---|---|---|---|
| Description | Clear learning parameters | | |
| Firmware | 1.5+ | | |
| Comment | Clears all stored learning parameters acquired – once enacted, device would start learning from scratch if feature is enabled.<br>If used in Holdover state, then device would go out of Holdover (to Free-run or Learning state) | | |
| Message Info | # bytes | # bytes | |
| | 2 | 2 | |

## 11.0 Marking

| Parameter | Test Condition / Description |
|---|---|
| a. Type | Label |
| b. Line 1 | [ Manufacturer identifier ] RAKON |
| c. Line 2 | [ Part Number ][3] SPT####LF |
| d. Line 3 | [ Nominal Frequency ] E.g., 20MHz |
| e. Line 4 | [ Serial Number] 1 Letter + 5 Numerals - SN: L12345 \| Batch info |
| f. Line 5 | [ Manufacturing Date Code ] 4 digits for Year & Week code - DC: YyWw |
| QR code | [QR code] Batch information  |



[3] Part Number Convention

## 12.0 Environmental Specification

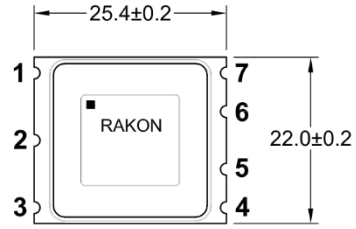
| Parameter | Min. | Typ. | Max. | Unit | Test Condition / Description |
|---|---|---|---|---|---|
| a. Operating temperature range | -40 | | +85 | °C | Temperature gradient ≤ ± 0.5°C/minute, airflow speed between 1m/s and 3 m/s |
| b. Relative Humidity | 5 | | 95 | % | |
| c. Air Pressure | 70 | | 106 | kPa | |

## 13.0 Quality and Reliability Requirements[4]

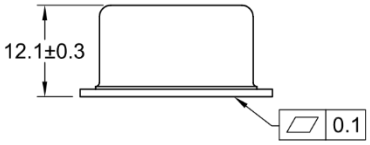
| Parameter | Test Condition / Description |
|---|---|
| a. RoHS compliant | Parts are fully compliant with the European Union directives 2002/95/EC and 2011/65/EU on the restriction of the use of certain hazardous substances in electrical and electronic equipment; with exemption 7(c)-1. Note the RoHS compliant parts are suitable for assembly using both Lead-free solders and Tin/Lead solders. |
| b. Vibration | Mechanical vibration (JESD22-B-103B, MIL-STD-883 Cond. A)<br>From 20Hz to 2kHz / 4 minutes per orthogonal axis with 20*g* acceleration |
| c. Shocks | Mechanical shocks (JESD22-B-104C, MIL-STD-202 meth 213 Cond. C)<br>6 shocks per direction with 100*g* acceleration - 6ms duration - 6 orthogonal directions |
| d. Electro-static discharge | ESD-CDM (JSESD22-C101 class C1 / 500V)<br>ESD-HBM (JESD22-A114-F / 2000V) |
| e. Latch-Up Test (LUT) | JESD78 Class II Forced current limits ± 100mA |
| f. High Temperature Operating Life (HTOL) test | HTOL over 1000hours at +125°C / $V_{CC}$=+3.5V |
| g. High Temperature Storage (HTS) | HTS over 1000 hours at +125°C |
| h. Low Temperature Storage (LTS) | LTS at -40°C 100 hours |
| i. Temperature Cycling Test (TCT) | TCT from -40°C to +125°C (JESD22-A-104)<br>500 cycles - 10 minutes Soak time with 2 cycles per hour – transfer ≤ 1 minute |
| j. MSL | MSL-3 |

[4] Qualification, not operational

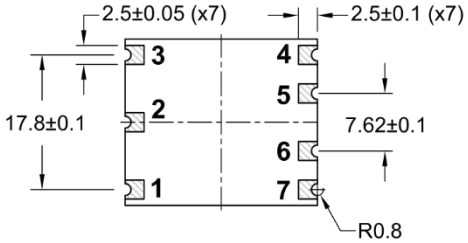
## 14.0 Model Outline




TOP VIEW



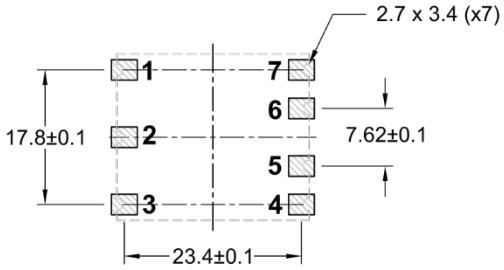

FRONT VIEW




BOTTOM VIEW

**RECOMMENDED PAD LAYOUT**

- TOP VIEW




**NOTE**

- Planarity of the bottom PCB ≤0.15mm typicao ≤0.1mm / PCB interfacing with customer's board
- No via, no trace on bottom side
- Unit: mm. Tolerance is ±0.2 mm if it has not been indicated.

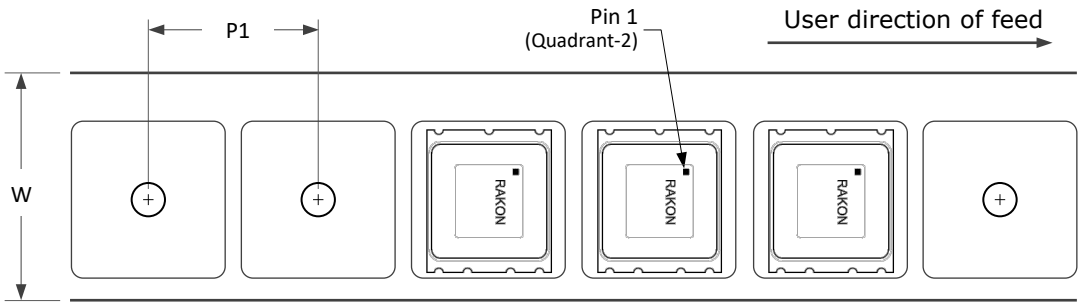
| Pin | Connections |
|---|---|
| **1** | 1PPS input |
| **2** | Do not connect |
| **3** | Supply Voltage ($V_{CC}$) |
| **4** | RF Output (HCMOS) |
| **5** | $I^2C$ bus – SCL |
| **6** | $I^2C$ bus – SDA |
| **7** | GND (mechanical & electrical) |

## 15.0 3D Model

| Parameter | Remarks |
|---|---|
| Package size | 25.4 x 22.0 x 12.1 mm |
| Net weight | 11 g/pc |
| STEP file | ROD2522S2H 7-pad 3D model<br>*To open or view the STP file, you will need to import it into one of the following software programs: Autodesk Fusion 360, CATIA, SolidWorks, Solid Edge, TurboCAD, Kubotek KeyCreator, FreeCAD, ABViewer, ShareCAD, or eMachineShop.* |

## 16.0 Tape and Reel

Tape and reel packaging: compliant with Standard EIA-481

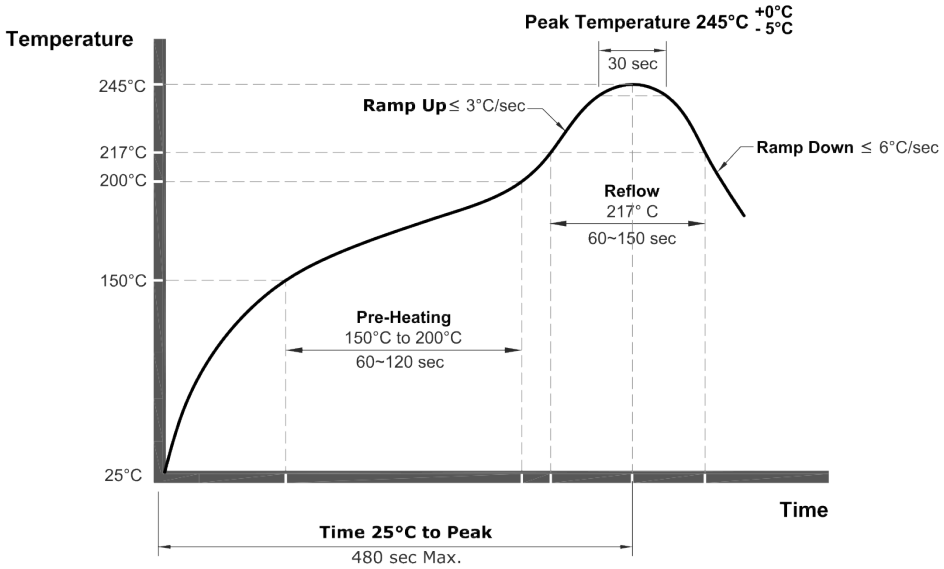



| P1 | W | SPQ/reel | Reel diameter | Pin 1 orientation |
|---|---|---|---|---|
| 28 mm | 44 mm | 100pcs. min. 200pcs. max | Φ380 mm | Quadrant-2 |

## 17.0 Recommended Reflow Profile

Reflow profile according IPC/JEDEC J-STD-020 with classification temperature Tc 245°C.

- This product is specifically designed for pick and place reflow manufacturing process.
- The Oscillator must be always on top side during the reflow process.
- The product might be damaged or destroyed when processed top down during second reflow process.




## 18.0 Evaluation Kit

Evaluation Kit ref: ROD2522S2 EVK (520815)

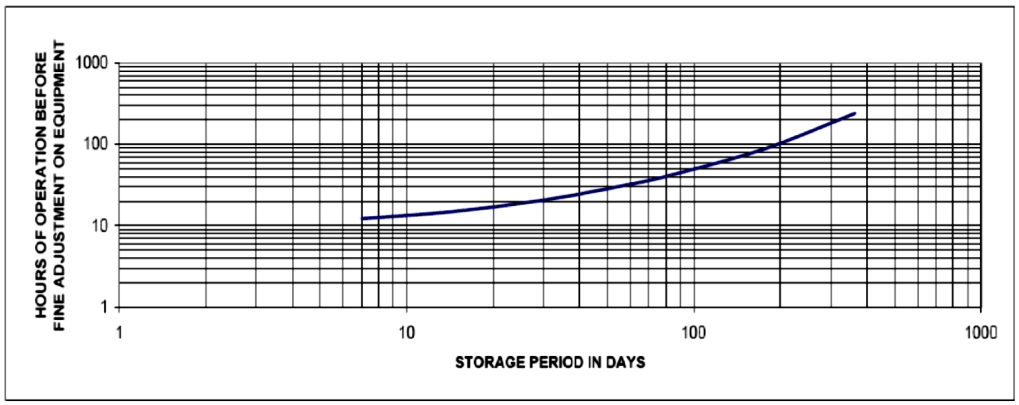
- RAKON EVK Hardware Installation Guide
- RAKON EVK Software User Guide

## 19.0 Recovery

The stability performances of the device are measured before shipment. Then parts are shipped and could remain powered-off for an uncontrolled time, then assembled and tested over the integration process.

Parts could again remain powered off until final installation in the application when they will operate in a continuous mode.

The graph on the right shows the typical recovery time as a function of the unpowered time:




## 20.0 Disclaimer

| Parameter | Test Condition / Description |
|---|---|
| a. Disclaimer | "Samples supplied according to this specification are supplied from our development or pre-production programme and are not qualification approved products. No condition, warranty or representation regarding quality, suitability, performance, life or continuation of supply is given or implied, and the Warranty in clause 7 of our standard Conditions of Sale is not applicable. The right is reserved to change the design or specification or cease supply without notice." Rakon Limited |