
# Samsung S3C2450 Mobile Processor

## RICH FEATURE SET AT LESS COST FOR PERSONAL NAVIGATION DEVICES AND OTHER HANDHELDS

**The 65nm S3C2450** is the new generation of Samsung's popular S3C24xx series, offering pin-to-pin compatibility along with a wealth of new features that were chosen based on customer feedback.

## High Performance and Low Power Requirements; Advanced Design Enables Fast Time to Market

The Samsung S3C2450 mobile application processor is the first ARM9 RISC microprocessor based on Samsung's 65nm low-power CMOS process, giving designers an excellent combination of advanced features and longer battery life while lowering overall system costs. In addition to mid-range Personal Navigation Devices (PNDs), the S3C2450 is an appealing solution for wirelessly connected consumer electronics and other embedded applications requiring high-performing ARM9 processors.

Samsung's processor is the latest in its popular S3C24xx series, offering pin-to-pin compatibility with the S3C2443 along with a wealth of new features that were chosen based on customer feedback. The addition of 2D graphics enhances screen images while a new two-channel high-speed SPI enables mobile tv and WiFi connectivity. Other multimedia improvements include better audio quality through support of a 5.1-channel Dolby digital codec interface and 12-bit ADC to support touchscreens with higher resolution in larger screen sizes.

New interfaces have been added to the S3C2450 to support more memory options. For example, the processor allows the use of DDR2 DRAM memory to cut costs while delivering great performance. Another improvement is a new power-saving setting called "deep-stop power mode" that minimizes power usage during standby.

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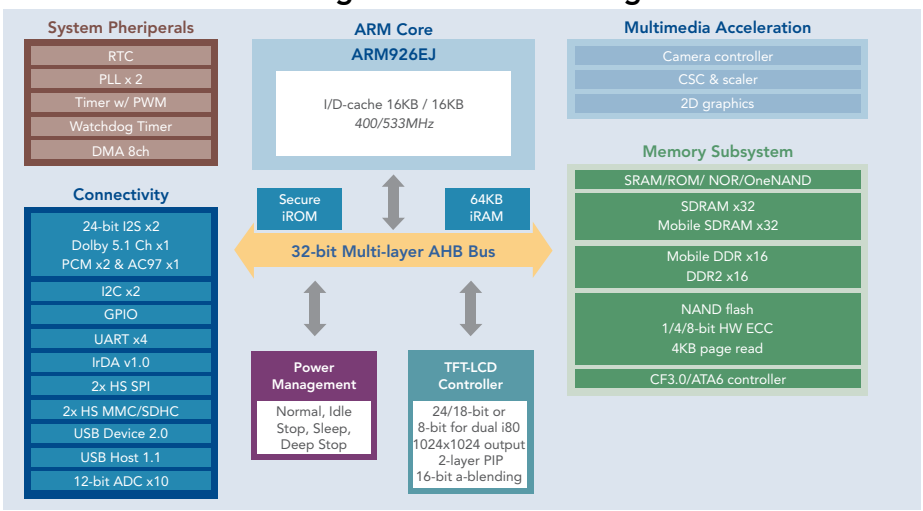
### Samsung S3C2450 Block Diagram



**With its excellent** multimedia capabilities and low cost, the Samsung S3C2450 is a good choice for connected mobile handheld devices and other embedded applications needing an LCD display.

This new processor still offers the rich set of peripheral interfaces — accommodating cameras, screens, storage and other items — and super-fast, multilayered memory bus architecture that have made Samsung processors the frequent choice of mobile product designers.

## Processor is "Nav-Ready" for Windows®-based PNDs

One of the many strengths of Samsung's S3C2450 is its support of Microsoft's Windows Embedded NavReady™, which lets developers quickly design PNDs compatible with Windows CE 5.0 with minimal effort. This "out-of-the-box" software architecture supports a connected navigation-device experience, enabling applications to receive information or access services from various sources including Bluetooth-enabled devices, Internet servers, Live Search engines, desktop computers or car audio kits. NavReady helps to lower development costs and accelerates time to market by introducing new technology into familiar development environments.

## Compatible with Earlier Generation

Samsung's new S3C2450 processor is available in a 400-pin, .5mm-pitch 13x13 FBGA package. Pin-to-pin compatibility with the earlier-generation S3C2443 simplifies upgrades for existing customers. This popular processor was known for its optimal performance and features for advanced handheld devices and has been used by major worldwide customers in a variety of graphics-intensive applications.

## Compatible with Earlier Generation

- ARM926EJ CPU, 400MHz and 533MHz with 16KB I-cache/16KB D-cache/MMU
- Dual-port external memory controller (DRAM/ROM controller and chip select logic)
- 32KB internal ROM and 64KB internal RAM allows booting from 4KB 8-bit MLC NAND, OneNAND and moviNAND flash
- x16 DDR2 support
- Deep-stop mode
- 2D hardware support
- 2 high-speed SPIs
- LCD controller with LCD-dedicated DMA
- Camera controller
- 2D graphics accelerator
- 8-ch DMAs with external request pins
- 4-ch UART with IrDA 1.0
- 2-ch HS SPI
- CF+ & ATA I/F
- 2-ch multi-master IIC
- 2-ch IIS controller (1-ch support of Dolby 5.1 channel) and combined PCM and AC97 I/F
- 2-ch SD host controller v2.0 (SDHC) & multimedia card protocol v2.11 (HS MMC)
- 1-port USB host v1.1 full speed
- 1-port USB dev v2.0 high speed
- 4-ch PWM timers & 1-ch internal timers
- Real-time clock & watchdog timer
- 2 PLLs with on-chip clock generator
- Power modes: Normal, Idle, Stop & Deep Stop, Sleep and Power-off
- MtCMOS technology incorporated
- 10-ch 12-bit ADC (touchscreen interface)
- 32KB internal ROM/64KB internal SRAM
- 128-bit e-Fuse for security
- 65nm low-power technology
- Package: 400-pin 0.5mm-pitch 13x13 FBGA (compatible with S3C2443)

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