AVR099: Replacing AT90S4433 by ATmega48

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Introduction

This application note is a guide to assist current AT90S4433 users in converting existing designs to ATmega48. ATmega48 is not designed to be a replacement for AT90S4433, but is pin compatible and has a very similar feature set.

ATmega48 contains more SRAM memory than AT90S4433, and it has additional peripheral modules and features. However with a few modifications to the I/O register access, ATmega48 can replace AT90S4433 on existing circuit boards. In addition to the functional changes, the electrical characteristics of the ATmega48 are different, including an increase in operating frequency ranges. Check the datasheet for detailed information.

Improvements and added features in ATmega48 that are not in conflict with those in AT90S4433 are not covered by the scope of this document. Throughout this document it is assumed that ATmega48 factory-default settings are used unless otherwise noted.

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Application Note

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AT90S4433 Errata Corrected in ATmega48

The following items from the Errata Sheets of AT90S4433 do not apply to ATmega48. Refer to the AT90S4433 Errata Sheet for a more detailed description of the Errata. All workarounds suggested in the AT90S4433 errata will work for the ATmega48, although these workarounds are no longer needed.

BOD Keeps the Device in Reset at Low Temperature

In ATmega48, the Brown-out Detector will not keep the device in Reset at low temperatures as long as the device is operated inside the voltage and frequency range specified in the datasheet for ATmega48.

Fuses and Programming Mode

When programming the ATmega48 in Serial Programming mode, it is possible to program the Flash and EEPROM after programming the Fuses. If leaving Serial Programming mode, it is possible to re-enter Programming mode.

Incorrect ADC Channel Changes in Free Running Mode

In ATmega48, the MUXn and REFS1:0 settings are buffered through a temporary register to which the CPU has random access. This ensures that the channels and reference selection only takes place at a safe point during the conversion. Refer to the ATmega48 data sheet for further information and advice on how to change these registers in Free Running mode.

Bandgap Reference Stabilizing Time

In ATmega48, the Bandgap Reference Voltage stabilizes within the time specified in the data sheet, independent from whether the internal Brown-out Detector is enabled or not.

Brown-out Detection Level

In ATmega48, the Brown-out Detection level is not influenced by activity on the I/O-pins.

Serial Programming at Voltages below 2.9V

There are no restrictions on the supply voltage or system frequency as long as the device is operated inside the voltage and frequency range specified in the datasheet for ATmega48.

UART Looses Synchronization if RXD line is Low when UART Receive is disabled

The UART is replaced by a USART, which does not have this problem. The starting edge of a reception is only accepted as valid if the Receive Enable bit in the USART Control Register is set.

Pin out

ATmega48 has alternate functions on most of its I/O pins that the AT90S4433 do not have. This will normally not create any problem when porting the code, as long as the alternate functions (which were not present in AT90S4433) are not used. The following sections discuss issues concerning the pin-out that the designer should consider when porting a design from AT90S4433 to ATmega48.

PB7:6 (XTAL/TOSC)

AT90S4433 has dedicated pins for XTAL1 and XTAL2, while ATmega48 combines the I/O pin PB7 with XTAL2 and TOSC2, and the I/O pin PB6 with XTAL1 and TOSC1. Set the CKSEL Fuses to select external crystal/ceramic resonator, external low frequency crystal or external clock, and the pins will be dedicated to XTAL1 and XTAL2 as in AT90S4433.

Interrupt Vector Table

All interrupt vectors on AT90S4433 have an equivalent on ATmega48. Because ATmega48 has more interrupts, most vectors have moved to other locations. Some interrupts also have changed names, but the functionality is the same. Table 1 below lists the vectors of AT90S4433 and their equivalents in ATmega48. The table does not show vectors in ATmega48 that do not have equivalents in AT90S4433. Refer to the ATmega48 datasheet for details on the extra interrupts.

Table 1. Interrupt vectors in AT90S4433 and ATmega48 equivalents

AT90S4433			**ATmega48**		
Vector #	**Address**	**Name**	**Vector #**	**Address**	**Name**
1	$00	RESET	1	$00	RESET
2	$01	INT0	2	$01	INT0
3	$02	INT1	3	$02	INT1
4	**$03**	**TIMER1 CAPT**	**11**	**$0A**	**TIMER1 CAPT**
5	**$04**	**TIMER1 COMP**	**12**	**$0B**	**TIMER1 COMPA**
6	**$05**	**TIMER1 OVF**	**14**	**$0D**	**TIMER1 OVF**
7	**$06**	**TIMER0 OVF**	**17**	**$10**	**TIMER0 OVF**
8	**$07**	**SPI, STC**	**18**	**$11**	**SPI, STC**
9	**$08**	**UART, RX**	**19**	**$12**	**USART, RX**
10	**$09**	**UART, UDRE**	**20**	**$13**	**USART, UDRE**
11	**$0A**	**UART, TX**	**21**	**$14**	**USART, TX**
12	**$0B**	**ADC**	**22**	**$15**	**ADC**
13	**$0C**	**EE_RDY**	**23**	**$16**	**EE READY**
14	**$0D**	**ANA_COMP**	**24**	**$17**	**ANALOG COMP**

I/O Registers and Bits

This section lists all the I/O registers in AT90S4433 that are not identical in ATmega48. Most registers and bits have a functional equivalent in ATmega48, some with new names and/or addresses. Use Table 2 to replace all register and bit references in your code, then read through the rest of this document for changes in functionality. Note that ST/STS/STD and LD/LDS/LDD instructions must be used to access the Extended I/O space in ATmega48.

The information in Table 2 assumes that all registers and bits that are unused/reserved in AT90S4433 is left untouched in ATmega48. Registers and bits in ATmega48 that have no equivalents in AT90S4433 are not included in the table, and should keep their initial values.

Table rows that show register names and no bit names are identical in AT90S4433 and ATmega48. Only register address and/or name is changed.

Table 2. Registers and bits in AT90S4433 and ATmega48 equivalents

AT90S4433										ATmega48										A	B	E	P	R	Notes
$3D ($5D)	SP									$3E ($5E) $3D ($5D)	SPH SPL									X				X	1
$3B ($5B)	GIMSK	INT1	INT0							$1D ($3D)	EIMSK							INT1	INT0	X			X	X	
$3A ($5A)	GIFR	INTF1	INTF0							$1C ($3C)	EIFR							INTF1	INTF0	X			X	X	
$39 ($59)	TIMSK	TOIE1	OCIE1				TICIE1		TOIE0	($6F) ($6E)	TIMSK1 TIMSK0				ICIE1			OCIE1A	TOIE1 TOIE0	X	X	X	X	X	2
$38 ($58)	TIFR	TOV1	OCF1				ICF1		TOV0	$16 ($36) $15 ($35)	TIFR1 TIFR0				ICF1			OCF1A	TOV1 TOV0	X	X		X	X	3
$35 ($55)	MCUCR			SE	SM	ISC11	ISC10	ISC01	ISC00	($69) $33 ($53)	EICRA SMCR						ISC11	ISC10 SM1	ISC01 SE	ISC00	X	X	X	X	X	4
$33 ($53)	TCCR0							CS02	CS01	CS00	$25 ($45)	TCCR0B							CS02	CS01	CS00	X				X	
$32 ($52)	TCNT0										$26 ($46)										X					
$2F ($4F)	TCCR1A	COM11	COM10					PWM11	PWM10	($80)		COM1A1	COM1A0						WGM11	WGM10	X	X	X			5
$2E ($4E)	TCCR1B	ICNC1	ICES1			CTC1	CS12	CS11	CS10	($81)		ICNC1	ICES1			WGM12	CS12	CS11	CS10		X	X			6
$2D ($4D)	TCNT1H									($85)										X		X			
$2C ($4C)	TCNT1L									($84)										X		X			
$2B ($4B)	OCR1H									($89)	OCR1AH									X		X		X	
$2A ($4A)	OCR1L									($88)	OCR1AL									X		X		X	
$27 ($47)	ICR1H									($87)										X		X			
$26 ($46)	ICR1L									($86)										X		X			
$21 ($41)	WDTCR				WDTOE	WDE	WDP2	WDP1	WDP0	($60)	WDTCSR				WDP3	WDCE	WDE	WDP2	WDP1	WDP0	incompatible					7
$1E ($3E)	EEAR									$21 ($41)	EEARL									X				X	
$1D ($3D)	EEDR									$20 ($40)										X					
$1C ($3C)	EECR					EERIE	EEMWE	EEWE	EERE	$1F ($3F)							EERIE	EEMPE	EEPE	EERE	X	X				8
$18 ($38)	PORTB									$05 ($25)										X					
$17 ($37)	DDRB									$04 ($24)										X					
$16 ($36)	PINB									$03 ($23)										X					
$15 ($35)	PORTC									$08 ($28)										X					
$14 ($34)	DDRC									$07 ($27)										X					
$13 ($33)	PINC									$06 ($26)										X					
$12 ($32)	PORTD									$0B ($2B)										X					
$11 ($31)	DDRD									$0A ($2A)										X					
$10 ($30)	PIND									$09 ($29)										X					
$0F ($2F)	SPDR									$2E ($4E)										X					
$0E ($2E)	SPSR									$2D ($4D)										X					
$0D ($2D)	SPCR									$2C ($4C)										X					
$0C ($2C)	UDR									($C6)	UDR0									X		X		X	
$0B ($2B)	UCSRA	RXC	TXC	UDRE	FE	OR				($C0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0				X	X	X		X	9
$0A ($2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	($C1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	X	X	X		X	9, 10
$09 ($29)	UBRR									($C4)	UBRR0L									X		X		X	
$08 ($28)	ACSR	ACD	AINBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	$30 ($50)		ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	X	X				11
$07 ($27)	ADMUX									($7C)										incompatible					12
$06 ($26)	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	($7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	X	X	X		X	13
$05 ($25)	ADCH									($79)										X		X			
$04 ($24)	ADCL									($78)										X		X			
$03 ($23)	UBRRHI									($C5)	UBRR0H									X		X		X	

Notes: A – Register address is changed
B – One or more bit names are changed
E – Register moved to Extended I/O space
P – One or more bit positions are changed
R – Register name is changed
Registers/bits in bold have changed names from AT90S4433 to ATmega48

1. Stack Pointer is 10bits in ATmega48
2. TICIE1 renamed to ICIE1
3. OCF1 renamed to OCF1A
4. SM renamed to SM1
5. COMxx renamed to COMxAx and PWMxx to WGMxx
6. CTC1 renamed to WGM12
7. See section “Watchdog Timer” below
8. EEMWE renamed to EEMPE and EEWE to EEPE
9. All bit names are renamed to xxx0
10. CHR9 renamed to UCSZ02
11. AINBG renamed to ACBG
12. See section “ADC” below
13. ADFR renamed to ADATE

Timer/Counters and Prescalers

For details about the improved and additional features, please refer to the datasheet. The following features have been added:

- The Prescalers in ATmega48 can be reset.
- Variable top value in PWM mode.
- Timer/Counter1 has Phase and Frequency Correct PWM mode in addition to the Phase Correct PWM mode.
- Fast PWM mode.

Differences Between ATmega48 and AT90S4433

Most of the improvements and changes apply to all the Timer/Counters and the description below is written in a general form. A lower case “x” replaces the output channel (A or B for Timer/Counter1, N/A for Timer/Counter0), while “n” replaces the Timer/Counter number (n = 0 or 1). Timer/Counter2 is not present in AT90S4433.

TCNT1 Cleared in PWM Mode

In AT90S4433 there are three different PWM resolutions – 8, 9, or 10 bits. Though only 8, 9, or 10 bits are compared, it is still possible to write values into the TCNT1 Register that exceed the resolution. Thus, the Timer/Counter has to complete the count to 0xFFFF before the reduced resolution becomes effective (i.e. if 8-bit resolution is selected and the TCNT1 Register contains 0x0100, the top value 0x00FF will not be effective until the counter has counted up to 0xFFFF, turned, and counted down to 0x0000 again). In ATmega48 this has been changed so that the unused bits in TCNT1 are being cleared to zero to avoid this unintended counting up to 0xFFFF. In ATmega48, the TCNT1 Register never exceeds the selected resolution.

OCR1xH Cleared in PWM Mode

Clearing OCR1xH in PWM mode is slightly different from clearing TCNT1. AT90S4433 clears the six most significant bits if 8, 9, or 10 bits PWM mode is selected. Hence, if 0xFFFF is written to OCR1x in PWM mode and OCR1x is read back, the result is 0x03FF regardless of which PWM mode is selected. In ATmega48 the number of cleared bits depends on the resolution.

Clear Timer/Counter1 on Compare Match with Prescaler

The relation between a Clear on Compare match and the internal counting of the Timer/Counters has been changed. The Clear on Compare match in AT90S4433 clears the Timer/Counter after the first internal count matching the compare value, whereas ATmega48 clears the Timer/Counter after the last internal count matching the compare value. See Figure 1 and Figure 2 for details on clearing, flag setting, and pin change.

Example: OCR1x = 0x02 when prescaler is enabled (divide clock by eight). The “↑” indicates where the Output Compare Flag/Pin will be set.

Figure 1. Setting Output Compare Flag/Pin for AT90S4433

TCNTn	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 0 0 0 0 0 0 0
Pin/Flag	↑ ↑

Figure 2. Setting Output Compare Flag/Pin for ATmega48

TCNTn	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
Pin/Flag	↑

Setting of Output Compare Pin/Flag with Prescaler Enabled (Applies to all Timer/Counters)

The relation between an Output Compare and the internal counting of the Timer/Counter has been changed. Output Compare in the AT90S4433 sets the Output Compare pin/flag after the first internal count matching the compare value, whereas the ATmega48 sets the Output Compare pin/flag after the last internal count matching the compare value. See Figure 3 and Figure 4 for details on Output Compare Flag setting and pin change.

Example: OCR1x = 0x02, prescaler enabled (divide clock by 8). The "↑" indicates where the Output Compare Flag/Pin will be set.

Figure 3. Setting Output Compare Flag/Pin for AT90S4433

TCNTn	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4
Pin/Flag	↑

Figure 4. Setting Output Compare Flag/Pin for ATmega48

TCNTn	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4
Pin/Flag	↑

OCR1x buffering in PWM Mode

As described in the data sheet, the OCR1x Registers are updated at the top value when written. Thus, when writing the OCR1x in PWM mode, the value is stored in a temporary buffer. When the Timer/Counter1 reaches the top, the temporary buffer is transferred to the actual Output Compare Register. If PWM mode is left after the temporary buffer is written, but before the actual Output Compare Register is updated, the behavior differs between ATmega48 and AT90S4433.

ATmega48

If the OCR1x Register is read before the update is done, the actual compare value is read, not the temporary OCR1 buffer.

AT90S4433

If the OCR1A Register is read before the update is done, the value in the OCR1A buffer is read. For example, the value read is the one last written (to the OCR1A buffer), but since the Timer/Counter never reached the top value, it was not latched into the OCR1A Register. Hence, the value that is used for comparison is not necessarily the same as being read.

Note: This applies to 16-bit Timer/Counter only. For 8-bit Timer/Counter2 in ATmega48, the temporary buffer is read.

Memory of previous OCnx pin level

In AT90S4433, there are two settings of COMnx1:0 that do not update the OCnx pin in PWM mode (0b00 and 0b01), and one setting of COMnx1:0 in non-PWM mode (0b00). Assume the Timer/Counter is taken from a state that updates the OCnx pin to a state that does not, and then back again to a state that does update the OCnx pin. The following differences should be noted:

ATmega48

The level of the OCnx pin before disabling the Output Compare mode is remembered. Re-enabling the Output Compare mode will cause the OCnx pin to resume operation from the state it had when it was disabled. All Output Compare pins are initialized to zero on Reset.

AT90S4433

For Timer/Counter1 in non-PWM mode, a compare match during the time when the Timer/Counter is not connected to the pin will reset the OC1 pin to the low level once enabled again. PWM mode will update the Internal Register for the OC1 pin, such that the state of the pin is unknown once enabled again.

UART replaced by USART

The UART in AT90S4433 has been replaced by a USART in ATmega48. The ATmega48 USART is compatible with the AT90S4433 UART with one exception: The two-level Receive Register acts as a FIFO. The following must be kept in mind:

- A second buffer register has been added. The two buffer registers operate as a circular FIFO buffer. Therefore the UDR must only be read once for each incoming data. More important is the fact that the Error Flags (FE and DOR) and the 9th data bit (RXB8) are buffered with the data in the receive buffer. Therefore the status bits must always be read before the UDR Register is read. Otherwise the error status will be lost since the buffer state is lost.
- The Receiver Shift Register can now act as a third buffer level. This is done by allowing the received data to remain in the Serial Shift Register if the buffer registers are full, until a new start bit is detected. The USART is therefore more resistant to Data OverRun (DOR) error conditions.

Another minor difference is the initial value of RXB8, which is “1” in the UART in AT90S4433 and “0” in the USART in ATmega48.

Watchdog Timer

The ATmega48 has the Enhanced Watchdog Timer (WDT) and is improved compared to the one in AT90S4433.

If the operating voltage is 5V and the WDTON fuse is left unprogrammed, the WDT will behave similar on AT90S4433 and ATmega48.

The frequency of the Watchdog Oscillator in ATmega48 is approximately128kHz for all supply voltages. The typical frequency of the Watchdog Oscillator in AT90S4433 is close to 1.0 MHz at 5V, but the Time-out period increases with decreasing V_{CC}. This means that the selection of Time-out period for the Watchdog Timer (in terms of number of WDT Oscillator cycles) must be reconsidered when porting the design to ATmega48.

If the WDT is not used, it is still recommended to disable it initially in the application code to clear unintentional WDT enabled events.

ADC

The ADCBG bit in the ADMUX register in AT90S4433 selects a bandgap reference as input to the ADC. The same thing is obtained in ATmega48 by setting the MUX3..0 bits to 1110. The ADMUX registers are therefore not directly compatible. The REFS1..0 bits in ATmega48 replaces the bit position for ADCBG and an unused position in AT90S4433. These bits determine the reference voltage, and have nothing to do with the input to the ADC.

Note: The internal bandgap reference voltage is typically 1.22V for AT90S4433 and 1.1V for ATmega48.

EEPROM

Be aware that EEPROM write access must be completed before entering Power Down sleep mode. Otherwise the system oscillator will continue to run, drawing additional current.

In AT90S4433, the EEPROM write time is dependent on supply voltage, typically 2.5ms @ V_{CC} = 5V and 4ms @ V_{CC} = 2.7V. In ATmega48, the EEPROM write time takes typically 3.4ms, independent of supply voltage. ATmega48 also has the ability to split EEPROM access into separate erase and write operations, but the EECR register is backwards compatible with AT90S4433 code.

Oscillators and Start-up Times

ATmega48 provides more Oscillator and Start-up Time selections than AT90S4433. During wake-up from Power-down mode, the ATmega48 uses the CPU frequency to determine the duration of the wake-up delay, while AT90S4433 determines the delay from the WDTR Oscillator frequency.

The Crystal Oscillator in AT90S4433 is capable of driving an additional clock buffer from the XTAL2 output. In ATmega48, this is only possible when the Full Swing Crystal Oscillator clock option is selected (CKSEL = 011x). In this mode the oscillator has a rail-to-rail swing at the output, but at the expense of higher power consumption. Hence, do only program this fuse when rail-to-rail swing is required. When using the Low Power Crystal Oscillator clock option (CKSEL = 1xxx), the CKSEL1 and CKSEL2 bits select the frequency range. Refer to the datasheets for details. Table 3 below shows the CKSEL settings for AT90S4433 and the closest matching equivalents for ATmega48.

Table 3. CKSEL and SUT closest matching settings.

AT90S4433			**ATmega48**			**Comment**
Start-up time from sleep mode	**Additional delay from Reset**	**CKSEL fuse settings**	**Start-up time from sleep mode**	**Additional delay from Reset**	**CKSEL/SUT fuse settings**	
6 CK	4 ms	000	6 CK	4.1ms + 14CK	0000/01	Ext. clock
6 CK	-	001	6 CK	14CK	0000/00	Ext. clock w/BOD
16k CK	64 ms	010	16k CK	65ms + 14CK	xxx1/11	Crystal
16k CK	4 ms	011	16k CK	4.1ms + 14CK	xxx1/10	Crystal, fast rising power
16k CK	-	100	16k CK	14CK	xxx1/01	Crystal w/BOD
1k CK	64 ms	101	1k CK	65ms + 14CK	xxx1/00	Resonator
1k CK	4 ms	110	1k CK	4.1ms + 14CK	xxx0/11	Resonator, fast rising power
1k CK	-	111	1k CK	14CK	xxx0/10	Resonator w/BOD

Brown-out Detector

In AT90S4433, the BODEN fuse enables the Brown-out Detector and the BODLEVEL fuse selects between 2.7V and 4.0V. In ATmega48, the BODLEVEL2..0 fuses controls the BOD, which also has more detection levels than the AT90S4433 BOD. Refer to the ATmega48 datasheet for details on how to configure the BOD.

Programming Interface

Both the serial and parallel programming interface and algorithms has been changed in ATmega48. Refer to the datasheets for details. However, this should not cause any trouble when STK500 is used and ATmega48 is selected.

Note: AT90S4433 signature: 0x1E 0x92 0x03
ATmega48 signature: 0x1E 0x92 0x05

Operating Voltage Ranges

AT90S4433 can operate from 2.7V to 6.0V.

ATmega48 can operate from 1.8V to 5.5V.

Electrical Characteristics

The ATmega48 is produced in a different process than the AT90S4433 and electrical characteristics will differ between these devices. Please consult the datasheets for details on electrical characteristics.

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
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