Embedded Processors and DSP Selection Guide

2008 Edition

ANALOG DEVICES BLACKfin®

ANALOG DEVICES SHARC®

ANALOG DEVICES TigerSHARC®

www.analog.com/processors

ANALOG DEVICES

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   Technical Documentation for Embedded Processors in Japanese can be found at *www.analog.com/processors/Japan/index.html* and *www.analog.com/processors/japan/technicalSupport/technicalLibrary*.
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In the United States and Canada, please call 800.ANALOGD (262.5643). For price, delivery, and samples, select option 3. For literature, select option 2.

Contact Embedded Processing and DSP Support via email at *processor.support@analog.com*.

Contact CROSSCORE Development Tools Support via email at *processor.tools.support@analog.com*.

In China, contact Embedded Processing and DSP Support via email at *processor.china@analog.com*.

In Japan, visit *www.analog.com/jp/contact* for the respective contact number or input all inquiries in Japanese to *forms.analog.com/Form_Pages/support/dsp/dspSupport.asp*.

In Europe and Israel, contact Embedded Processing and DSP Support via email at *processor.europe@analog.com*, telephone 49.89.76903.333 or fax 49.89.76903.157.

Contents

ADI Embedded Processors Portfolio

Analog Devices embedded architectures feature simple yet powerful programming models and are supported by high quality development tools.

Blackfin® Processors

High Performance, Low Power Processing

Blackfin Processors embody a new breed of embedded processors designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. Blackfin Processors deliver breakthrough signal processing performance and power efficiency with a RISC programming model. Blackfin Processors present high performance, homogeneous software targets that allow flexible resource allocation between hard real-time DSP tasks and nonreal-time control tasks. System control tasks can often run in the shadow of DSP and video tasks.

Blackfin Processors are ideal for:

- Portable and networked digital media appliances
- Consumer communications and networks
- Automotive telematics, safety driver assistant, and infotainment
- Industrial instrumentation and medical equipment

TigerSHARC® Processors

Highest Performance Multiprocessor Systems

The TigerSHARC Processor family offers the industry's highest performance per watt and per square inch of board space for the most demanding signal and image processing applications. Its patented link port technology allows glueless interprocessor communication within arrays of two or more TigerSHARC Processors, delivering unbounded performance in terms of MMACS and MFLOPS.

Based on a 128-bit static superscalar architecture, TigerSHARC Processors offer native support of fixed- and floating-point data types and a balanced combination of computational performance, I/O bandwidth, and memory integration. Together, this yields sustained DSP system-level performance that is two to four times greater than conventional DSPs or microprocessors with vector processing units.

By providing native support for 1-bit data formats used for chip-rate processing, TigerSHARC Processors pioneer a new class of software-defined radios and serve applications that were previously the exclusive domain of expensive ASICs (application-specific integrated circuits) and FPGAs (field-programmable gate arrays). In addition, by moving to a software-centric design model, TigerSHARC Processors allow IP reuse, which greatly enhances R&D productivity throughout each successive product generation.

TigerSHARC Processors are ideal for:

- Wireless infrastructure WiMAX applications such as 802.16 and other advanced standards (e.g., OFDM), base stations, and software-defined radios
- Floating point, performance density related systems in both the single and multiprocessor environments
  - Medical imaging equipment (e.g., CAT scan, ultrasound, and MRI)
  - Military equipment (e.g., radar/sonar, munitions targeting, and optoelectronics)
  - Industrial and instrumentation equipment
  - Automated test equipment

SHARC® Processors

Leadership in Floating-Point Applications

SHARC Processors offer exceptionally high floating-point DSP performance while integrating application-specific peripherals and interfaces designed to minimize overall system costs. The completely code-compatible family portfolio extends from entry-level products that are priced under $10 to high-end products providing 400 MHz/2.4 GFLOPS of signal processing performance. The broad range of price and performance points available in the SHARC Processor family makes its members particularly well-suited to applications ranging from consumer, automotive, and professional audio to industrial and medical applications.

All SHARC Processors are based on a 32-bit Super Harvard Architecture that combines a high performance signal processing core with sophisticated memory and I/O processing subsystems. This balanced architecture enables unparalleled performance while ensuring that sufficient memory and I/O bandwidth are available for the most algorithmically challenging applications. In addition to these hardware-centric efficiencies, all SHARC Processors offer a very flexible algorithm development environment by supporting a variety of fixed- and floating-point data types.

SHARC Processors are ideal for:

- Home theater audio systems
- Professional audio systems
- Automotive audio systems
- Industrial and instrumentation equipment
- Medical imaging
- Telephony

Markets and Applications

Market	Applications	Architecture/ Platform
Communications		
Broadband	Broadband Over Power Lines	Blackfin
	Digital Media Gateways (VOD)	Blackfin
	Home Networking	Blackfin
	IP PBX	Blackfin
	IP Set-Top Box	Blackfin
	Media Node	Blackfin
	Multimedia Over IP	Blackfin
	Video Conferencing/Phone	Blackfin
	Video Surveillance/Security	Blackfin
	Voice Over IP	Blackfin
Wireless	Access (Broadband) (i.e., 802.16 ...)	Blackfin, TigerSHARC
	Base Station	TigerSHARC
	Cellular Location	Blackfin
	Satellite Phone	Blackfin
Automotive		
In Cabin	Audio Amplifier	SHARC
	Audio Jukebox	Blackfin
	Digital Radio	Blackfin
	Driver Assistance	Blackfin
	Handsfree	Blackfin
	Head Unit	Blackfin, SHARC
	Multimedia Device Interface	Blackfin
	Navigation	Blackfin
	Occupancy/Classifications	Blackfin
	Premium Audio System	SHARC
	Rear Seat Audio/Video	Blackfin
Consumer		
Security	Biometrics	Blackfin, SHARC
	Video Surveillance	Blackfin
Entertainment	Digital Home Video Appliance	Blackfin
	Digital Network Media Devices	Blackfin
	Digital Radio	Blackfin
	Digital Still Camera	Blackfin
	Digital TV (Audio)	Blackfin, SHARC
	Digital Video Camera	Blackfin
	Digital Video Recorder	Blackfin
	DVD/HD DVD/Blu-ray	SHARC
	Home Server	Blackfin, SHARC
	Home Theater A/V Receiver	SHARC
	Wireless Headphones/Headsets	Blackfin
	IP Set-Top Box	Blackfin
	Networked A/V Receiver	Blackfin
	Portable Media Player/ Portable Entertainment Console	Blackfin
	Multimedia Accessories	Blackfin
	Professional Audio/Broadcast	SHARC
	Prosumer Audio	SHARC
	Satellite Radio	Blackfin
Toys	Interactive Toys	Blackfin
	Video Game Console	Blackfin

Market	Applications	Architecture/ Platform
Industrial and Instrumentation		
Medical	CT	Blackfin, SHARC, TigerSHARC
	Diagnostic	Blackfin, SHARC, TigerSHARC
	MRI	SHARC, TigerSHARC
	Patient Monitoring	Blackfin, SHARC, TigerSHARC
	Portable Medical	Blackfin, SHARC
	Ultrasound	Blackfin, SHARC, TigerSHARC
	X-Ray	SHARC, TigerSHARC
Point of Sale	Scanner	Blackfin
	Vending Machine	Blackfin
Test/Measurement Equipment	ATE	Blackfin, SHARC, TigerSHARC
	Communications	Blackfin, SHARC, TigerSHARC
	Measurement	Blackfin, SHARC, TigerSHARC
Industrial	Data Acquisition	Blackfin, SHARC
	Factory Automation	Blackfin
	Industrial Control	Blackfin, SHARC, TigerSHARC
	Machine Control	Blackfin
	Metering	Blackfin
	Motor Control	Blackfin
	Network Management	Blackfin
	Power Control	Blackfin
	Robotics	Blackfin, SHARC, TigerSHARC
	Verification and Biometrics	Blackfin
	Video Surveillance Systems	Blackfin
	Vision Systems	Blackfin
Military/Aerospace		
Guidance	Radar	SHARC, TigerSHARC
	Sonar	SHARC, TigerSHARC
Aerospace	Control	Blackfin
	Entertainment	Blackfin
Military	Avionics	Blackfin, SHARC, TigerSHARC
	Communications	Blackfin, TigerSHARC
	Digital Radio	Blackfin, SHARC, TigerSHARC
	Location	Blackfin, TigerSHARC
	Military Imaging	TigerSHARC
	Radar/Sonar	SHARC, TigerSHARC
	Smart Munitions	TigerSHARC
	Target Detection	TigerSHARC

Key Products

Blackfin Processors

Generic	Max (MHz)	Max (MMACS)	L1 Memory (kB)	L2 Memory (Bytes)	External I/O Voltage (V)	Package	Price Range @ 1k ($U.S.)[1]	Status
ADSP-BF522	400	800	132	—	1.8, 2.5, 3.3	289-CSP_BGA, 208-CSP_BGA	Contact ADI	Contact ADI
ADSP-BF522C	400	800	132	—	1.8, 2.5, 3.3	289-CSP_BGA	Contact ADI	Contact ADI
ADSP-BF523	600	1200	132	—	1.8, 2.5, 3.3	289-CSP_BGA, 208-CSP_BGA	Contact ADI	Contact ADI
ADSP-BF523C	600	1200	132	—	1.8, 2.5, 3.3	289-CSP_BGA	Contact ADI	Contact ADI
ADSP-BF524	400	800	132	—	1.8, 2.5, 3.3	289-CSP_BGA, 208-CSP_BGA	Contact ADI	Contact ADI
ADSP-BF524C	400	800	132	—	1.8, 2.5, 3.3	289-CSP_BGA	Contact ADI	Contact ADI
ADSP-BF525	600	1200	132	—	1.8, 2.5, 3.3	289-CSP_BGA, 208-CSP_BGA	Contact ADI	Contact ADI
ADSP-BF525C	600	1200	132	—	1.8, 2.5, 3.3	289-CSP_BGA	Contact ADI	Contact ADI
ADSP-BF526	400	800	132	—	1.8, 2.5, 3.3	289-CSP_BGA, 208-CSP_BGA	Contact ADI	Spring 2008
ADSP-BF526C	400	800	132	—	1.8, 2.5, 3.3	289-CSP_BGA	Contact ADI	Spring 2008
ADSP-BF527	600	1200	132	—	1.8, 2.5, 3.3	289-CSP_BGA, 208-CSP_BGA	Contact ADI	X-Grade Samples
ADSP-BF527C	600	1200	132	—	1.8, 2.5, 3.3	289-CSP_BGA	Contact ADI	X-Grade Samples
ADSP-BF531	400	800	52	—	1.8, 2.5, 3.3	169-PBGA, 160-CSP_BGA, 176-LQFP	8.79 to 13.93	Released
ADSP-BF532	400	800	84	—	1.8, 2.5, 3.3	169-PBGA, 160-CSP_BGA, 176-LQFP	9.22 to 14.33	Released
ADSP-BF533	750	1500	148	—	1.8, 2.5, 3.3	169-PBGA, 160-CSP_BGA	12.05 to 21.95	Released
ADSP-BF534	500	1000	132	—	1.8, 2.5, 3.3	182-CSP_BGA, 208 Sparse CSP_BGA	12.25 to 16.73	Released
ADSP-BF535	350	700	52	256k	3.3	260-PBGA	30.00 to 45.38	Released
ADSP-BF536	400	800	100	—	2.5, 3.3	182-CSP_BGA, 208 Sparse CSP_BGA	9.95 to 14.25	Released
ADSP-BF537	600	1200	132	—	2.5, 3.3	182-CSP_BGA, 208 Sparse CSP_BGA	16.95 to 20.95	Released
ADSP-BF538/ ADSP-BF538F	533	1066	148	—	3.3	316-CSP_BGA	15.84 to 20.42	Sampling
ADSP-BF542	600	1200	132	—	2.5, 3.3	400-CSP_BGA	Contact ADI	Sampling
ADSP-BF544	533	1066	132	64k	2.5, 3.3	400-CSP_BGA	Contact ADI	Sampling
ADSP-BF547	600	1200	132	128k	2.5, 3.3	400-CSP_BGA	Contact ADI	Engineering Samples
ADSP-BF548	600	1200	132	128k	2.5, 3.3	400-CSP_BGA	Contact ADI	Sampling
ADSP-BF549	533	1066	132	128k	2.5, 3.3	400-CSP_BGA	Contact ADI	Sampling
Dual Core								
ADSP-BF561	600[2]	1200	200	128k	1.8, 2.5, 3.3	256-CSP_BGA, 297-PBGA	24.90 to 35.32	Released

NOTES

[1]Products in U.S. dollars. Lowest speed/temperature grade suggested resale price per unit in 1000 unit quantities. All pricing is budgetary and subject to change. Please contact your local ADI sales representative or distributor for more information.

[2]Per core.

Packages: PBGA = Plastic Ball Grid Array
LQFP = Low-Profile Quad Flat Pack
CSP_BGA = Chip Scale Package Ball Grid Array

Key Products

SHARC Processors

32-Bit Generic	MMACS/ MFLOPS	On-Chip Memory SRAM/ROM (Mb)	External I/O Voltage (V)	Package	Price Range @ 1k ($U.S.)[1]	Status
ADSP-21065L	66/198	0.5/—	3.3	208-MQFP/196-CSP_BGA	22.58 to 65.84	Released
ADSP-21160M	160/480	4/—	3.3	400-PBGA	167.48 to 184.22	Released
ADSP-21160N	200/600	4/—	3.3	400-PBGA	167.48 to 196.93	Released
ADSP-21161N	200/600	1/—	3.3	225-CSP_BGA	25.86 to 34.13	Released
ADSP-21261	300/900	1/2	3.3	144-LQFP/136-CSP_BGA	7.22 to 12.32	Released
ADSP-21262	400/1200	2/4	3.3	144-LQFP/136-CSP_BGA	16.95 to 23.85	Released
ADSP-21266[2]	400/1200	2/4	3.3	144-LQFP/136-CSP_BGA	14.24 to 17.80	Released
ADSP-21362[2]	666/1998	3/4	3.3	144-LQFP E_Pad/ 136-CSP_BGA	26.80 to 32.16	Released
ADSP-21363	666/1998	3/4	3.3	144-LQFP E_Pad/ 136-CSP_BGA	19.98 to 28.78	Released
ADSP-21364	666/1998	3/4	3.3	144-LQFP E_Pad/ 136-CSP_BGA	29.40 to 42.34	Released
ADSP-21365[2]	666/1998	3/4	3.3	144-LQFP E_Pad/ 136-CSP_BGA	28.21 to 33.85	Released
ADSP-21366[2]	666/1998	3/4	3.3	144-LQFP E_Pad/ 136-CSP_BGA	22.33 to 32.16	Released
ADSP-21367[2]	800/2400	2/6	3.3[3]	208-MQFP/256-SBGA	20.48 to 37.54	Released
ADSP-21368	800/2400	2/6	3.3[3]	256-SBGA	30.67 to 44.99	Released
ADSP-21369	800/2400	2/6	3.3[3]	208-MQFP/256-SBGA	19.46 to 35.67	Released
ADSP-21371	532/1596	1/4	3.3	208 LQFP E_Pad	13.11 to 15.73	Released
ADSP-21375	532/1596	0.5/2	3.3	208 LQFP E_Pad	9.71 to 11.65	Released

NOTES
[1]Products in U.S. dollars. Lowest speed/temperature grade suggested resale price per unit in 1000 unit quantities. All pricing is budgetary and subject to change. Please contact your local ADI sales representative or distributor for more information.
[2]Requires IP licensing prior to shipment. See individual product pages for details.
[3]1.2 V operation for 266 MHz speed grade.

Packages: SBGA = Thermally Enhanced BGA
PBGA = Plastic Ball Grid Array
LQFP = Low-Profile Quad Flat Pack
MQFP = Metric Quad Flat Pack
CSP_BGA = Chip Scale Package Ball Grid Array

TigerSHARC Processors

32-Bit Generic	Max (MHz)	Max (MMACS)	On-Chip Memory (Mb)	External I/O Voltage (V)	Package	Price Range @ 1k ($U.S.)[1]	Status
ADSP-TS101S	300	2100	6	3.3	625-PBGA, 484-PBGA	186.00 to 244.20	Released
ADSP-TS201S	600	4800	24	2.5	576-PBGA	242.00 to 319.44	Released
ADSP-TS202S	500	4000	12	2.5	576-PBGA	201.00 to 221.10	Released
ADSP-TS203S	500	4000	4	2.5	576-PBGA	177.00 to 194.70	Released

NOTES
[1]Products in U.S. dollars. Lowest grade suggested resale price per unit in 1000 unit quantities. All pricing is budgetary and subject to change. Please contact your local ADI sales representative or distributor for more information.

Packages: PBGA = Plastic Ball Grid Array

Technical Workshops and University Program

Technical Workshops

Cut your time to market by getting up to speed fast. The Embedded Processing and DSP system development and programming workshops provide comprehensive hands-on training on Analog Devices embedded processors and DSPs. The workshops are geared toward people who have a working knowledge of microprocessors and want to learn how to use Analog Devices embedded processors and DSPs. These courses cover the DSP architecture, assembly language syntax, I/O interface, hardware, and software development tools. Throughout the workshop, attendees learn how easy it is to use Analog Devices embedded processors and DSPs from lecture sessions and hands-on exercises.

1-Day Workshops and Seminars

Workshops and seminars for those who want to evaluate the capabilities of ADI's high performance embedded processors and development tools. Practical issues and concerns will be addressed in addition to the strengths and power of these devices.

Multiday Workshops

In-depth technical training designed to develop a strong working knowledge of embedded processors and development tools through lecture and hands-on exercises. Workshops are typically 3.5 days and presented by Kaztek Engineering's ADI-trained instructors.

μClinux on the Blackfin Processor 4-Day Workshop

Designed to be a complete introduction to all aspects of programming with μClinux based on the Blackfin Stamp board.

University Workshops

These workshops are presented by ADI's worldwide university network and are taught by local university professors who are supported by Analog Devices embedded processor and DSP application teams.

Embedded Processing and DSP International Workshops

Analog Devices sponsors embedded processing and DSP workshops throughout Europe.

For more information and schedules, visit *www.analog.com/processors/workshops*.

ADI Embedded Processing and DSP University Program

The Analog Devices DSP University Program promotes embedded and digital signal processing education and research at engineering institutions worldwide. It provides the next generation of engineers with embedded processing and DSP knowledge to help them compete in the industry of tomorrow.

Benefits of the ADI DSP University Program:

- Lab recommendations

  Complete software and hardware tools to set up an embedded processor or DSP lab

- Discounts on development tools

  Discounts of up to 90% on hardware and software development tools

- Teaching resources

  Sample lectures and labs

- Discounts on ADI Embedded Processor and DSP workshops

  In-depth, hands-on, 3.5-day training sessions

Analog Devices Technologies Are Ideally Suited for Teaching:

- Embedded processor and DSP architectures that are the simplest in the industry to program
- Simple instruction sets
- High level of SRAM integration

To learn more about the program and available discounts, visit *www.analog.com/processors/university*.

Online Training

Blackfin Online Learning and Development

Master the incredible potential of the Blackfin Processor and build better applications. Discover how without ever leaving your desk by taking one of the new Blackfin online training modules.

The modules cover a wide range of topics that address different stages of your development cycle—from the fundamentals of Analog Devices' development tools to tips on how developers can optimize their system performance. These modules are designed to be used independently or in combination, depending on the experience and interest of the viewer.

Course Name: Blackfin Core Architecture

This module introduces the Blackfin family, which includes the Blackfin Processors, tools, and other development support that is available.

Course Name: Lockbox Secure Technology on Blackfin Processors

This module focuses on the highlights of Lockbox technology on Blackfin Processors.

Course Name: Blackfin Optimizations for Performance and Power Consumption

This module is about optimizing your software design for the Blackfin Processor for better performance and lower power consumption.

Course Name: Introduction to LabVIEW Embedded Module for ADI Blackfin

Through numerous demonstrations, this course provides an introduction to the LabVIEW embedded module for the Blackfin development environment. Starting with simple application examples this course covers building, downloading, and running virtual instruments on the Blackfin Processor as well as peripheral control, application tuning using background telemetry channels and seamless debugging support through the VisualDSP++ development environment.

Course Name: Introduction to VisualDSP++ Tools

This module will give the user an overview of the VisualDSP++ Tools. For demonstration purposes, the ADSP-BF537 EZ-KIT Lite will be used as the target. Users will learn some quick tips on how to analyze and fine tune their applications.

Course Name: Programming and Optimizing C Code on Blackfin Processors

This module introduces concepts, tools, and approaches to optimizing Blackfin C applications. It highlights the problems and opportunities that can lead to potential performance improvements and review the available tools/techniques. The module covers a wide range from automatic optimization to detailed rewriting of C expressions.

Course Name: Blackfin System Services

This module discusses the System Services software available for Blackfin Processors. It is recommended that users have some understanding of the Blackfin architecture, basic knowledge of software terminology, and experience in embedded systems.

Course Name: Performance Tuning on the Blackfin Processor

This module discusses the techniques users can use to tune system performance for Blackfin Processors. Users should have some understanding of the Blackfin architecture, a basic knowledge of software terminology, and experience in embedded systems.

Course Name: Basics of Building a Blackfin Application

This module describes the basic software build process of VisualDSP++, specific Blackfin programming "gotchas," and basic code optimization strategies. Users will see an example demonstrating "Zero Effort" Optimization by using built-in Optimizer and Cache.

Course Name: Blackfin Device Drivers

This module discusses the device driver model for the Blackfin family of processors. It is recommended that users should have an understanding of the Blackfin architecture and are familiar with the Blackfin System Services software.

Course Name: Interfacing Blackfin with Audio and Video Peripherals

This module will familiarize the user with the principles behind connecting Blackfin Processors to audio and video devices. It is recommended that users have some basic working knowledge of audio and video fundamentals.

Course Name: Rapid Development of a Blackfin-Based Video Application

This module discusses the rapid development process of a Blackfin video application using readily available and fully supported software and hardware modules. It is recommended that users understand the basic knowledge of software terminology, have experience in embedded systems and understand Blackfin Systems Services and Device Drivers.

Course Name: Introduction to VDK

This 27 minute module provides an overview of the VisualDSP++ Kernel. A demonstration shows the basics of building and debugging VDK projects. Users should have previous experience with operating systems as well as a basic knowledge of software terminology.

Online Training

Blackfin Online Learning and Development

Course Name: Multimedia Starter Kit

This 52 minute module introduces the Multimedia Starter Kit. A demonstration covers JPEG and MJPEG. Users should have previous experience with embedded systems, basic knowledge of software terminology, and familiarity with VisualDSP++, Blackfin Processors, and ADI evaluation boards.

Course Name: Introduction to VisualAudio®

This 35 minute module provides an overview of VisualAudio, a tool for rapid development of audio processing software. A demonstration shows how to design audio processing layouts using the graphical editor. Users should have some experience with embedded processing, audio, Blackfin Processors, and VisualDSP++.

Course Name: Advanced VisualAudio

This 27 minute module provides advanced training on VisualAudio: high and low level variables, expression language, presets, use with applications like MATLAB. Users should be audio algorithm developers comfortable writing C code, familiar with Blackfin Processors and VisualDSP++.

New modules are in development. To see the latest modules available or take a training module, visit
www.analog.com/BOLD.

Development Tools: CROSSCORE

Analog Devices CROSSCORE® development tools are focused on providing easier and more robust methods for engineers to develop and optimize systems by shortening product development cycles to reduce time to market.

- VisualDSP++® development environment
- EZ-KIT Lite® evaluation kits
- EZ-Extender® daughter boards
- Emulators

VisualDSP++ Integrated Development Environment

VisualDSP++ is an easy-to-install, easy to use, integrated software development and debugging environment (IDDE). More in-depth information is available on Page 9.

EZ-KIT Lite Evaluation Kit

These systems consist of a standalone evaluation board and an evaluation suite of VisualDSP++ to facilitate architecture evaluations via a PC-hosted tool set. Users can evaluate ADI's processors, learn about digital signal processing applications, as well as simulate, debug, and prototype applications.

EZ-Extender Daughter Boards

EZ-Extender daughter boards give developers access to and the ability to connect to various peripherals from Analog Devices and third parties via the expansion interface of the EZ-KIT Lite evaluation kits.

Blackfin EZ-Extender[1]

Expands the capabilities of the evaluation system by providing a connection between the Parallel Peripheral Interface (PPI) of the ADSP-BF533 processor (the PPI0 and PPI1 interfaces of the ADSP-BF561 processor), an Analog Devices high speed converter (HSC) evaluation board, a camera evaluation board, and an LCD display device. Moreover, the extender broadens the range of the EZ-KIT Lite applications by providing surface-mounted (SMT) footprints for breadboard capabilities and access to all of the pins on the EZ-KIT Lite's expansion interface.

Blackfin A-V EZ-Extender[2]

Expands the capabilities of the evaluation system by providing a connection to a video decoder, a video encoder, multiple camera evaluation boards, a flat panel display, and a 3-stereo input channel, 2-stereo output channel audio codec.

Blackfin FPGA EZ-Extender[2]

Expands the capabilities of the evaluation system by providing a Xilinx FPGA with external memory, IDC connectors for off-board connections, and a small breadboard area.

Blackfin Audio EZ-Extender[2]

The Blackfin Audio EZ-Extender expands the capabilities of the evaluation system by providing an interface for eight channels of analog audio input and 16 channels of analog audio output along with an interface to digital audio I/O through a Sony/Philips Digital Interface (S/PDIF) transceiver.

Blackfin USB-LAN EZ-Extender[2]

Expands the capabilities of the evaluation system by providing a connection between the Asynchronous Memory Bus of the Blackfin Processor (Asynchronous Memory Bank 3) and either a USB 2.0 or a 10/100 Mbps Ethernet device.

SHARC EZ-Extender[3]

Expands the capabilities of the evaluation system by providing a connection between the Parallel Data Access Port (PDAP) of the ADSP-21262 processor and an Analog Devices analog-to-digital high-speed converter (ADC HSC) evaluation board. Moreover, the extender broadens the range of the EZ-KIT Lite applications by providing surface mounted (SMT) footprints for breadboard capabilities and access to all of the pins on the EZ-KIT Lite's expansion interface.

SHARC USB EZ-Extender[4]

Expands the capabilities of the evaluation system by providing a connection between the parallel port or asynchronous memory bus of the SHARC Processor and a USB 2.0 device.

USB-Based Emulators

Analog Devices' cost-effective Universal Serial Bus (USB)-based emulator and high performance (HP) Universal Serial Bus (USB)-based emulator each provide an easy, portable, nonintrusive, target-based debugging solution for Analog Devices JTAG processors and DSPs. These powerful USB-based emulators perform a wide range of emulation functions, including single-step and full speed execution with predefined breakpoints, and viewing and/or altering of register and memory contents.

[1]Daughter board for ADSP-BF533 EZ-KIT Lite and ADSP-BF561 EZ-KIT Lite only (sold separately).

[2]Daughter board for ADSP-BF533 EZ-KIT Lite, ADSP-BF537 EZ-KIT Lite, ADSP-BF538 EZ-KIT Lite, and ADSP-BF561 EZ-KIT Lite only (sold separately).

[3]SHARC EZ-Extender daughter board available for ADSP-21262 EZ-KIT Lite only (sold separately).

[4]SHARC USB EZ-Extender daughter board available for ADSP-21262 EZ-KIT Lite, ADSP-21364 EZ-KIT Lite, and ADSP-21369 EZ-KIT Lite only (sold separately).

VisualDSP++
Integrated Development Environment

Key Features

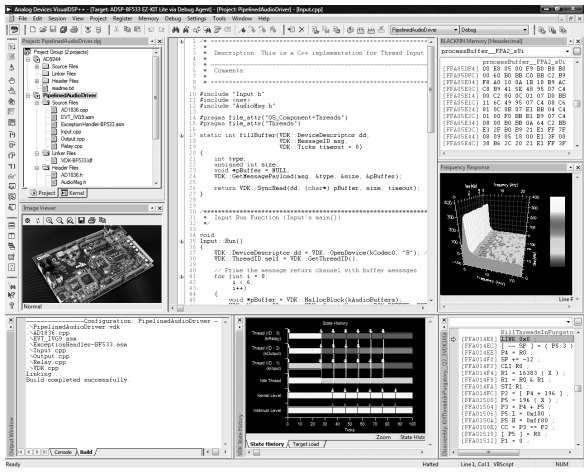
Integrated Development and Debugging Environment
- Supports all Analog Devices processors and DSPs
- Multiple project management
- Profiling and tracing of instruction execution
- Automation API and Automation Aware Scripting Engine
- Multiple processor support
- Background Telemetry Channel (BTC) support with data streaming capability
- Statistical profiling
- Graphical plotting capabilities
- Cache visualization
- Execution pipeline viewer
- Compiled simulation

Efficient Application Code Generation
- Native C/C++ compiler and enhanced assembler
- Profile Guided Optimization (PGO)
- Expert linker with profiling capability
- Integrated source code control
- TCP/IP and USP support for Blackfin Processors
- Processor configuration/start-up code wizard for Blackfin Processors
- VisualDSP++ Kernel (VDK) with multiprocessor messaging capability
- System services and device driver support for Blackfin Processors
- File system support for Blackfin Processors

Platform and Processor Support
VisualDSP++ release 5.0 supports Analog Devices' Blackfin Processor, TigerSHARC Processor, and SHARC Processor families. Windows® XP, Windows 2000, and Windows Vista® hosts are supported.

Description	Part Number
VisualDSP++ Test Drive 90-day free trial	VDSP-BLKFN-PC-TEST
	VDSP-TS-PC-TEST
	VDSP-SHARC-PC-TEST

VisualDSP++ Development and Debugging Environment
VisualDSP++ is a state-of-the-art software development environment targeting the Analog Devices embedded processor portfolio. With the embedded software engineer and signal-processing-intensive applications specifically in mind, VisualDSP++, coupled with Analog Devices in-circuit emulator (ICE) and EZ-KIT Lite evaluation products, provide best-in-class capabilities for developing demanding real-time applications.



VisualDSP++ interface.

Develop High Performance Applications Quickly
At the heart of VisualDSP++ is a robust and powerful C/C++ compiler. The compiler consistently delivers industry-leading performance on standard benchmarks, ensuring that all but the most performance-demanding applications can be written entirely in the C language, accelerating development time while maintaining a portable code base. The compiler is backed by a rich library of signal-processing routines, allowing easy access to hand-coded, optimized implementations of FFTs, FIRs, etc. The Blackfin and SHARC compilers support MISRA-C:2004, for safety-critical embedded systems (*www.misra-c.com*).

The ANSI-C compiler is also augmented with popular language extensions and enhancements to make it more amiable to existing code bases. Examples include GNU GCC extensions, ETSI fractional libraries, and multiple heap support.

A compiler's first job is to produce correct code, so there are occasions when the compiler must take a conservative approach to a code sequence when a more aggressive approach should have been taken if certain constraints are guaranteed by the programmer. The VisualDSP++ compiler supports a broad range of pragma that allow the programmer to better exploit the compiler while maintaining C language neutrality. Just as important, the compiler has the ability to feed back advisory information to the programmer, offering further improvements to a code sequence should the programmer be able to make certain guarantees about it. This information is displayed seamlessly in the VisualDSP++ main editor window. This "lifts the veil" off the "black box" that compilers are often, and accurately, accused of being.

VisualDSP++

Integrated Development Environment


```
#include <fract.h>
fract32 sp (fract16* a, fract16* b)
{
    int i;
    fract32 sum = 0;

    #pragma all_aligned
    for ( i = 0; i < 100; ++i )
    {
[Info] This loop executes 2 iterations of the original loop in estimated 1 cycles.
[Info] Loop was vectorized by a factor of 2
[Advice] Consider using pragma extra_loop_loads for this loop.
                                                        b[i] )
    }

    return sum;
}
```

Backing the compiler is a powerful assembler and linker technology. Analog Devices' processors are noted for their intuitive algebraic assembly language syntax, and the VisualDSP++ assembler extends that ease of use with the ability to import C header files, allowing for symbolic references into arbitrarily complex C data structures. Binary data can be "#included" directly into assembly source files, creating an easy way to add blocks of static data (such as audio samples and bitmaps) to an application. The VisualDSP++ linker is fully multicore and multiprocessor (MP) aware, allowing for the creation of cross-linked multi-executable applications in a single pass. Other powerful capabilities of the linker include dead code and data elimination, code and data overlays, section spilling (i.e., automatic overflow from internal to external memory), and automatic short-to-long call expansion.

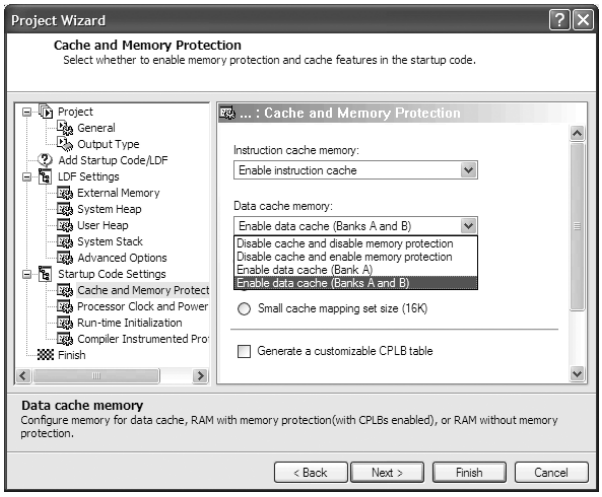
Leverage Proven Application Infrastructure

VisualDSP++ goes beyond robust code generation tools, providing considerable application infrastructure and "middleware" out-of-the-box to speed application development. The VisualDSP++ Kernel (VDK) is a robust, royalty-free real-time operating system (RTOS) kernel. It provides essential kernel features in a minimal footprint. Features include a fully pre-emptive scheduler (time slicing and cooperative scheduling are also supported), thread creation, semaphores, interrupt management, inter-thread messaging, events, and memory management (memory pools and multiple heaps). In MP environments, MP messaging is also provided. Configuration of these elements is done graphically, with code wizards to speed the creation of new threads and interrupt handlers. VDK has been available for multiple releases of VisualDSP++ and is now a key component of products shipping from a number of high volume vendors. Several commercial RTOSs are also available from select Analog Devices third parties.

Blackfin Processors can take advantage of the System Service Library (SSL), which provides consistent, easy C language access to Blackfin features such as the interrupt manager, direct memory access (DMA), and power management units. Clock frequency and voltage can be changed easily at runtime through a set of simple APIs. Interrupt handling can be "live," fired at the time of the event, or "deferred" to a later time of the application's choosing. A device manager integrates device drivers for on- and off-chip peripherals. VisualDSP++ includes ever expanding device driver support for all on-chip peripherals and off-chip devices found on Analog Devices EZ-KIT Lite and EZ-Extender® products. The SSL is OS-neutral and can be run as a standalone or in conjunction with an RTOS.

Built upon the system service library, the file system service (FSS) provides a portable and extensible means of accessing mass storage media from the Blackfin Processor. Support for the ADSP-BF548 EZ-KIT Lite development board is provided with VisualDSP++ 5.0 for FAT file systems on the attached hard disk drive, supplied SD card, and USB flash.

As embedded applications become increasingly part of the "connected world," the ability to rapidly add reliable Ethernet or USB connectivity to an application can often make or break a development schedule. For Blackfin Processors, VisualDSP++ includes a tuned port of the open-source LwIP TCP/IP stack. An example application showcasing an embedded Web server is among the highlights of this support. For Blackfin Processors and SHARC Processors, USB 2.0 device connectivity is provided. Bulk and asynchronous transfer modes are supported out-of-the-box, with USB-IF logo certified embedded and host applications provided with full source code.



Source code generation.

Wrapping all of these powerful tools and libraries is VisualDSP++'s state-of-the-art Integrated Development and Debugging Environment (IDDE). The IDDE includes full-featured editing and project management tools, with incremental builds, multiple build configurations ("Debug" and "Release," for example), syntax-coloring editor, and many other code editing features. Makefiles can be imported and exported freely. For Blackfin Processors, many application attributes can be configured graphically, enabling point-and-click access to SDRAM setup, stack and heap placement, power management, clock speed, cache setup, and more.

Debug and Tune Your Application with Ease

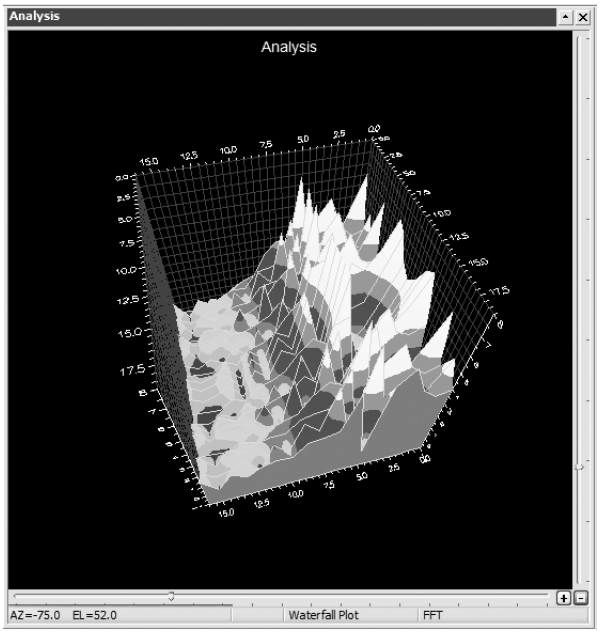
The ability to develop a high performance application is often gated by the visibility into your running system that your debugger provides. VisualDSP++ excels in this regard, with best-in-class debugging and inspection support. Robust fundamental C language source debugging (source level stepping and breakpoints, stack unwinds, local variable and C expression support, memory and register windows) serves as a foundation upon which multiple innovative and unique tools rest.

VisualDSP++

Integrated Development Environment

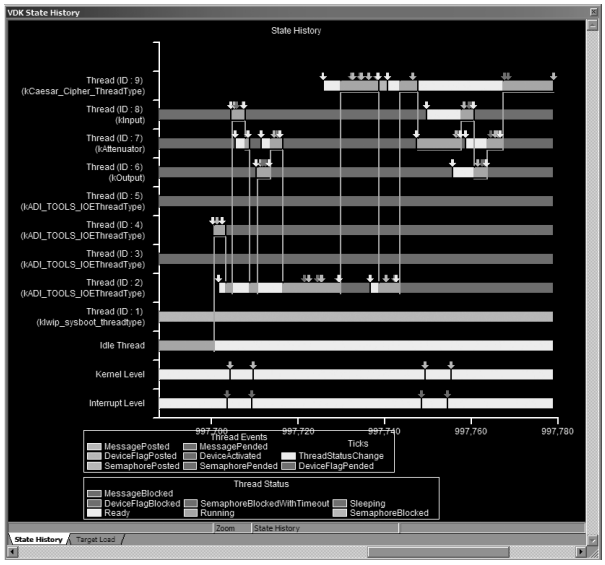
VisualDSP++ supports a variety of debugging "targets." Most common is a JTAG connection to an EZ-KIT Lite board or to custom target board by means of Analog Devices' emulator products. However, there will be occasions where closer inspection in a simulated environment may be required. VisualDSP++ provides core cycle-accurate simulators, allowing inspection of every nuance of activity within the processor, including visualization of the processor's pipeline and cache. These simulators are robust and highly accurate, so much so that they are used by Analog Devices' own silicon designers for validation. A second simulator is available to Blackfin Processor users—a high speed functional simulator. Using proprietary just-in-time (JIT) technology, the simulators have the ability to simulate millions of cycles per second on the most modest of host PCs. Effectively, this means that what used to be an overnight run is now a 10 minute coffee break, and what was once a coffee break is now a near instantaneous simulation.

As many of the most performance-demanding applications process a signal of some sort, comprehensive memory plotting is a cornerstone of VisualDSP++ debugger support. VisualDSP++ provides multiple views, from basic (line plots) to sophisticated (eye diagrams and waterfalls), to pinpoint anomalous data sequences in your application. Image viewing in a number of data formats is also available.



Comprehensive memory plotting.

Users of the VDK get unparalleled visibility into the internals of the kernel. Status on a per-thread basis is available, as is a comprehensive pictorial history of kernel events and CPU loading. Thread changes, posted and pended semaphores, and other kernel events are captured in this display.



Kernel event history.

For Blackfin Processors and SHARC Processors, inspection, or even application stimulation, from the debugger at run-time is possible through the use of the processor's Background Telemetry Channel (BTC). BTC allows for an arbitrary number of communication channels to be established between the host debugger and application. Channels may go in either direction, so BTC can be used to read and write data as the processor runs. Scalar values or entire arrays may be serviced by a channel. Arrays read from the target can even be plotted in real time.

MP users get the same compelling set of debugging features across all processors, unified into a single debugging interface. Individual windows can be made to "float" their focus to whichever processor currently is the debugger's focus, or they can be "pinned" to a specific processor so their contents do not follow the debugger's focus. To further aid MP debug, synchronous run, step, halt, and reset are also provided.

The Analog Devices patented statistical profiler offers unprecedented and unique visibility into a running application. Operating completely nonintrusively to the application, the application is polled thousands of times per second and a statistical view of where an application is spending the majority of its time is quickly assembled. This tool can be used to easily inspect an application for unexpected hotspots (suggesting the need to move a key routine from external to internal memory, for example). Simulator targets provide a completely linear profiling view. For Blackfin Processors, traditional instrumented profiling is also available.

Going even further, the VisualDSP++ compiler is able to act upon profiling information. Profile-guided optimization (PGO) is a technique that allows the compiler to instrument an application, run the application, and then make a second-pass compilation, exploiting the information that was gathered during the run of the application. This gives the compiler unique insight on a block-by-block basis, allowing it to optimize with a level of granularity that is not possible with a tool that operates only a file-by-file basis.

VisualDSP++

Integrated Development Environment

Integrate into Your Existing Environment

A development tool suite is always a part of an organization's larger software engineering environment. VisualDSP++ has been designed to operate in a larger environment.

Since an embedded engineer is often developing on a new platform while maintaining existing products that were likely developed with an earlier version of the tools, VisualDSP++ can be installed discretely an arbitrary number of times at a variety of release levels, allowing engineering to easily switch between current and legacy versions of VisualDSP++.

To better integrate to source code control (SCC) systems, VisualDSP++ is able to connect to any SCC provider that supports the Microsoft Common Source Code Control (MCSCC) interface. This interface is supported by all leading SCC vendors. VisualDSP++ goes one step further by supporting the control of VisualDSP++ itself within a source code control system.

The ability to robustly test an embedded application is enabled through a comprehensive automation Application Programmers Interface (API). Using Microsoft's language-neutral automation technology, nearly every feature of the graphical environment is available to script authors. Applications can be rebuilt, downloaded, and run from a simple script executed from the command-line or from within a custom test harness framework. The Automation API is supported by C++ and VBScript examples for all API calls, though any Automation-aware language can be used.

For prototype runs and/or small volume deployment, an Analog Devices emulator can be used to flash a program onto your custom system. Accessible through the Automation API, the flash programmer can be scripted, making it possible to develop a turnkey user interface for use by a production floor technician or other individual not familiar with VisualDSP++. Device drivers are provided for all flash devices found on EZ-KIT Lite products and these drivers are easily adjusted to support an arbitrary flash device.

The standalone flash programmer enables the development engineer to script or automate this process with a license-free tool, allowing the manufacturing technician to repeatedly program any number of boards prior to major production.

To download a test drive, visit *www.analog.com/processors/tools/testdrive*.

Development Tools: Extended Development Tools Products

In addition to CROSSCORE development tools, there are a variety of starter kits, hardware, and software available.

Starter Kit—provides everything needed to get started on an application. Starter Kits contain a Blackfin EZ-KIT Lite, EZ-Extender daughter board(s) and the Software Development Kit (SDK) which contains sample code, "how to" documents, and various encoders/decoders that make getting started on an application easy and shortens the learning curve.

Software Development Kits (SDK)—contains example software, source code, device drivers, algorithms, utilities information, and application notes that allow you to develop processor applications. The software can be used as a framework, or as examples of how to use certain aspects and peripherals, in conjunction with an ADI processor. The SDK is included in the starter kits and is also available for free download, provided you have the required hardware, at *www.analog.com/SDK/downloads*.

Multimedia Starter Kit—The Blackfin multimedia starter kit provides everything you need to get started on a multimedia application. Using a Blackfin EZ-KIT Lite and EZ-Extenders daughter board(s) to perform multimedia related tasks, learn how to render/capture video and audio streams using various off the shelf multimedia devices. As well, the SDK contains source code, "how to" documents, and various encoders/decoders that make getting started easy and shortens the learning curve.

Audio Starter Kit—The Blackfin audio starter kit provides everything you need to get started on an audio application. Using an ADSP-BF537 Blackfin EZ-KIT Lite and EZ-Extenders daughter board(s) to perform audio related tasks, learn how to render audio streams using various off the shelf audio devices and from files available on PCs. As well, the SDK contains source code, "how to" documents, and various encoders/decoders that make getting started easy and shortens the learning curve.

Also included in the starter kit is VisualAudio release 2.5. VisualAudio enables engineers from other backgrounds to leverage a set of basic audio libraries and tools to jump start their projects, modularize the development process, and shorten the learning curve.

VisualAudio®—embodies a significant amount of SHARC and Blackfin Processor audio expertise and enables engineers from other backgrounds to leverage a set of basic audio libraries and tools to jump-start their projects, modularize the development process, and shorten the learning curve. It works in conjunction with VisualDSP++, Analog Devices' development environment for SHARC and Blackfin Processors.

μClinux—is an open-source OS that has gained significant attention and popularity over the past few years. There are several advantages for having open-source tools available for the Blackfin Processor: source code availability, royalty-free licenses, reliability, community support, tools availability, networking support, portability, and an extensive application base. Developers have the opportunity to develop even the most demanding feature-rich applications in a very short time frame, and can leverage the work of others in the community. The μClinux kernel and GNU toolchain have been ported to the Blackfin Processor and are both available for download from the μClinux website. This website (*www.blackfin.uclinux.org*) is the central repository for all open-source Blackfin projects. Examples of current Blackfin Projects are: GNU Toolchain for Blackfin (gcc 3.x), Uboot for the Blackfin Processor, CoLinux Port of Blackfin Tools, μClinux for Blackfin Documentation, JTAG Tools for Blackfin, Networked Audio Media Node, and Networked Oscilloscope.

One of the board support packages is the ADSP-BF537 STAMP μClinux Kernel board support Package (BSP). The STAMP board has been specifically designed to support the development and porting of open-source μClinux applications and includes the full complement of memory along with serial and network interfaces. A variety of daughter cards that plug into this board are also available. Go to *www.blackfin.uclinux.org* for the most current open-source hardware and software information for the Blackfin Processor.

NI LabVIEW Embedded Module for ADI Blackfin Processors—The NI LabVIEW Embedded Module for ADI Blackfin Processors is a comprehensive graphical development environment for embedded design. This module builds on NI LabVIEW Embedded technology, which facilitates dataflow graphical programming for embedded systems and includes hundreds of analysis and signal-processing functions, integrated I/O, and an interactive debugging interface. With the NI LabVIEW Embedded Module for ADI Blackfin Processors, users can easily access essential VisualDSP++ specific compiler options through LabVIEW such as the ability to enable cache, optimize linking, and view live front-panel updates via JTAG. To help debug those challenging designs, users can connect the host development PC to evaluation hardware or end product using an Analog Devices JTAG emulator. LabVIEW includes a wide array of built-in visualization features including tools for charting and graphing real-time data and reconfiguring attributes of data presentation, such as colors, font size, and graph types. Furthermore, users can dynamically tune applications at run time through live front panel controls.

Green Hills® Software (GHS)—Along with Analog Devices, GHS has developed a multiyear product roadmap for hardware and software development tools, providing full support for the Blackfin Processor. These include MULTI® Integrated Development Environment (IDE); C, C++, and EC++ compilers; Probe™ and Slingshot™ probe; and real-time operating systems (RTOS) INTEGRITY® and μ-velOSity.™ From simulation to deployment, GHS technology saves time throughout a project development life cycle with powerful features and an efficient design that eliminates having to learn different tools and user interfaces.

CROSSCORE Development Tools Selection Table

Processor	Evaluation Development Platform	Emulator	VisualDSP++ Development Software	Additional Software Available
Blackfin Processors				
ADSP-BF531 ADSP-BF532 ADSP-BF533	ADZS-BF533-EZLITE ADZS-BF-EZEXT-1 ADZS-BFAV-EZEXT ADZS-USBLAN-EZEXT ADZS-BFAUDIO-EZEXT ADZS-BFFPGA-EZEXT ADZS-BF533-MMSKIT	ADZS-USB-ICE ADZS-HPUSB-ICE	VDSP-BLKFN-PC-TEST VDSP-BLKFN-PC-FULL VDSP-BLKFN-PCFLOAT VDSP-BLKFN-PCFLT-5	VDSP-LABVIEW-EMB (All parts except ADSP-BF535, ADSP-BF561) VDSP-LVBF-TOOLKIT (ADSP-BF533, ADSP-BF537 only) VDSP-LABVIEW-FULL (All parts except ADSP-BF535, ADSP-BF561) Software Development Kit (SDK) (ADSP-BF533, ADSP-BF537, ADSP-BF561 only) VisualAudio (ADSP-BF533, ADSP-BF537 only) Mathworks (ADSP-BF531, ADSP-BF532, ADSP-BF533, ADSP-BF534, ADSP-BF536, and ADSP-BF537 only)
ADSP-BF535	ADDS-BF535-EZLITE			
ADSP-BF534 ADSP-BF536 ADSP-BF537	ADZS-BF537-EZLITE ADZS-BFAV-EZEXT ADZS-USBLAN-EZEXT ADZS-BFAUDIO-EZEXT ADZS-BFFPGA-EZEXT ADZS-BF537-STAMP ADZS-BF537-ASKIT			
ADSP-BF538/ ADSP-BF538F	ADZS-BF538F-EZLITE ADZS-BFAV-EZEXT ADZS-USBLAN-EZEXT ADZS-BFAUDIO-EZEXT ADZS-BFFPGA-EZEXT			
ADSP-BF561	ADZS-BF561-EZLITE ADZS-BF-EZEXT-1 ADZS-BFAV-EZEXT ADZS-BFAUDIO-EZEXT ADZS-BFFPGA-EZEXT ADZS-USBLAN-EZEXT ADZS-BF561-MMSKIT			
ADSP-BF542 ADSP-BF544 ADSP-BF547 ADSP-BF548 ADSP-BF549	ADZS-BF548-EZLITE			
ADSP-BF523/C ADSP-BF525/C ADSP-BF527/C	ADZS-BF527-EZLITE			
ADSP-BF522/C ADSP-BF524/C ADSP-BF526/C	TBD			
TigerSHARC Processors				
ADSP-TS101S ADSP-TS201S ADSP-TS202S ADSP-TS203S	ADZS-TS201S-EZLITE	ADZS-USB-ICE ADZS-HPUSB-ICE	VDSP-TS-PC-TEST VDSP-TS-PC-FULL VDSP-TS-PCFLOAT VDSP-TS-PCFLT-5	Mathworks (ADSP-TS201 only)
SHARC Processors				
ADSP-21065L	ADDS-21065L-EZLITE	ADZS-USB-ICE ADZS-HPUSB-ICE	VDSP-SHARC-PC-TEST VDSP-SHARC-PC-FULL VDSP-SHARC-PCFLOAT VDSP-SHARC-PCFLT-5	VisualAudio (ADSP-21262, ADSP-21364, and ADSP-21369 only) Mathworks (ADSP-21363, ADSP-21364, and ADSP-21365 only)
ADSP-21160M ADSP-21160N	ADZS-21160-EZLITE			
ADSP-21161N	ADZS-21161N-EZLITE			
ADSP-21261 ADSP-21262 ADSP-21266	ADZS-21262-EZLITE ADZS-21262-1-EZEXT ADZS-SHRCUSB-EZEXT			
ADSP-21362 ADSP-21363 ADSP-21364 ADSP-21365 ADSP-21366	ADZS-21364-EZLITE ADZS-SHRCUSB-EZEXT			
ADSP-21367 ADSP-21368 ADSP-21369	ADZS-21369-EZLITE ADZS-SHRCUSB-EZEXT			
ADSP-21371 ADSP-21375	ADZS-21375-EZLITE			

Software Modules for Blackfin and SHARC Processors

Overview

Analog Devices (ADI) software modules are a series of popular audio and video algorithms for Blackfin Processor-based designs and a series of SHARC Processors. The highly optimized software modules allow you to quickly and easily incorporate these multimedia functions, providing a fast development path to the end product. The software modules feature a consistent API and framework to ensure rapid integration of multiple software algorithms. In addition, these audio software modules can be combined with ADI's award-winning VisualAudio postprocessing libraries consisting of over 200 audio building-block modules including mixers, filters, and delays, as well as cascaded biquad filters, reverbs, equalization, and musical effects. For more information on VisualAudio, please visit *www.analog.com/visualaudio*.

Developed internally by ADI, these software module implementations are provided free to Blackfin and SHARC Processor software programmers. New and revised modules and their supported processors are added frequently. For the latest information on software modules go to *www.analog.com/software*.

Hardware Requirements

The software modules run on ADI EZ-KIT Lite evaluation boards and EZ-Extender daughter boards or on custom boards with supported processors.

Availability and Licensing

Each module supports ADI Blackfin and SHARC Processors and is a licensed product that is available in object code format. Recipients must sign a license agreement with ADI prior to receiving the production modules identified in the license agreement.

Licensing restrictions for Dolby®, DTS®, and Microsoft®

Customer must be a licensee for Dolby, DTS, or Microsoft before production code can be shipped for that particular algorithm. Dolby, DTS, and Microsoft modules have been certified on specific processors. Check *www.analog.com/software* for more information.

Worldwide Support

Each software module includes a detailed developer's guide and example code to get you started. Online support for each module is available on ADI's website, *www.analog.com/software*. Additional support for designers and programmers is available by emailing *software.module.support@analog.com*. Support for system integration is available through ADI's third parties.

Third-Party Developers

ADI has an extensive network of ADI third-party developers available to provide additional software modules and system integration support. Visit *www.analog.com/processors/collaborative*.

Platforms and Reference Designs

Platforms and reference designs help jumpstart your design. They include comprehensive software suites with documented APIs running on application-specific evaluation boards. The easy to use APIs enable customization and control of core system functions, letting you focus on adding value through product differentiation. For more information on Analog Devices platforms, reference designs, and third-party reference designs, visit *www.analog.com/software*.

Key Features

- Free implementation of popular multimedia algorithms
- Many evaluation code modules downloadable from the Web
- Modules developed directly by Analog Devices
- Highly optimized—coded by ADI processor experts
- Consistent API (application programming interface) and framework across all modules
- Uses ADI's development tools
- Runs on VisualDSP++ 4.5
- Support for Blackfin and SHARC Processors

Each Software Module Includes

- Library module with a standard C-callable API consistent with other code modules
- Reference C source code interface routine that calls the code as a single library module
- Demonstration software for execution on ADI evaluation boards
- Documentation, including application notes and detailed developers' guides

Video/Imaging Decoders for Blackfin
MPEG-4 SP/SAP Decoder
H.264 BP Decoder
Windows Media Video (WMV9) Standard Decoder
MPEG-2 Video Decoder
JPEG/Motion-JPEG Decoder
Video Encoders for Blackfin
H.264 BP Encoder
JPEG/Motion-JPEG
MPEG-4 SP Encoder
Audio Decoders and Post Decoders for Blackfin
MP3 Decoder
Windows Media Audio (WMA9) Standard Decoder
MPEG-4 HE-AAC v1 Decoder
MPEG-4 HE-AAC v2 Decoder
MPEG-4 AAC-BSAC Decoder
MPEG-4 AAC-LC Decoder
Audio Decoders and Post Decoders for Blackfin and SHARC
DTS Neo.6
DTS 5.1 Decoder
Dolby Digital (AC-3) 5.1 Decoder
Dolby Headphone v2
Dolby Virtual Speaker
Dolby Pro Logic IIx/EX Decoder
Audio Encoders for Blackfin
MP3 Encoder
MPEG-4 HE-AAC v2 Encoder
Dolby Digital (AC-3) Consumer Encoder
Postprocessing for Blackfin
Asynchronous Sample Rate Converter

The Collaborative

Third-Party Program for Embedded Processor and DSP Applications

Tap Into the Experience and Global Reach of the Collaborative

Working together to extend your design team

The Collaborative is Analog Devices' Third-Party Program for Embedded Processor and DSP Applications. Our partners offer tools, services, and solutions for the Blackfin, SHARC, and TigerSHARC processors, and target a wide range of marketing applications:

Audio
Automotive
Digital Home
Industrial and Instrumentation
Multimedia
Portable Consumer/Low Power
VoIP
Security
Medical

Refer to the Markets and Applications section of this selection guide for a full list of application areas our third-party partners can assist you with. When you select Analog Devices as your Embedded Processor vendor, you are broadening your design team to include the industry-leading resources of the ADI Collaborative. The Collaborative is composed of over 200 partners who offer more than 700 commercial products and hundreds of custom solutions. These partners offer consulting services as well as a wide range of commercial off-the-shelf (COTS) products. Their development tools are specifically designed to work with Analog Devices Embedded Processor-based systems.

Platforms and Reference Designs

Platforms and reference designs help jumpstart your design. They include comprehensive software suites with documented APIs running on application-specific evaluation boards. The easy to use APIs enable customization and control of core system functions, letting you focus on adding value through product differentiation. For more information on Analog Devices platforms, reference designs, and third-party reference designs, visit *www.analog.com/software*.

With the Collaborative, you are supported by highly reputable brands, patented technologies, and the pioneers in real-time system design and debugging. The Collaborative partners offer products and services that provide both system- and application-level expertise.

Speed up your design process by leveraging the solutions our partners have to offer:

ADI Embedded Processor Support
Algorithms and Libraries
COTS Hardware Boards
Debuggers
Development and Evaluation Boards
Development Tools
Emulators
Integrated Systems for ADI Embedded Processors
Real-Time Operating Systems
Design Test Optimization
Software IDDE Tools
Software

Designing with Analog Devices' third-party Collaborative team is a proven strategy for maximizing your resources.

To see a complete listing of third-party developers, visit the Collaborative website at *www.analog.com/processors/collaborative*.

Benchmarks
Comparing Processors

To truly assess a processor's performance, you have to look beyond MHz, MIPS, or MFLOPS. There are many attributes that may be more accurate predictors of real-time signal processing performance.

Circular Buffers
Circular buffers allow a region of memory to be continually accessed without explicit program interaction. The buffer uses a pointer that automatically resets to the beginning of the buffer (wraparound) if the pointer is advanced beyond the last location in the buffer. Circular buffers are a key feature of DSP routines. Multiple buffers are used in the same routine to store filter coefficients and implement a delay line of input samples. Performance suffers if the DSP core has to perform pointer calculations along with the calculations for the routine. Performance also suffers if the DSP core only supports one circular buffer and must save and restore address registers to implement multiple buffers.

Analog Devices processors have hardware support for multiple circular buffers, eliminating processor overhead for address calculations.

DMA Channels/Nonintrusive DMA
The DMA (direct memory access) channels transfer data between an external source and the processors' on-chip memory. With DMA channels, data transfers occur without the core processor having to execute data movement instructions. For example, the overhead clock cycles used to move data for an FFT can add a significant amount of time to overall algorithm execution. With multiple DMA channels available, all data transfers happen without core involvement, eliminating any overhead clock cycles.

One of the strengths of Analog Devices processor architecture is that these DMAs do not interfere with the core operation. This capability is referred to as nonintrusive or zero-overhead DMA.

Interrupt Latency
Interrupt latency is a measure of how quickly a processor responds to an interrupt. Quick response is important, especially in real-time processing. For example, an interrupt that might indicate the availability of data is only available for a finite amount of time; therefore, fast response is critical, or the data will be lost.

Analog Devices products feature fast interrupt response time for quick execution of interrupt service routines.

Multiprocessing Support
Even with the powerful DSPs available today, there are times when the DSP task for a given system does not fit into a single processor. Examples of such applications include sonar, radar, medical imaging, audio mixers, etc. In these cases, the ability to connect multiple processors in a system without any glue logic greatly simplifies the implementation.

Analog Devices offers TigerSHARC Processors with specialized hardware for glueless multiprocessing.

On-Chip Memory/On-Chip SRAM Size
The amount of on-chip memory available can greatly impact system performance, cost, size, power consumption, and complexity. Any time the DSP core accesses external memory, performance can suffer. Off-chip memory often requires the core to wait additional cycles. In contrast, the DSP core can access on-chip memory at the same rate as its instruction rate. Supplemental memory adds extra components to the system, which increases cost, power consumption, and complexity.

Analog Devices leads the industry in DSP SRAM integration. ADI processors have on-chip memories that often eliminate the need for external memory in a system. Furthermore, the memory is configurable for data-word size, code word size, and storage size. This allows designers to tailor the memory to meet the algorithm requirements.

TDM Mode
TDM (time division multiplexed) mode refers to time division multiplexing, which is a common mode for transferring serial data. In telecommunications applications, T1 and E1 lines use TDM. TDM allows multiple serial devices to send and receive information using the same physical connection. TDM also allows communication between multiple processors.

All ADI products support TDM mode in the serial ports.

Zero-Overhead Looping
The code for most DSP routines falls naturally into a set of nested loops. Without the support for zero-overhead looping, the DSP core must spend cycles calculating the loop termination values, in addition to the cycles used to process the algorithm's computations. Without zero-overhead looping, performance degrades.

Analog Devices offers 16-bit fixed-point and 32-bit fixed- and floating-point processors with zero-overhead, nestable looping to save instruction cycles.

ADI Processor Benchmarks[1]

	Cycle Count	Execution Time @ 750 MHz
Blackfin Processor		
Block FIR Filter	(x/2)(2 + h)	
Biquad IIR Filter (4 Coeff)	2.5bq + 3.5	
Complex FIR Filter	2h + 2	
Delayed LMS Filter	1.5h + 4.5	
1024-Point Complex FFT (Prescaled)	11,559	15.4 µs
256-Point Complex FFT (Out of Place)	2324	3.10 µs
Max Search	0.5×	
Max Index Search	0.5×	

	Cycle Count	Execution Time @ 600 MHz
TigerSHARC Processor		
256-Point Radix 2 Complex FFT (16-Bit)	585	0.975 µs
1k Point Complex FFT[2] (Radix 2) (32-Bit)	9419	15.7 µs
64k Point Complex FFT[2] (Radix 2) (32-Bit)	1,397,544	2.33 ms
FIR Filter (per Real Tap) (32-Bit)	0.5	0.83 ns
[8 × 8][8 × 8] Matrix Multiply (Complex, Floating-Point)	1399	2.3 µs

	ADSP-21160N ADSP-21161N	ADSP-2126x	ADSP-2136x	ADSP-21371 ADSP-21375
SHARC Processor (SIMD)				
Clock Speed	100 MHz	200 MHz	400 MHz	266 MHz
Instruction Cycle Time	10 ns	5 ns	2.5 ns	3.75 ns
MFLOPS Sustained, Peak	400 MFLOPS, 600 MFLOPS	800 MFLOPS, 1200 MFLOPS	1600 MFLOPS, 2400 MFLOPS	1064 MFLOPS, 1596 MFLOPS
MOPS (32-Bit, Fixed-Point) Sustained, Peak	400 MFLOPS, 600 MFLOPS	800 MFLOPS, 1200 MFLOPS	1600 MFLOPS, 2400 MFLOPS	1064 MFLOPS, 1596 MFLOPS
1024-Point Complex FFT (Radix 4, with Digit Reverse)	92 ms	46 µs	23 µs	34.5 µs
FIR Filter (per Tap)	5 ns	2.5 ns	1.25 ns	1.88 ns
IIR Filter (per Biquad)	20 ns	10 ns	5.0 ns	7.5 ns
Matrix Multiply (3 × 3) × (3 × 1)	45 ns	22.5 ns	11.25 ns	16.91 ns
(4 × 4) × (4 × 1)	80 ns	40 ns	20.0 ns	30.07 ns
Divide (y/x)	30 ns	15 ns	7.5 ns	11.27 ns
Inverse Square Root	45 ns	22.5 ns	11.25 ns	16.91 ns

NOTES
[1]Benchmarks are for best data conditions.
[2]Cache preloaded.

h = number of taps.
bq = number of biquads.
x = number of samples.

ADI Processor Benchmarks

BDTI Processor Comparison

The BDTImark2000 provides a summary measure of signal processing speed. A higher BDTImark2000 score indicates a faster processor. For more information about the BDTImark2000 and how it is calculated, visit *www.BDTI.com*.

BDTImark2000® Scores for 2006	
Fixed-Point	
ADSP-TS201 (600 MHz)	6400
ADSP-TS202/ADSP-TS203 (500 MHz)	5130
ADSP-BF53x (750 MHz)	4190
ADSP-219x (160 MHz)	410
ADSP-218x (80 MHz)	240
Floating-Point	
ADSP-TS201 (600 MHz)	4480
ADSP-TS202/ADSP-TS203 (500 MHz)	3620
ADSP-213xx (400 MHz)	2050
ADSP-2126x (200 MHz)	1090
ADSP-2116x (100 MHz)	550

ADI Processor Benchmarks

EEMBC Blackfin Comparison

EEMBC® benchmarks represent out-of-the-box performance for a typical suite of consumer applications. For more information, see *www.eembc.com*.

Blackfin Controller Performance

Processor	Blackfin	ARM1136JF-S	ARM926EJ-S
Product	**BF533**	**i.MX31**	**i.MX21**
Clock Frequency (MHz)	594	532	266
Certified on Hardware?	yes	yes	yes
EEMBC Networking 2.0[1]			
IPmark[2]	45	50.4	24.4
TCPmark[2]	117	68.5	29.2[3]
EEMBC Autobench 1.1[1]			
Automark[2]	183.1	126.6	29.6
EEMBC ConsumerBench1.1[1]			
Consumermark[2]	54.9	26.6	13.7
EEMBC AOBench1.1[1]			
AOmark[2]	352	341	152
EEMBC TeleBench1.1[1]			
Telemark[2]	11.7	6.1	2.5
EEMBC DENBench1.0[1]			
MPEG Decodemark[2]	337	231	112
MPEG Encodemark[2]	392	243	100
Cryptomark[2]	257	219	104
Imagemark[2]	352	315	154
DENmark[2]	57.5	45.5	21.6
EEMBC Geometric Mean	138.7	99.3	42.6

NOTES
[1]Out-of-the-box category.
[2]Iterations per second (bigger is better).
[3]i.MX21 TCPmark contains an estimate for one subtest whose result is filed n/a at EEMBC. (Estimate was ½ i.MX31 performance.)

EEMBC is a registered trademark of the Embedded Microprocessor Benchmark Consortium.
For more information and scores go to *www.eembc.org*.

eCL Certified!
http://www.ebenchmarks.com

Part Numbering System

ADSP-XXxxxxtpp[z][qqq(q)][1]

Analog Devices Digital Signal Processing

Product Number
BFxxxx = Blackfin Processor
TSxxxx = TigerSHARC Processor
21xxxx = SHARC Processor
21xx = 16-Bit DSP
2199x = Mixed-Signal DSP

Temperature (t)
J, K, L, M = Commercial Temp Range
A, B, C = Industrial Temp Range
S, T, U = Military Temp Range
W, Y, Z[2] = Automotive Temp Range

Examples:
ADSP-BF538BBCZ-4A
ADSP-BF533SBBZ500
ADSP-BF534BBC-4A
ADSP-21261SKBC-150
ADSP-21367KBPZ-2A
ADSP-TS201SABP-060

X-Grade (q)
R, R7, RL, Reel

Speed or Product code [q]
See data sheet for speed and product code definition

Pb-Free

Package (p): Per ADI Spec ADI0386
S = Metric Quad Flat Pack (MQFP)
ST = Low-Profile Quad Flat Pack (LQFP)
B, B1, B2 = Plastic Ball Grid Array (PBGA)
BZ, BZ1, BZ2 = Lead-Free Plastic Ball Grid Array (PBGA)
Z = Ceramic Quad Flat Pack (QFP), heat slug up
W = Ceramic Quad Flat Pack (QFP), heat slug down
P = Plastic Leaded Chip Carrier (PLCC)
G = Pin Grid Array (PGA)
BC, CA = Chip Scale Package Ball Grid Array (CSP_BGA)
BCZ, CAZ = Lead-Free Chip Scale Package Ball Grid Array (CSP_BGA)
BP = *Super* BGA® (SBGA) Thermal-Enhanced Flip Chip Ball Grid Array (FCBGA)
SW = Exposed Pad (E_Pad)

[1]Please refer to individual data sheets for specific part numbering, temperature ranges, and ordering information.

[2]Z for legacy model temp range.

Blackfin Processor Family

High Performance, Low Power Processing Leadership

Blackfin Processors are a new breed of embedded media processors, designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. Blackfin Processors combine a 32-bit RISC-like instruction set and dual 16-bit Multiply Accumulate (MAC) signal processing functionality with the ease-of-use attributes found in general-purpose microcontrollers. Blackfin Processors perform equally well in both signal processing and control processing applications, in many cases deleting the requirement for separate heterogeneous processors. This capability greatly simplifies both the hardware and software design implementation tasks.

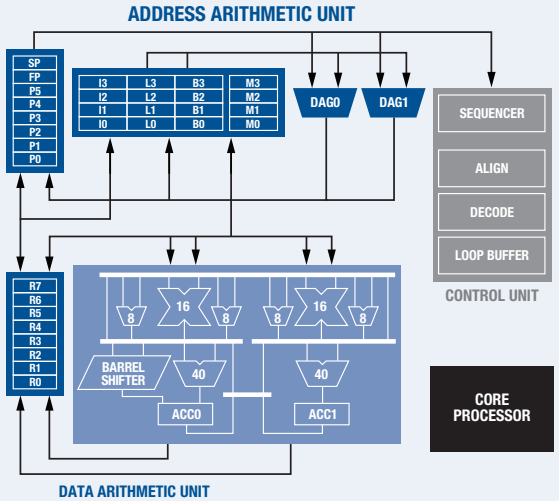
Blackfin Processors offer performance up to 750 MHz/1512 MMACS in single-core products. New symmetric, multiprocessor members of the Blackfin family extend this to over 3000 MMACS. The family offers the lowest power consumption—as low as 0.15 mW/MMAC at 0.8 V. The combination of high performance and low power is essential in meeting the needs of today and future signal processing applications, including broadband wireless, audio/video-capable Internet appliances, and mobile communications.

All Blackfin Processors offer fundamental benefits to the system designer, including:

- High performance signal processing and efficient control processing capability
- Dynamic power management (DPM), enabling the system designer to tailor device power consumption to the end-system requirements
- Easy to use instruction set architecture and development tools suite that saves development time

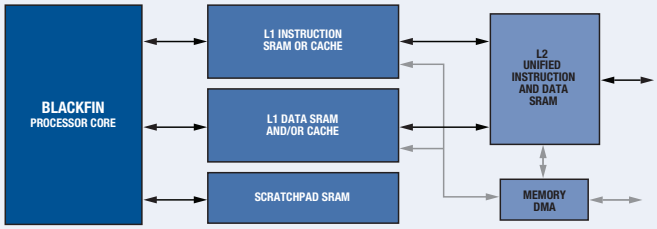
High Performance Signal Processing

The Blackfin Processor architecture employs numerous techniques to ensure that signal processing performance is maximized. These include a fully interlocked instruction pipeline, multiple parallel computational blocks, efficient DMA capability, and instruction set enhancements designed to accelerate video processing.



Efficient Control Processing

The Blackfin Processor architecture also offers a variety of benefits most often seen in RISC control processors. These features include a hierarchical memory architecture, superior code density, and a variety of microcontroller-style peripherals, including a watchdog timer, a real-time clock, and an integrated SDRAM controller. All of these features provide the system designer with a great deal of design flexibility while minimizing end system costs.



Dynamic Power Management

All Blackfin Processors employ multiple power-saving techniques. Blackfin Processors are based on a gated clock core design that selectively powers down functional units on an instruction-by-instruction basis. Blackfin Processors also support multiple power-down modes for periods when little or no CPU activity is required. Last, and probably most importantly, Blackfin Processors support a dynamic power management scheme whereby the operating frequency and voltage can be tailored to meet the performance requirements of the algorithm currently being executed. These transitions may occur continually under the control of an RTOS or user firmware. Currently available products also offer on-chip core voltage regulation circuitry as well as operation to as low as 0.8 V, and are particularly well-suited for portable applications requiring extended battery life.

Easy to Use

A single Blackfin Processor can be utilized in many applications previously requiring both a high performance signal processor and a separate efficient control processor. This benefit greatly reduces development time and costs, ultimately enabling end products to get to market sooner. Additionally, a single set of development tools can be used, which decreases the system designer's initial expenses and learning curve.

Platforms

- Blackfin Car Telematics
- Blackfin BRAVO®

Blackfin Processor Family

High Performance, Low Power Processing Leadership

Blackfin Car Telematics Platform

To serve the embedded processing market for feature-rich, multimedia car-telematics applications, Analog Devices has designed the Blackfin Car Telematics Platform. Based on a Blackfin Processor, which combines best-in-class signal processing performance with microcontroller functionality, the platform meets the computational demands and power constraints of in-vehicle safety systems, audio, video, and wireless communications.

The Blackfin Car Telematics Platform capitalizes on the processing power of a single Blackfin Processor to reduce telematics system costs, size, and development time by integrating many telematics tasks onto a single processing platform. This significantly reduces the system deployment costs compared with existing schemes where there are often separate hardware and software modules for each function. The functions implemented on the Blackfin Processor include GPS, handsfree operation, microphone array, voice-activated control, GSM interfaces, and car audio play/record of MP3 and WMA content.

The Blackfin Car Telematics Platform is fully supported with speech recognition and text-to-speech algorithms available from Scansoft, Inc., and with the noise- and echo-cancellation algorithms from Mbwave and Clarity.

Analog Devices Blackfin Car Telematics Platform is offered as a hardware reference design to suppliers of the automotive industry and includes all third-party software for MP3 and CD block decoding, AM/FM decoding, GPS, dead reckoning, acoustic echo cancellation, noise reduction, speech recognition, text-to-speech, and Bluetooth® stacks.

Blackfin BRAVO

The Blackfin BRAVO video chipsets deliver audio, streaming video, networked camera, and videophone capabilities with up to full D1, MPEG-4/MPEG-2/DivX/WMV9 30 fps full-color, full-motion video in CIF resolution over broadband networks. The chipsets include an Ethernet port to interface with cable, xDSL, Ethernet, USB, IEEE 802.11x, and fiber, and support Microsoft Windows Media, ISMA, and QuickTime protocols. Each is available as a chipset or a complete, highly integrated reference design.

Blackfin BRAVO Broadband Videophone

Delivering full-duplex audio and videophone functions for broadband networks, the Broadband Video and Audio Communications Reference Design uses a scalable bit rate and Ethernet port to enable operation over cable, xDSL, Ethernet, 3G, and fiber. The ADSST-VC-7000 delivers up to 30 fps resolution for CIF video and 4CIF for still images. It allows NTSC/PAL TVs equipped with standard RC-output and camera-input connectors to be connected to a high quality videophone.

Blackfin BRAVO Networked Camera Chipset

Any remote, unmanned camera connected to a broadband network or LAN can be used for remote surveillance applications with the Blackfin BRAVO NetCam Network Camera Chipset. The ADSST-NC-7000 chipset enables a PC browser to display what the camera sees, supporting an HTTP server function with MJPEG and MPEG-4 video to enable access and control from any standard PC with a Microsoft Internet Explorer or Netscape browser or QuickTime player. An optional trigger function enables the browser to sound an alarm when the camera senses predefined changes in motion or position. The reference design features full-color, full-motion video with up to 30 fps CIF resolution.

Blackfin BRAVO Voice-Over-IP Reference Design

The Blackfin BRAVO VoIP Reference Design is a complete system solution for building feature-rich, high performance, low cost VoIP desktop phones and telephone adapters. The design includes the complete suite of software for VoIP applications, all controlled by a comprehensive set of application program interfaces (APIs). The easy to use APIs provide the functionality for customization and control of core system functions, letting you focus on adding high value through product differentiation.

Blackfin Processor Roadmap

Analog Devices' long-term commitment to the Blackfin Processor means each subsequent generation of Blackfin-based designs will benefit from increases in speed, power efficiency, and cost reductions across a broad range for single and dual core processors.

The Blackfin Processor family includes devices that target a wide range of applications in the consumer, automotive, industrial, instrumentation, and communications markets. To address these markets, the Blackfin Processor family offers scalable performance from the 200 MHz ADSP-BF535 to the dual core 600 MHz ADSP-BF561 and the new ADSP-BF52x with advanced peripherals. Blackfin products also offer very low power consumption with products using as low as 0.16 mW/MHz. Future devices will further extend ADI's leadership in performance and power efficiency while maintaining code compatibility and providing the widest array of processor options for the most demanding converged processing challenges.

ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527 Blackfin Processors

Low Power with Advanced Peripherals

The ADSP-BF52x Blackfin Processor family combines high performance, power efficiency, and system integration to enable highly optimized designs without compromises. With built-in peripheral selectivity the ADSP-BF52x family provides the greatest flexibility for today's most demanding convergent signal processing applications. With power consumption as low as 0.16 mW/MHz[1] and performance up to 600 MHz, applications can now add greater signal processing performance without sacrificing battery life. The ADSP-BF52x family supports peripheral flexibility and system scalability to enable developers to create products that fit their target needs.

The high performance 16-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality allow system designers a flexible platform to address a wide range of portable applications, including consumer, communications, and industrial/instrumentation.

IP protection has become a necessary part of today's embedded computing applications. The ADSP-BF52x family provides a security scheme which balances flexibility and upgradeability with performance through the inclusion of a firmware-based solution including OTP (one-time programmable) memory to enable users to implement private keys for secure access to program code.

[1]Referenced at 250 MHz operating speed for 300 MHz and 400 MHz ADSP-BF52x parts only.

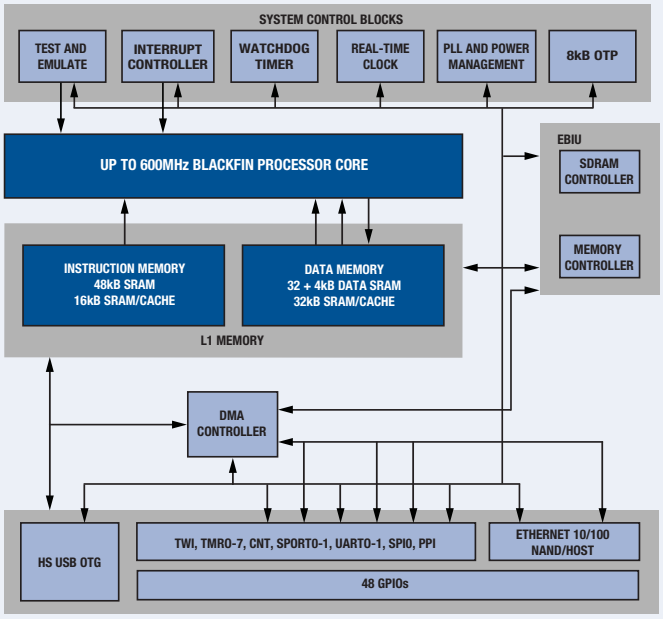
Applications

- VoIP
- Multimedia
- Multimedia accessories
- Home audio/video
- Instrumentation
- Imaging
- Industrial control
- PMP
- Mobile TV
- Coprocessor applications
- Networked audio
- Biometric systems
- Consumer audio
- Handheld and portable devices

Features

- Lockbox™ technology: hardware-enabled security for code and content
- Blackfin Processor core with up to 600 MHz (1200 MMACS) performance
- 2 dual-channel, full-duplex synchronous serial ports supporting 8 stereo I²S channels
- 12 peripheral DMA channels supporting one- and two-dimensional data transfers
- NAND flash controller with 8-/16-bit interface for commands, addresses, and data
- Connectivity: HS USB OTG, Host DMA Port, UARTs, SPORTs, SPI, and TWI
- Ethernet 10/100 MII/RMII interface
- Memory controller providing glueless connection to multiple banks of external SDRAM, SRAM, flash, or ROM
- Core voltage 0.95 V to 1.26 V
- 289-ball, 12 mm × 12 mm, 0.5 mm pitch CSP_BGA (commercial temperature range 0°C to 70°C)
- 208-ball, 17 mm × 17 mm, 0.8 mm pitch CSP_BGA (industrial temperature range –45°C to +85°C)
- For space-constrained audio applications the ADSP-BF52xC supports an embedded low power stereo codec

ADSP-BF527 BLOCK DIAGRAM



ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527 Blackfin Processors

Low Power with Advanced Peripherals

Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF522BBCZ-3A	300	600	132	208-CSP_BGA	Contact ADI
ADSP-BF522BBCZ-4A	400	800	132	208-CSP_BGA	
ADSP-BF522KBCZ-3	300	600	132	289-CSP_BGA	
ADSP-BF522KBCZ-3C1	300	600	132	289-CSP_BGA	
ADSP-BF522KBCZ-4	400	800	132	289-CSP_BGA	
ADSP-BF522KBCZ-4C1	400	800	132	289-CSP_BGA	
ADSP-BF523BBCZ-5A	533	1000	132	208-CSP_BGA	
ADSP-BF523KBCZ-5	533	1000	132	289-CSP_BGA	
ADSP-BF523KBCZ-5C1	533	1000	132	289-CSP_BGA	
ADSP-BF523KBCZ-6	600	1200	132	289-CSP_BGA	
ADSP-BF523KBCZ-6A	600	1200	132	208-CSP_BGA	
ADSP-BF523KBCZ-6C1	600	1200	132	289-CSP_BGA	
ADSP-BF524BBCZ-3A	300	600	132	208-CSP_BGA	
ADSP-BF524BBCZ-4A	400	800	132	208-CSP_BGA	
ADSP-BF524KBCZ-3	300	600	132	289-CSP_BGA	
ADSP-BF524KBCZ-3C1	300	600	132	289-CSP_BGA	
ADSP-BF524KBCZ-4	400	800	132	289-CSP_BGA	
ADSP-BF524KBCZ-4C1	400	800	132	289-CSP_BGA	
ADSP-BF525BBCZ-5A	533	1000	132	208-CSP_BGA	
ADSP-BF525KBCZ-5	533	1000	132	289-CSP_BGA	
ADSP-BF525KBCZ-5C1	533	1000	132	289-CSP_BGA	
ADSP-BF525KBCZ-6	600	1200	132	289-CSP_BGA	
ADSP-BF525KBCZ-6A	600	1200	132	208-CSP_BGA	
ADSP-BF525KBCZ-6C1	600	1200	132	289-CSP_BGA	
ADSP-BF526BBCZ-3A	300	600	132	208-CSP_BGA	
ADSP-BF526BBCZ-4A	400	800	132	208-CSP_BGA	
ADSP-BF526KBCZ-3	300	600	132	289-CSP_BGA	
ADSP-BF526KBCZ-3C1	300	600	132	289-CSP_BGA	
ADSP-BF526KBCZ-4	400	800	132	289-CSP_BGA	
ADSP-BF526KBCZ-4C1	400	800	132	289-CSP_BGA	
ADSP-BF527BBCZ-5A	533	1000	132	208-CSP_BGA	
ADSP-BF527KBCZ-5	533	1000	132	289-CSP_BGA	
ADSP-BF527KBCZ-5C1	533	1000	132	289-CSP_BGA	
ADSP-BF527KBCZ-6	600	1200	132	289-CSP_BGA	
ADSP-BF527KBCZ-6A	600	1200	132	208-CSP_BGA	
ADSP-BF527KBCZ-6C1	600	1200	132	289-CSP_BGA	

NOTES

[1]Certain models available in automotive grade temperature range.

[2]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548/ADSP-BF549 Blackfin Processors

High Performance Convergent Multimedia Processors

The ADSP-BF54x family was specifically designed to meet the needs of convergent multimedia applications where system performance and cost are essential ingredients. The integration of multimedia, human interface, and connectivity peripherals combined with increased system bandwidth and on-chip memory provides customers a platform to design the most demanding applications.

IP protection has become a necessary part of today's embedded applications. The ADSP-BF54x provides a security scheme that balances flexibility and upgradeability with performance through the inclusion of a firmware-based solution including OTP memory to enable users to implement private keys for secure access to program code.

The ADSP-BF54x provides peripheral flexibility to complement its high performance processing. These rich system level peripherals are well-suited for industrial multimedia and automotive infotainment applications where multiple standards are prevalent and system performance is required.

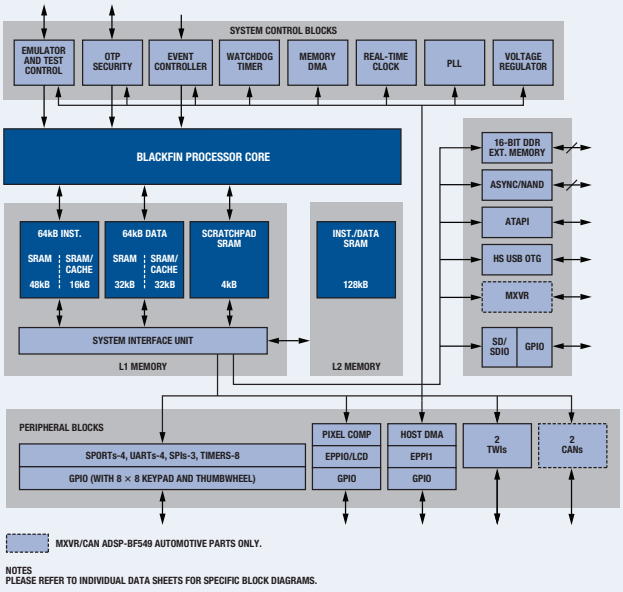
Features

- Powerful and flexible cache architecture suitable for soft real-time control tasks and industry-standard operating systems, plus hard real-time signal processing tasks
- Blackfin Processor core with up to 600 MHz (1200 MMACS) performance
- Lockbox secure technology
- Two independent DMA controllers
- Human interface: 18-/24-bit LCD controller, 32-bit up/down counter/thumbwheel interface, 8 × 8 keypad interface
- Connectivity: high speed USB on-the-go (OTG) controller, host DMA, UARTs, SPORTs, SPI, TWI, and CAN (not available on ADSP-547)
- Expansion: SD/SDIO and ATAPI controllers
- Multimedia: 18-/24-bit LCD controller, multiple enhanced parallel peripheral interfaces (EPPI), pixel compositor hardware accelerator, and Media Transceiver (MXVR [ADSP-BF549 only]) for connection to a MOST® Network
- Asynchronous memory interface for SRAM, EEPROM, NAND/NOR flash connectivity
- Synchronous memory interface for DDR/Mobile DDR connectivity
- Core voltage 0.8 V to 1.2 V

Applications

- Digital radio
- Audio jukebox
- Navigation
- Driver assistance
- Rear seat audio and video
- Advance vehicle infotainment
- Mobile communications
- Security and access control systems
- Industrial control and factory automation
- Automotive driver assistance/safety
- Telecommunications radio and switches
- Security and access control systems
- Factory/building automation
- Automotive multimedia device interconnect
- PC peripherals
- POS barcode scanners

ADSP-BF548/ADSP-BF549 BLOCK DIAGRAM



ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548/ADSP-BF549 Blackfin Processors

High Performance Convergent Multimedia Processors

Part Number[1]	Max (MHz)	Max (MMACS)	L1/L2 Memory (kB)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF542BBCZ-4A	400	800	132/—	400-CSP_BGA	Contact ADI
ADSP-BF542KBCZ-4A	400	800	132/—	400-CSP_BGA	
ADSP-BF542BBCZ-5A	533	1066	132/—	400-CSP_BGA	
ADSP-BF542KBCZ-6A	600	1200	132/—	400-CSP_BGA	
ADSP-BF544BBCZ-4A	400	800	132/64	400-CSP_BGA	
ADSP-BF544KBCZ-4A	400	800	132/—	400-CSP_BGA	
ADSP-BF544BBCZ-5A	533	1066	132/64	400-CSP_BGA	
ADSP-BF547BBCZ-5A	533	1066	132/128	400-CSP_BGA	
ADSP-BF547KBCZ-6A	600	1200	132/128	400-CSP_BGA	
ADSP-BF548BBCZ-5A	533	1066	132/128	400-CSP_BGA	
ADSP-BF548KBCZ-6A	600	1200	132/128	400-CSP_BGA	
ADSP-BF549BBCZ5A	533	1066	132/128	400-CSP_BGA	

NOTES

[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part

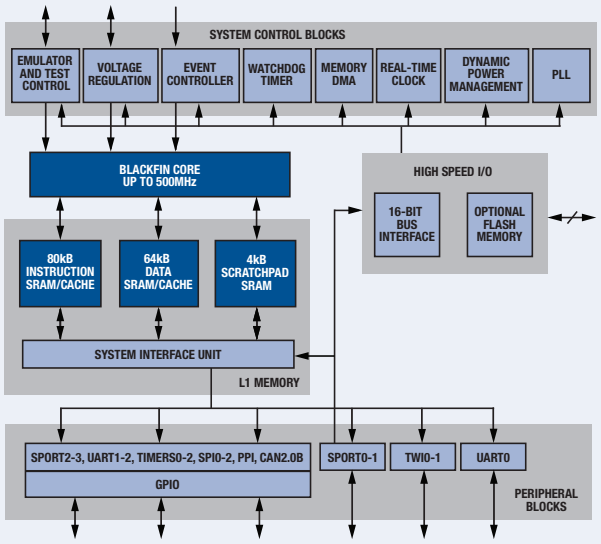
ADSP-BF538/ADSP-BF538F Blackfin Processors

Embedded and Integrated Development

The Blackfin Processor family has been expanded to address the ever increasing need for more connections possibilities with two new family members. This connectivity is coupled with the high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality. System designers can take advantage of the combined control and signal processing capabilities of the processor core across a wide range of end applications through code compatibility of these new family members with existing Blackfin offerings.

The ADSP-BF538 and ADSP-BF538F are functional extensions of the popular ADSP-BF533 processor, and they are ideally suited for applications with multiple device connections. The ADSP-BF538 offers equivalent embedded memory and is well-suited for applications such as video security/surveillance and industrial-environment-based distributed control/factory automation applications. The ADSP-BF538F is equivalent in functionality to the ADSP-BF538 processor with the addition of on-board flash memory. Both devices are ideally suited for a broad range of industrial, instrumentation, and medical appliance applications—allowing for broad connection possibilities coupled with a mix of control and signal processing needs based in the end product.

ADSP-BF538/ADSP-BF538F BLOCK DIAGRAM



Features

- Powerful and flexible cache architecture suitable for soft real-time control tasks and industry-standard operating systems, plus hard real-time signal processing tasks
- Addition of on-board flash memory for code storage of complex system application that run on a powerful 400 MHz or 500 MHz processor
- Applications-tuned peripherals provide glueless connectivity to general-purpose converters in data acquisition applications
- Enhanced dynamic power management with on-chip voltage regulation
- 10-stage RISC MCU/DSP pipeline with mixed 16-/32-bit ISA for optimal code density
- Full SIMD architecture, including instructions for accelerated video and image processing
- Memory Management Unit (MMU) supporting full memory protection for an isolated and secure environment
- More SPORT, UART, SPI, and TWI peripherals over the popular ADSP-BF533 processor
- Controller area network (CAN) 2.0B interface
- Enhanced DMA controller for high bandwidth throughput accommodating multiple peripherals
- 148 kB on-chip full-speed SRAM
- Glueless SDRAM, SRAM, and flash controllers
- On-board 512 kB or 1 MB of flash memory on ADSP-BF538F devices
- Glueless video capture/display port
- 316-ball, lead-free CSP_BGA package
- Core voltage 0.8 V to 1.2 V
- Industrial temperature range
- Multiple pin- and code-compatible derivatives

Applications

- Video security/surveillance
- Industrial
- Instrumentation
- Medical appliance

Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Flash Memory (Bytes)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF538BBCZ-4A	400	1000	148	—	316-CSP_BGA	15.84 to 20.42
ADSP-BF538BBCZ-4F4	400	1000	148	512k	316-CSP_BGA	
ADSP-BF538BBCZ-4F8	400	1000	148	1M	316-CSP_BGA	
ADSP-BF538BBCZ-5A	533	1006	148	—	316-CSP_BGA	
ADSP-BF538BBCZ-5F4	533	1006	148	512k	316-CSP_BGA	
ADSP-BF538BBCZ-5F8	533	1006	148	1M	316-CSP_BGA	

NOTES
[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

ADSP-BF536/ADSP-BF537 Blackfin Processors

Embedded Network Connectivity

The Blackfin Processor family has been expanded to address the ever increasing need for pervasive embedded network connectivity with two new family members. This connectivity is powerful when utilized in conjunction with the high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality. System designers can take advantage of the combined control and signal processing capabilities of the processor core across a wide range of end applications through the scalability of the pin and code compatibility of these new family members. The ADSP-BF536 and ADSP-BF537 are a functional extension of the popular ADSP-BF531, ADSP-BF532, and ADSP-BF533 processors, and they are ideally suited for a variety of networked applications.

Designed for Endpoint Connectivity

The Blackfin Processor core is ideally suited for handling both control-oriented networking tasks and user interface mechanisms while also offering full signal processing capabilities for analyzing almost any condition. To complement the performance, the Blackfin Processor's memory system offers a powerful and flexible cache architecture that can dynamically balance between the hard real-time tasks desired in SRAM, the soft real-time control tasks, and an operating system (OS) requiring cache functionality. DPM lowers power consumption for extending battery life or for minimizing power dissipation in enclosed applications.

Designed for Bandwidth

The ADSP-BF536/ADSP-BF537 processors integrate a fully compliant IEEE 802.3-2002 standard 10/100 Ethernet MAC that has been enhanced with advanced features to allow for higher network bandwidth capabilities. In addition, the DMA subsystem has been enhanced with greater traffic management abilities to allow for higher data throughput with minimal processor core intervention. The DMA subsystem also includes dual external handshake DMA request lines that when used in conjunction with the external bus interface unit (EBIU) can be used when a high speed interface is required for external FIFOs and high bandwidth communication peripherals, such as USB 2.0 devices. The ADSP-BF536/ADSP-BF537 processors also embed a controller area network (CAN) module and are capable of data rates of up to 1 Mbps.

Features

- Up to 600 MHz operation
- Embedded IEEE 802.3 2002 compliant 10/100 Ethernet MAC and buffered oscillator output to a separate PHY
- Controller area network (CAN) 2.0B interface
- I²C®-compatible 2-wire interface
- Enhanced DMA controller, including two external handshake DMA request lines
- Up to 132 kB on-chip, full-speed SRAM
- Glueless SDRAM, SRAM, and flash controllers
- Glueless video capture/display port
- 182-ball and 208-ball sparse CSP_BGA packages
- Lead-free and lead-bearing package options
- Industrial temperature ranges
- Core voltage 1.25 V to 1.3 V

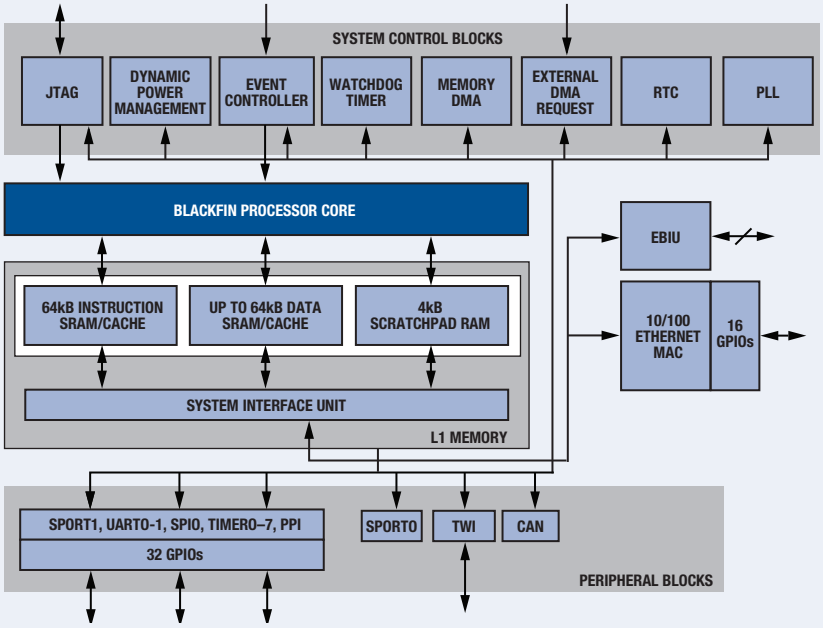
Applications

- Video security
- Video surveillance
- Industrial distributed control
- Industrial factory automation
- Remote monitoring devices
- Point-of-sale terminals
- VoIP
- Biometrics/security
- Instrumentation
- Medical
- Consumer appliances

ADSP-BF536/ADSP-BF537 Blackfin Processors

Embedded Network Connectivity

ADSP-BF536/ADSP-BF537 BLOCK DIAGRAM



Part Number	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-BF536BBC-3A	300	600	100	182-CSP_BGA	9.95 to 14.25
ADSP-BF536BBCZ-3A	300	600	100	182-CSP_BGA	
ADSP-BF536BBCZ-3B	300	600	100	208-CSP_BGA[2]	
ADSP-BF536BBC-4A	400	800	100	182-CSP_BGA	
ADSP-BF536BBCZ-4A	400	800	100	182-CSP_BGA	
ADSP-BF536BBCZ-4B	400	800	100	208-CSP_BGA[2]	
ADSP-BF537BBC-5A	500	1000	132	182-CSP_BGA	16.95 to 20.95
ADSP-BF537BBCZ-5A	500	1000	132	182-CSP_BGA	
ADSP-BF537BBCZ-5B	500	1000	132	208-CSP_BGA[2]	
ADSP-BF537BBCZ-5AV	533	1066	132	182-CSP_BGA	
ADSP-BF537BBCZ-5BV	533	1066	132	208-CSP_BGA[2]	
ADSP-BF537KBCZ-6AV	600	1200	132	182-CSP_BGA	
ADSP-BF537KBCZ-6BV	600	1200	132	208-CSP_BGA[2]	

NOTES

[1]All pricing is budgetary and subject to change.

[2]Sparse ball layout for easy PCB routing.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

ADSP-BF534 Blackfin Processor

CAN Connectivity for Automotive and Industrial Applications

The ADSP-BF534 is a functional extension of the popular ADSP-BF531, ADSP-BF532, and ADSP-BF533 processors and is ideally suited for a variety of CAN networked applications. The ADSP-BF534 offers a high performance series for embedded applications such as automotive safety, automotive body control, automotive driver assistance, automotive entertainment, and industrial factory automation. This processor is ideally suited for a broad range of industrial, instrumentation, medical applications, and fleet monitoring that allow for scalability and CAN network connectivity utilizing a mix of control plus signal processing in the end product.

Designed for Endpoint Connectivity

Embedded CAN networked applications require ever increasing intelligence and analytical capabilities for endpoint decision making. The Blackfin Processor core is ideally suited for handling both control-oriented networking tasks and user interface mechanisms while also offering full signal processing capabilities for analyzing almost any condition. To complement the performance, the Blackfin Processor's memory system offers a powerful and flexible cache architecture that can dynamically balance the hard real-time tasks desired in SRAM, the soft real-time control tasks, and an operating system (OS) requiring cache functionality. Dynamic power management (DPM) lowers power consumption for extending battery life or for minimizing power dissipation in enclosed applications. DPM allows for independent dynamic scaling of either voltage or frequency in a self-contained system with the integration of both a voltage regulator and PLL that are software programmable.

Designed for Bandwidth

The ADSP-BF534 integrates a fully compliant CAN 2.0B module capable of data rates of up to 1 Mbps. This module supports up to 32 mailboxes with individual acceptance masks and data filtering. In addition, the DMA subsystem has been enhanced with greater traffic management abilities to allow for higher data throughput with minimal processor core intervention. The DMA subsystem also includes dual external handshake DMA request lines that when used in conjunction with the External Bus Interface Unit (EBIU) can be used when a high speed interface is required for external FIFOs and high bandwidth communication peripherals, such as USB 2.0 devices.

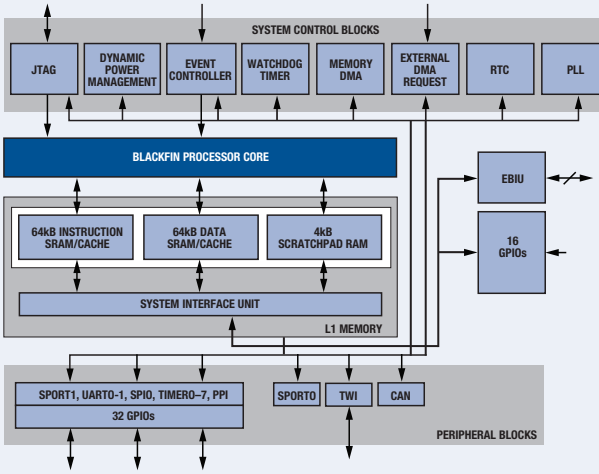
Features

- Up to 500 MHz operation
- Controller area network (CAN) 2.0B interface
- Enhanced DMA controller, including two external handshake DMA request lines
- 132 kB on-chip, full-speed SRAM
- Glueless SDRAM, SRAM, and flash controllers
- Glueless video capture/display port
- 8 timers supporting PWM and pulse width/event count modes
- 48 general-purpose I/Os, eight with high source/high sink capabilities
- 182-ball and 208-ball sparse CSP_BGA packages
- Lead-free and lead-bearing package options
- Industrial and extended industrial temperature ranges
- Core voltage 0.8 V to 1.2 V

Applications

- Automotive safety
- Automotive body control
- Automotive driver assistance
- Automotive entertainment
- Industrial factory automation
- Instrumentation
- Medical
- Consumer appliances

ADSP-BF534 BLOCK DIAGRAM



Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF534BBC-4A	400	800	132	182-CSP_BGA	12.25 to 16.73
ADSP-BF534BBCZ-4A	400	800	132	182-CSP_BGA	
ADSP-BF534BBCZ-4B	400	800	132	208-CSP_BGA[3]	
ADSP-BF534BBC-5A	500	1000	132	182-CSP_BGA	
ADSP-BF534BBCZ-5A	500	1000	132	182-CSP_BGA	
ADSP-BF534BBCZ-5B	500	1000	132	208-CSP_BGA[3]	

NOTES
[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.
[3]Sparse ball layout for easy PCB routing.
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

ADSP-BF561 Blackfin Processor

Symmetric Multiprocessing

Analog Devices has extended the Blackfin Processor family with the introduction of the ADSP-BF561 configured as a symmetric multiprocessing arrangement of two Blackfin Processor cores.

The ADSP-BF561 offers twice the signal processing performance of the ADSP-BF533, with twice the on-chip memory and significantly increased data bandwidth capability.

The ADSP-BF561 retains full code compatibility with the ADSP-BF533 and still maintains very low power consumption by using the dynamic power management capabilities of the Blackfin architecture.

The ADSP-BF561 integrates two Blackfin Processor cores, each capable of operating at up to 600 MHz and 2.6 Mb of on-chip SRAM memory. The on-chip memory is portioned between individual, high speed L1 memory for each core and a large 128 kB of shared L2 memory. Extremely high data bandwidth is provided by the 32-bit external port and dual 16-channel DMA controllers.

On-chip peripherals include dual parallel peripheral interfaces, each with support for ITU-R 656 video formatting and high speed serial ports supporting I²S formats. The product is optimized for a variety of consumer multimedia and other processing intensive applications.

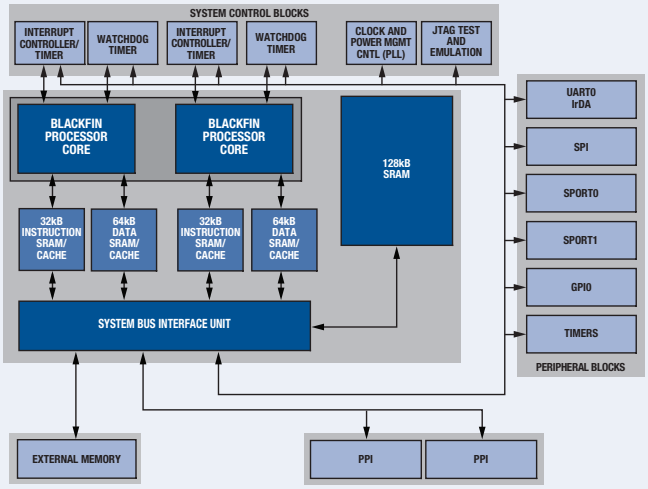
Features

- Dual Blackfin cores with each core capable of 600 MHz/ 1200 MMACS (2400 MMACS total)
- Large on-chip memory of 328 kB— arranged as individual L1 memory systems for each core, plus a shared L2 memory space
- High data throughput tailored for the needs of imaging and consumer multimedia applications
- Application-tuned peripherals provide glueless connectivity to a variety of audio/video converters and general-purpose ADCs/DACs
- Core voltage 0.8 V to 1.35 V

Applications

- Digital still cameras
- Digital video cameras
- Portable media players
- Digital video recorders
- Set-top boxes
- Consumer multimedia
- Automotive vision systems
- Broadband wireless systems
- Instrumentation
- Security and surveillance

ADSP-BF561 BLOCK DIAGRAM



Part Number[1]	Max (MHz)	Max (MMACS)	L1/L2 Memory (kB)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF561SBB500	500	2000	100[3]/128	297-PBGA	24.90 to 35.32
ADSP-BF561SBBZ500	500	2000	100[3]/128	297-PBGA	
ADSP-BF561SBBCZ-5A	500	2000	100[3]/128	256-CSP_BGA	
ADSP-BF561SKB500	500	2000	100[3]/128	256-CSP_BGA	
ADSP-BF561SKBZ500	500	2000	100[3]/128	256-CSP_BGA	
ADSP-BF561SKBCZ-5A	500	2000	100[3]/128	256-CSP_BGA	
ADSP-BF561SKBCZ-5V	533	2000	100[3]/128	256-CSP_BGA	
ADSP-BF561SBB600	600	2400	100[3]/128	297-PBGA	
ADSP-BF561SBBZ600	600	2400	100[3]/128	297-PBGA	
ADSP-BF561SBBCZ-6A	600	2400	100[3]/128	256-CSP_BGA	
ADSP-BF561SKB600	600	2400	100[3]/128	256-CSP_BGA	
ADSP-BF561SKBZ600	600	2400	100[3]/128	256-CSP_BGA	
ADSP-BF561SKBCZ-6A	600	2400	100[3]/128	256-CSP_BGA	
ADSP-BF561SKBCZ-6V	600	2400	100[3]/128	256-CSP_BGA	

NOTES
[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.
[3]Per core.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

ADSP-BF531/ADSP-BF532 Blackfin Processors

Low Power General-Purpose Applications

The ADSP-BF531 and ADSP-BF532 provide a low cost, power-efficient processor choice for today's most demanding convergent signal processing applications. With power consumption as low as 0.23 mW/MHz, and performance of 400 MHz, applications can now add greater signal processing performance without sacrificing battery life.

The high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem, and the dynamic power management (DPM) functionality allow system designers a flexible platform to address a wide range of applications including: consumer, communications, automotive, and industrial/instrumentation.

Designed for Performance and Power Efficiency

Both the ADSP-BF531 and the ADSP-BF532 offer 400 MHz performance and up to 800 MMACS. This processor core is supported by an advanced DMA controller supporting one- and two-dimensional DMA transfers between on-chip memory, off-chip memory, and system peripherals. The combination of the processor core speed and the DMA controller allows for efficient processing of audio, voice, video, and image data.

Blackfin Processors also offer enhanced power management capabilities by integrating on-chip core voltage regulation circuitry. This on-chip voltage regulator allows for the core and system clocks to be dynamically modified via a digital divider circuit, providing systems designers an additional tool for optimization of power and performance in their end products.

Designed for Flexibility

With multiple package and memory options, many pin for pin compatible, designers can choose the price point and cost point to meet their system requirements. Combined with a number of standard peripherals, including multifunction serial ports supporting I^2S audio capability, UART, SPI-compatible port, three multifunction timers, and a programmable parallel port (PPI) with ITU-656 video support, the ADSP-BF531/ADSP-BF532 can address a wide variety of existing and emerging applications.

Designed for Low Cost

Both the ADSP-BF531 and the ADSP-BF532 were designed for cost-sensitive applications. By efficiently processing both control and signal processing code on a single processor, the Blackfin architecture eliminates the additional cost of having a separate digital signal processor in the system. Each product offers LQFP package options to simplify board design, and peripherals like an on-chip real-time clock and voltage regulation to further reduce systems costs. The Blackfin Processor's combination of performance, flexibility, and low cost is ideally suited for the most demanding convergent processing applications.

This processor family, combined with ADI's investment in future Blackfin products, provides a robust platform for tomorrow's most challenging future convergent applications.

Features

- Performance to 400 MHz/800 MMACS enables multichannel audio plus CIF video processing in multimedia applications
- Enhanced dynamic power management with on-chip core voltage regulation allows operation to 0.8 V extending battery life in portable applications
- Application-tuned peripherals provide glueless connectivity to general-purpose converters in data acquisition applications
- Multiple low cost, pin- and code-compatible derivatives enable software differentiation in cost-sensitive consumer applications
- Pin compatible with the ADSP-BF533
- Core voltage 0.8 V to 1.3 V

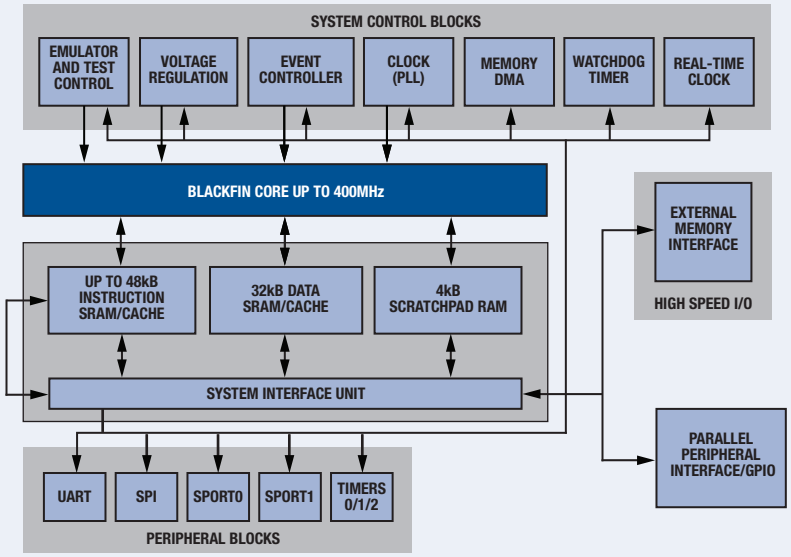
Applications

- Biometric systems
- Consumer audio
- Email terminals
- Embedded modems
- Games/learning aids
- Information appliances
- Industrial control
- Portable test equipment
- Web tablets/terminals
- Automotive telematics
- Consumer multimedia
- Digital and satellite radio
- Information appliances
- Point-of-sale terminals
- Medical instrumentation
- Professional audio
- Telephony and communications
- Video conferencing
- VoIP terminals

ADSP-BF531/ADSP-BF532 Blackfin Processors

Low Power General-Purpose Applications

ADSP-BF531/ADSP-BF532 BLOCK DIAGRAM



Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF531SBBC400	400	800	52	160-CSP_BGA	8.79 to 13.93
ADSP-BF531SBBCZ400	400	800	52	160-CSP_BGA	
ADSP-BF531SBST400	400	800	52	176-LQFP	
ADSP-BF531SBSTZ400	400	800	52	176-LQFP	
ADSP-BF531SBB400	400	800	52	169-PBGA	
ADSP-BF531SBBZ400	400	800	52	169-PBGA	
ADSP-BF532SBBC400	400	800	84	160-CSP_BGA	9.22 to 14.33
ADSP-BF532SBBCZ400	400	800	84	160-CSP_BGA	
ADSP-BF532SBST400	400	800	84	176-LQFP	
ADSP-BF532SBSTZ400	400	800	84	176-LQFP	
ADSP-BF532SBB400	400	800	84	169-PBGA	
ADSP-BF532SBBZ400	400	800	84	169-PBGA	

NOTES
[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

ADSP-BF533 Blackfin Processor

High Performance General-Purpose Applications

The ADSP-BF533 provides a high performance, power-efficient processor choice for today's most demanding convergent signal processing applications. With performance up to 756 MHz (1512 MMACS), applications can now add greater signal processing performance without significantly increasing their system cost. The high performance 16-/32-bit Blackfin embedded processor core, the flexible cache architecture, the enhanced DMA subsystem and the dynamic power management (DPM) functionality allow system designers a flexible platform to address a wide range of applications including consumer, communications, automotive, and industrial/instrumentation.

Designed for Performance

The ADSP-BF533 combines the high performance Blackfin core with a large on-chip Level 1 cacheable instruction and data memories. This combination allows the ADSP-BF533 to achieve very high system performance for applications such as video or multimedia. This processor core is supported by an advanced DMA controller aiding one- and two-dimensional DMA transfers between on-chip memory, off-chip memory, and system peripherals. Blackfin Processors also offer enhanced power management capabilities by integrating on-chip core voltage regulation circuitry. This on-chip voltage regulator allows for the core and system clocks to be dynamically modified via a digital divider circuit, providing systems designers an additional tool for optimization of power and performance in their end products.

Designed for Flexibility

With multiple package and memory options, designers can choose the price point and cost point to meet their system requirements. Combined with a number of standard peripherals, including multifunction serial ports supporting I²S audio capability, UART, SPI-compatible port, three multifunction timers, and a programmable parallel port (PPI) with ITU-656 video support, the ADSP-BF533 can address a wide variety of existing and emerging applications. Also, the ADSP-BF533 is code compatible with all of the Blackfin family of processors, providing more choices and offering greater leverage across developments. The Blackfin Processor's combination of performance and flexibility is ideally suited for the most demanding convergent processing applications. This processor family, combined with Analog Devices' investment in future Blackfin products, provides a robust platform for tomorrow's most challenging convergent applications.

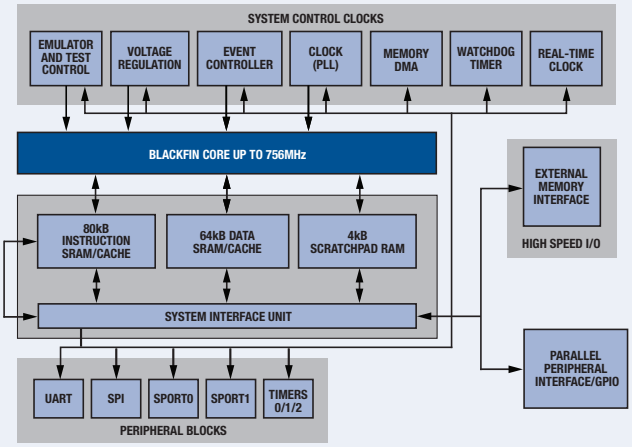
Features

- Up to 756 MHz performance
- 1512 MMACS
- Application-tuned peripherals provide glueless connectivity to general-purpose converters in data acquisition applications
- Large on-chip SRAM for maximum system performance
- Pin for pin compatible with the ADSP-BF531/ADSP-BF532 for scalable solutions
- Core voltage 0.8 V to 1.3 V

Applications

- Multimedia
- Home audio/video
- Embedded modems
- Instrumentation
- Imaging
- Industrial control
- Voice communication

ADSP-BF533 BLOCK DIAGRAM



Part Number[1]	Max (MHz)	Max (MMACS)	L1 Memory (kB)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-BF533SBBZ400	400	800	148	169-PBGA	12.05 to 21.95
ADSP-BF533SBST400	400	800	148	176-LQFP	
ADSP-BF533SBSTZ400	400	800	148	176-LQFP	
ADSP-BF533SBBCZ400	400	800	148	160-CSP_BGA	
ADSP-BF533SBBC500	500	1000	148	160-CSP_BGA	
ADSP-BF533SBBCZ500	500	1000	148	160-CSP_BGA	
ADSP-BF533SBB500	500	1000	148	169-PBGA	
ADSP-BF533SBBZ500	500	1000	148	169-PBGA	
ADSP-BF533SBBC-5V	533	1066	148	160-CSP_BGA	
ADSP-BF533SBBCZ-5V	533	1066	148	160-CSP_BGA	
ADSP-BF533SKBC-6V	600	1200	148	160-CSP_BGA	
ADSP-BF533SKBCZ-6V	600	1200	148	160-CSP_BGA	
ADSP-BF533SKBC750	750	1500	148	160-CSP_BGA	Contact ADI

NOTES
[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

ADSP-BF535 Blackfin Processor

High Performance Processor for Internet Appliances

The ADSP-BF535 high performance processor features dual MACs, high clock rates, and dynamic power management, allowing for optimization of system performance and power consumption. Additionally, through the advantages of a clean, orthogonal RISC instruction set, the ADSP-BF535 is optimized for programming in high level languages (HLL) like C/C++, resulting in extremely dense code.

At the heart of the Blackfin Processor is ADI's most advanced 16-bit digital signal processing core architecture. This new core has three primary objectives—performance, power management, and ease of use.

High Performance

Blackfin Processors employ a dual-MAC processor that also includes efficient RISC MCU system control functionality and multimedia processing capabilities. All are combined into one simple, optimized instruction set architecture.

Dynamic Power Management

Blackfin Processor's dynamic power management offers a flexible, software controlled environment that delivers the required amount of performance to the processor via independent, dynamic variation of both voltage and frequency. Blackfin Processors also employ a gated clock scheme and multiple power-down modes for minimal power consumption.

Ease of Use

Blackfin Processors employ both an optimized compiler and architecture to support software development in HLL, for example, C/C++, thus delivering code densities comparable to those of traditional microcontrollers. The architecture also has embedded features to support efficient use of a real-time operating system (RTOS).

Features

- Up to 350 MHz/700 MMACS
- 16-bit dual-MAC processor core
- Flexible, software controlled dynamic power management
- Enhanced media instructions for audio, image, and video multimedia applications
- Integrated system peripherals, including USB device, PCI, serial ports, UARTs, SPI, and timers
- Core voltage 1.0 V to 1.6 V

Blackfin Processors Utilize:

- Single processor core
- Single instruction set
- Single programming model
- Single set of development tools

Applications

- Automotive applications
- Broadband home gateways
- Central office/network switch
- Digital imaging and printing
- Global positioning systems
- Home networking/wireless LAN
- Internet appliances
- Modem solutions
- PDAs and other portable handheld devices
- Video conferencing
- VoIP phone solutions
- Personal branch exchanges (PBX)
- Point-of-sale terminals
- Telecommunications

Part Number	Max (MHz)	Max (MMACS)	L1/L2 Memory (kB)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-BF535PKB-350	350	700	52/256	260-PBGA	30.00 to 45.38
ADSP-BF535PKBZ-350	350	700	52/256	260-PBGA	
ADSP-BF535PBB-300	300	600	52/256	260-PBGA	
ADSP-BF535PKB-300	300	600	52/256	260-PBGA	
ADSP-BF535PKBZ-300	300	600	52/256	260-PBGA	
ADSP-BF535PBB-200	200	400	52/256	260-PBGA	
ADSP-BF535PBBZ-200	200	400	52/256	260-PBGA	

NOTES

[1]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

SHARC Processor Family

Leadership in Floating-Point Applications

Analog Devices 32-bit floating-point SHARC Processors are based on a Super Harvard Architecture that balances exceptional core and memory performance with outstanding I/O throughput capabilities. This Super Harvard Architecture extends the original concepts of separate program and data memory buses by adding an I/O processor with its associated dedicated buses. In addition to satisfying the demands of the most computationally intensive, real-time signal processing applications, SHARC Processors integrate large memory arrays and application-specific peripherals designed to simplify product development and reduce time to market.

The SHARC Processor portfolio currently consists of three generations of products providing code-compatible solutions ranging from entry-level to the high performance products offering fixed- and floating-point computational power. All SHARC Processors provide a common set of features and functionality usable across many signal processing markets and applications, allowing designers an easy transition to the newest products with the latest features and the highest performance.

First Generation

First-generation SHARC Processors offer performance to 66 MHz/198 MFLOPS. Their easy to use instruction set architecture supports both 32-bit fixed-point and 32-/40-bit floating-point data formats combined with large memory arrays, and sophisticated communications ports make them suitable for a wide array of parallel processing applications, including consumer audio, medical imaging, military, industrial, and instrumentation.

Second Generation

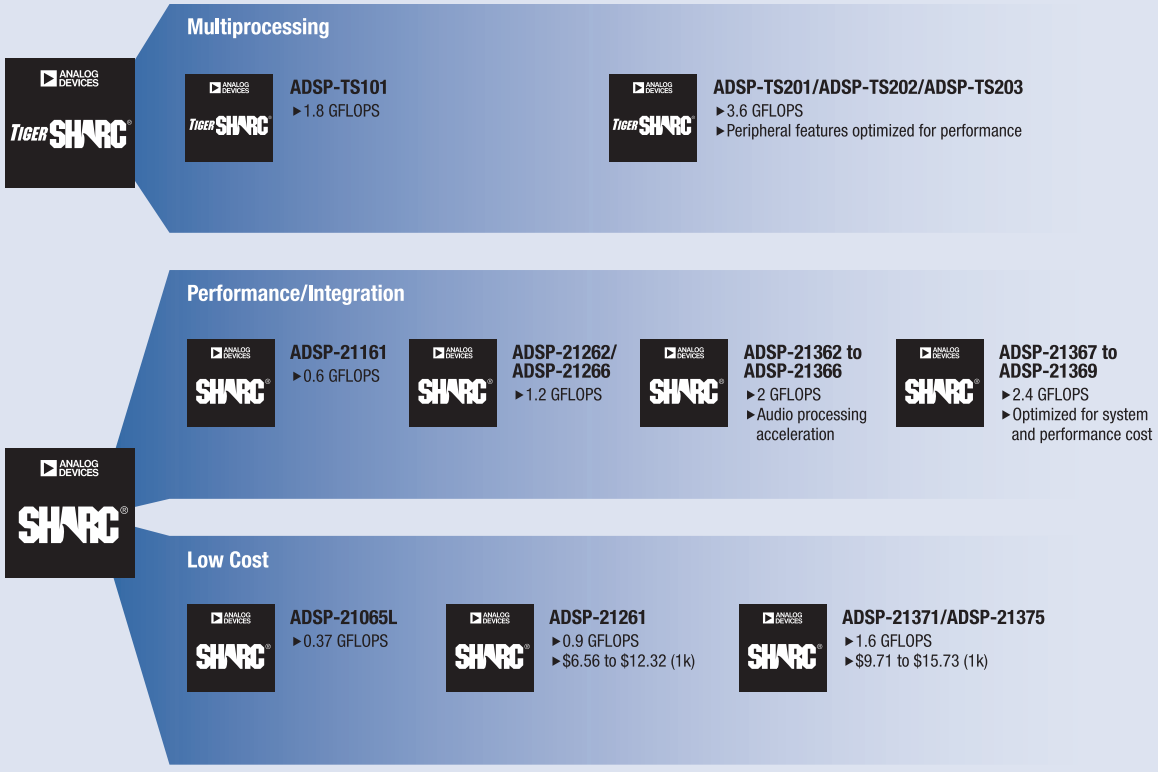
Second-generation SHARC Processors double the level of signal processing performance (100 MHz/600 MFLOPS) by utilizing a single-instruction, multiple-data (SIMD) architecture. This hardware extension doubles the number of computational resources available to the system programmer. Second-generation products contain dual multipliers, ALUs, shifters, and data register files—significantly increasing overall system performance. This capability is especially relevant in consumer, automotive, and professional audio applications where the algorithms related to multichannel processing can effectively utilize the SIMD architecture.

Third Generation

Third-generation SHARC Processors are based on an enhanced SIMD architecture, which extends core performance to an industry-leading 400 MHz/2.4 GFLOPS. Third-generation SHARC Audio Processors feature the highest level of integrated on-chip peripherals, such as multichannel audio surround sound decoders and postprocessing algorithms, S/PDIF transmitter/receiver, high performance asynchronous sample-rate conversion, PWM channels, code security, and DTCP cipher for protection of digital data in automobiles.

All SHARC Processors are code-compatible with previous generations of SHARC Processors, so legacy code is easily ported to the newer products. In addition, a number of third-generation processors are also pin compatible for use with a single hardware platform.

Floating-Point Roadmap



SHARC Processor Family

Leadership in Floating-Point Applications

All SHARC Processors are code-compatible with previous generations of SHARC Processors, so legacy code is easily ported to the newer products. In addition, a number of third-generation processors are also pin compatible for use with a single hardware platform.

- Home theater applications—The ADSP-21266, ADSP-21365, ADSP-21363, and ADSP-21367 permit highly efficient software implementations of audio decode and postprocessing algorithms, such as Dolby® Digital, Dolby Digital EX, DTS-ES Discrete 6.1, DTS-ES Matrix 6.1, DTS 96/24™ 5.1, DTS-HD, DTS Express, MPEG-2 AAC LC, MPEG-2 BC 2ch, Dolby Pro Logic II, Dolby Pro Logic 2x, Dolby True HD, DTS Neo:6, DDPlus DCV, Neural Audio, Audyssey room equalization, and WMA Pro. Libraries of all standard—and many proprietary—audio algorithms reside in on-chip ROM, eliminating the need for external ROM.
- Professional audio applications—A number of the third-generation SHARC Processors are well-suited for professional audio applications requiring high processing power and advanced on-chip peripherals such as sample rate conversion, S/PDIF transmitter/receiver, and BGA and LQFP package options.
- Automotive audio applications—The ADSP-2136x, with integration of sample-rate conversion, DTCP cipher, precision clock generators, and serial ports, is an ideal choice for new multichannel automotive audio designs.
- Broad market use—SHARC Processors are available in commercial, industrial, and automotive temperature grade packages. They are used in a wide variety of signal processing applications, providing up to 400 MHz performance in a single instruction, multiple data architecture (SIMD).

The combination of a high performance core surrounded by appropriate peripherals, a large software library, and award-winning CROSSCORE development tools makes the third-generation SHARC Processors the ideal choice for audio and broad market processor applications.

SHARC Melody Platform

Analog Devices' SHARC Melody platform brings the highest quality audio processing available to audio receivers based on the premium performance of the third-generation SHARC Processors. The SHARC Melody with floating-point capability provides the highest quality platform on which to build high fidelity audio decoders, and are now widely available in home theater systems designed by a range of leading global brands. These programmable DSP-based platforms ensure that end equipment is always up to date and able to support the newest standards as soon as content is available.

Music enthusiasts love the quality of their living room surround sound systems. These audiophiles want that experience in their cars, necessitating a variety of audio-spatializer algorithms and equalizer functions that can be developed on SHARC Melody platforms. For mid-range systems required in cars, Analog Devices also offers a SigmaDSP that integrates 24-bit DSP functionality with very high performance digital-to-analog converters to make an integrated, customizable equalizer.

ADI also offers a wide range of audio codec and amplifier components, plus software to support in-car music playing and recording.

ADSP-21371/ADSP-21375 SHARC Processors

High Performance 32-Bit Floating-Point Processors

The ADSP-21371 and the ADSP-21375 are the latest offerings in the SHARC Processor family and provide the highest MFLOP/$ performance for a variety of applications. Both the ADSP-21371 and the ADSP-21375 devices are pin compatible and code compatible with prior SHARC Processors such as the ADSP-21367 and ADSP-21369. These latest members of the SHARC Processor family are based on a single-instruction, multiple-data (SIMD) core, which supports both 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats, making them particularly suitable for cost optimized high precision applications.

The ADSP-2137x SHARC Processors also integrate many peripherals designed to simplify hardware design, minimize system design risks, and reduce end-customer time to market. Grouped together, and broadly named the digital applications interface (DAI), these functional blocks may be connected to each other or to external pins via the software-programmable signal routing unit (SRU). The SRU is an innovative architectural feature that enables complete and flexible routing amongst DAI blocks. Peripherals connected through the SRU include, but are not limited to, serial port and SPI port blocks.

The ADSP-21375 provides up to 266 MHz core clock performance with 0.5 Mb on-chip SRAM and four serial ports. The ADSP-21371 provides the same maximum core clock frequency with 1.0 Mb on-chip SRAM and eight serial ports.

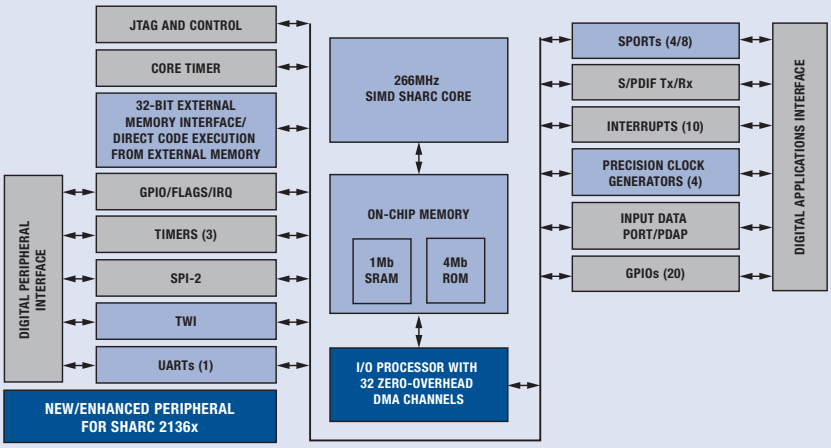
Features

- 266 MHz SIMD SHARC core, capable of 1596 MFLOPS peak performance
- 0.5 Mb or 1.0 Mb SRAM
- 24 zero-overhead DMA channels
- Digital applications interface (DAI) enabling user-definable access to peripherals
- 4 or 8 serial ports (SPORTs) supporting I²S, left justified sample pair, and TDM modes
- 2 SPI-compatible ports supporting master and slave modes
- 1 UART
- 1 TWI
- 2 full-featured timers
- 208-lead LQFP E_Pad package
- Commercial temperature ranges
- Core voltage 1.2 V

Applications

- Professional audio
- Medical applications
- Industrial and instrumentation

ADSP-21371 BLOCK DIAGRAM



Part Number	Max (MHz)	On-Chip Memory SRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21371BSWZ-2B	266	1	208-LQFP E_Pad	13.11 to 15.73
ADSP-21371KSWZ-2B	266	1	208-LQFP E_Pad	
ADSP-21375BSWZ-2B	266	0.5	208-LQFP E_Pad	9.71 to 11.65
ADSP-21375KSWZ-2B	266	0.5	208-LQFP E_Pad	

NOTES
[1]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to 85°C ambient).
Z = RoHS compliant part.

ADSP-21367/ADSP-21368/ADSP-21369 SHARC Processors

Industry-Leading Performance for Floating-Point Applications

The ADSP-21367/ADSP-21368/ADSP-21369 are Analog Devices' highest performance SHARC Processors. At up to 400 MHz/2.4 GFLOPS, these newest processors deliver superior performance and a high degree of functional integration. These floating-point SHARC Processors are designed to simplify audio product development, reduce time to market, and reduce product costs for a variety of applications, including multichannel A/V receivers, professional mixing consoles, and digital synthesizers. Using these new SHARC Processors, manufacturers can create differentiated products for their customers more quickly, more easily, and more cost-effectively than ever before.

With its 6 Mb on-chip ROM factory-programmed with industry-standard audio decoders and postprocessor algorithms from Dolby,® DTS,® Microsoft,® and SRS, the ADSP-21367 is the industry's highest performance audio processor available today.

The 400 MHz ADSP-21368 adds shared memory capabilities, making it an ideal choice for professional audio applications and other processing intensive applications.

The ADSP-21369 provides high performance signal processing with audio and broad market peripherals as well as a 32-bit external memory interface supporting SRAM, SDRAM, flash, and ROM memory. Along with the ADSP-21367 and ADSP-21368, the ADSP-21369 supports both 16-bit and 32-bit SDRAM at speeds up to 166 MHz. The ADSP-21369 is well-suited to address the needs of professional audio applications and other applications where high performance processing is essential.

Features

- 400 MHz/2.4 GFLOPS SIMD SHARC core supporting 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 2 Mb SRAM, 6 Mb factory-programmed ROM (ADSP-21367 only)
- 32-bit external memory interface supports SDRAM, SRAM, flash, and ROM memory
- 8-channel, asynchronous samples rate conversion based on the AD1896
- S/PDIF transmitter and receiver
- 8 serial ports
- 2 precision clock generators
- 20 lines of digital I/O port
- 4 timers, UART, I^2C-compatible interface
- ROM/JTAG security mode
- Available in 256-ball SBGA, 208-lead LQFP E_Pad, and 208-lead MQFP package options
- Available in commercial and industrial temperature grades
- Core voltage 1.2 V to 1.3 V

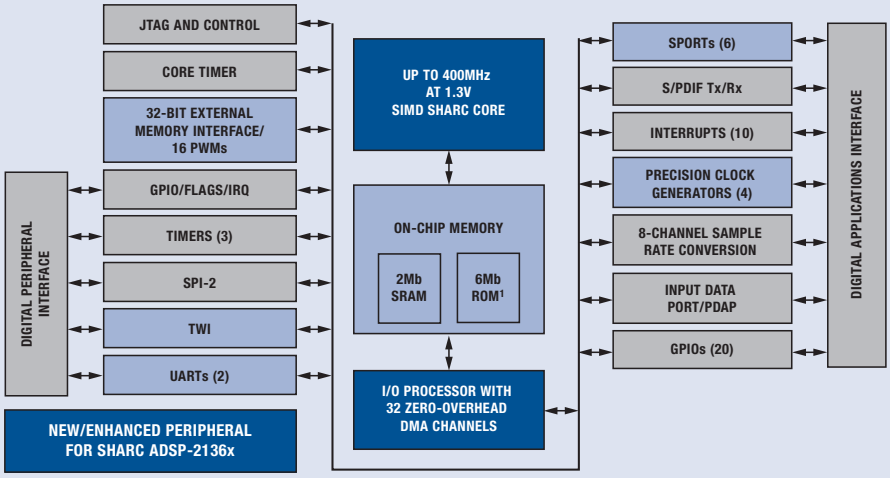
Applications

- Consumer A/V receivers
- Home theater systems
- Professional audio equipment
- Industrial and instrumentation

ADSP-21367/ADSP-21368/ADSP-21369 SHARC Processors

Industry-Leading Performance for Floating-Point Applications

ADSP-21368/ADSP-21369 BLOCK DIAGRAM



[1]FOR CONS. APPLICATIONS

Part Number	Max (MHz)	On-Chip Memory SRAM/ROM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21367BBP-2A	333	2/6	256-SBGA	20.48 to 37.54
ADSP-21367BBPZ-2A	333	2/6	256-SBGA	
ADSP-21367BSWZ-1A	266	2/6	208-LQFP E_Pad	
ADSP-21367KBP-2A	333	2/6	256-SBGA	
ADSP-21367KBPZ-2A	333	2/6	256-SBGA	
ADSP-21367KBPZ-3A	400	2/6	256-SBGA	
ADSP-21368BBP-2A	333	2/6	256-SBGA	30.67 to 44.99
ADSP-21368BBPZ-2A	333	2/6	256-SBGA	
ADSP-21368KBP-2A	333	2/6	256-SBGA	
ADSP-21368KBPZ-2A	333	2/6	256-SBGA	
ADSP-21368KBPZ-3A	400	2/6	256-SBGA	
ADSP-21369BBP-2A	333	2/6	256-SBGA	19.46 to 35.67
ADSP-21369BBPZ-2A	333	2/6	256-SBGA	
ADSP-21369BSWZ-1A	266	2/6	208-LQFP E_Pad	
ADSP-21369KBP-2A	333	2/6	256-SBGA	
ADSP-21369KBPZ-2A	333	2/6	256-SBGA	
ADSP-21369KBPZ-3A	400	2/6	256-SBGA	

NOTES
[1]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

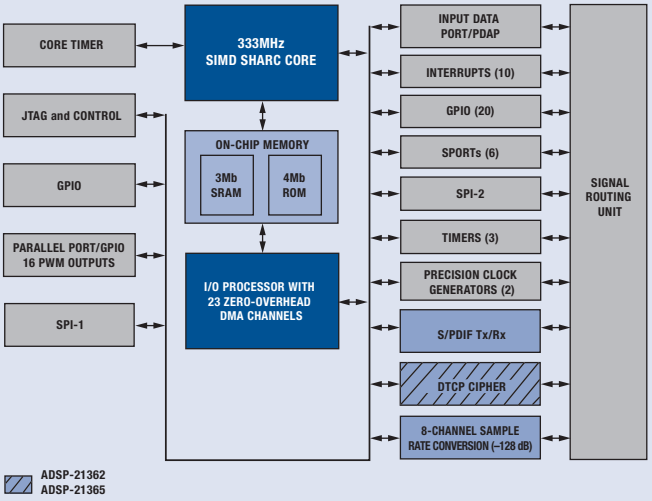
Customers must be current licensees of Dolby and DTS to obtain samples or purchase the ADSP-21367.

ADSP-21362/ADSP-21365/ADSP-21366 SHARC Processors

333 MHz Performance for Automotive Audio and Home Theater

The ADSP-21362/ADSP-21365/ADSP-21366 are particularly well-suited to address the increasing requirements of the professional and automotive audio and home theater market segments. In addition to their higher core performance, the ADSP-21362/ADSP-21365/ADSP-21366 include additional peripherals such as 16-bit parallel ports, an S/PDIF transmitter/receiver, an 8-channel asynchronous sample rate converter, and a hardware Digital Transmission Content Protection (DTCP) encryption/decryption block (ADSP-21362 and ADSP-21365 only).

ADSP-21362/ADSP-21365/ADSP-21366 BLOCK DIAGRAM



Features

- 333 MHz/2 GFLOPS SIMD SHARC core supporting IEEE 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 3 Mb SRAM; 4 Mb ROM embedded with the latest industry-standard audio decode and postprocessing algorithms
- 25 zero-overhead DMA channels
- Digital applications interface (DAI) enabling user-definable access to peripherals, including an S/PDIF Tx/Rx, 8-channel asynchronous sample rate converter, and Digital Transmission Content Protection hardware accelerator
- 6 serial ports (SPORTs) supporting I²S, left justified sample pair, and TDM modes
- 2 SPI-compatible ports supporting master and slave modes
- 16 pulse-width modulation (PWM) channels
- 3 full-featured timers
- PLL capable of 1× to 32× frequency multiplication
- 16-bit parallel port
- Core voltage 1.2 V

Applications

- Automotive audio
- Consumer home theater
- Digital audio amplifiers
- Professional audio

Part Number[1]	Max (MHz)	On-Chip Memory SRAM/ROM (Mb)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-21362BBCZ-1AA	333	3/4	136-CSP_BGA	26.80 to 32.16
ADSP-21362BSWZ-1AA	333	3/4	144-LQFP E_Pad	
ADSP-21362YSWZ-2AA	200	3/4	144-LQFP E_Pad	
ADSP-21365BBCZ-1AA	333	3/4	136-CSP_BGA	28.21 to 33.85
ADSP-21365BSWZ-1AA	333	3/4	144-LQFP E_Pad	
ADSP-21365YSWZ-2AA	200	3/4	144-LQFP E_Pad	
ADSP-21365YSWZ-2CA	200	3/4	144-LQFP E_Pad	
ADSP-21366BBCZ-1AA	333	3/4	136-CSP_BGA	22.33 to 32.16
ADSP-21366KBCZ-1AA	333	3/4	136-CSP_BGA	
ADSP-21366BSWZ-1AA	333	3/4	144-LQFP E_Pad	
ADSP-21366KSWZ-1AA	333	3/4	144-LQFP E_Pad	
ADSP-21366YSWZ-2AA	200	3/4	144-LQFP E_Pad	

NOTES
[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Y = automotive temperature (–40°C to +105°C ambient).
Z = RoHS compliant part.

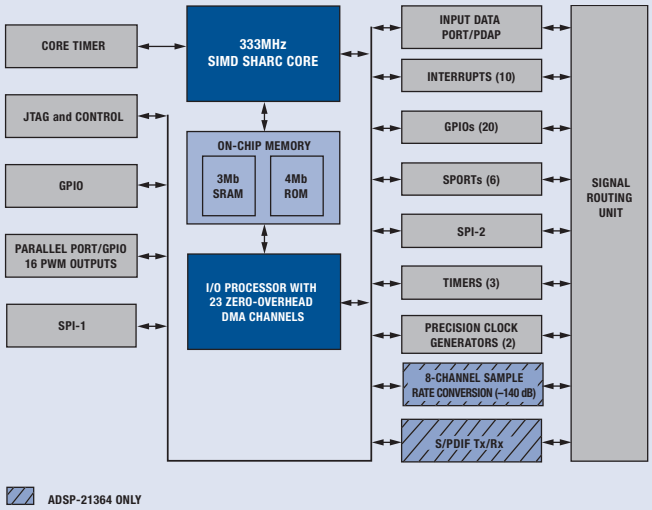
Customers must be current licensees of DTLA to obtain samples of the ADSP-21362.
Customers must be current licensees of Dolby, DTS, and DTLA to obtain samples or purchase the ADSP-21365.
Customers must be current licensees of Dolby and DTS to obtain samples or purchase the ADSP-21366.

ADSP-21363/ADSP-21364 SHARC Processors

333 MHz Performance for Broad Market Applications

The ADSP-21363/ADSP-21364 provide superior performance—333 MHz/2 GFLOPS—within the third-generation SHARC Processor family. This level of performance makes the ADSP-21363/ADSP-21364 particularly well-suited to address the increasing requirements of a broad range of applications. High core performance, combined with audiocentric peripherals, including a high precision, 8-channel asynchronous sample rate converter and 16-bit parallel port, makes the ADSP-21363/ADSP-21364 an excellent choice.

ADSP-21363/ADSP-21364 BLOCK DIAGRAM



Features

- 333 MHz/2 GFLOPS SIMD SHARC core supporting IEEE 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 3 Mb SRAM, 4 Mb ROM
- 23 zero-overhead DMA channels
- High precision, 8-channel asynchronous sample rate converter based on the award-winning AD1896
- Digital applications interface (DAI) enabling user-definable access to peripherals, including an input data port (IDP) and general-purpose I/O
- 6 serial ports (SPORTs) supporting I²S, left justified sample pair, and TDM modes
- 2 SPI-compatible ports supporting master and slave modes
- 16 pulse-width modulation (PWM) channels
- 3 full-featured timers
- PLL capable of 1× to 32× frequency multiplication
- 16-bit parallel port
- Core voltage 1.2 V

Applications

- Automotive audio
- Consumer home theater
- Digital audio amplifiers
- Professional audio

Part Number[1]	Max (MHz)	On-Chip Memory SRAM/ROM (Mb)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-21363KBCZ-1AA	333	3/4	136-CSP_BGA	19.98 to 28.78
ADSP-21363KSWZ-1AA	333	3/4	144-LQFP E_Pad	
ADSP-21363KBC-1AA	333	3/4	136-CSP_BGA	
ADSP-21363BBC-1AA	333	3/4	136-CSP_BGA	
ADSP-21363BBCZ-1AA	333	3/4	136-CSP_BGA	
ADSP-21363BSWZ-1AA	333	3/4	144-LQFP E_Pad	
ADSP-21363YSWZ-2AA	200	3/4	144-LQFP E_Pad	
ADSP-21364KBCZ-1AA	333	3/4	136-CSP_BGA	29.40 to 42.34
ADSP-21364KSWZ-1AA	333	3/4	144-LQFP E_Pad	
ADSP-21364KBC-1AA	333	3/4	136-CSP_BGA	
ADSP-21364BBC-1AA	333	3/4	136-CSP_BGA	
ADSP-21364BBCZ-1AA	333	3/4	136-CSP_BGA	
ADSP-21364BSWZ-1AA	333	3/4	144-LQFP E_Pad	
ADSP-21364YSWZ-2AA	200	3/4	144-LQFP E_Pad	

NOTES
[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Y = automotive temperature (–40°C to +105°C ambient).
Z = RoHS compliant part.

ADSP-21266 SHARC Processor

32-Bit Floating-Point Processor for Home Theater

The ADSP-21266 is a third-generation SHARC Processor optimized for consumer audio applications. This processor offers the same features as the ADSP-21262, with the additions of factory programmed ROM to contain the latest multichannel audio decoders from Dolby and DTS.

The ADSP-21266 is code compatible with all prior SHARC Processors and pin compatible with third-generation processors. The ADSP-21266 is based on a SIMD core, which supports both 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats, making them particularly suitable for high performance consumer audio applications, such as home theater systems and A/V receiver systems.

SHARC Melody Platform

The SHARC Melody platform combines high performance processors with optimized software, offering complete audio solutions to home theater manufacturers.

The ADSP-21266 is a large memory, high performance device targeted primarily at mid- to high-end home theater systems. SHARC Melody solutions are offered through on-chip ROM containing industry-standard audio decoder algorithms such as:

- PCM
- Dolby Digital
- Dolby Digital EX2
- Dolby Pro Logic® IIx
- DTS 5.1
- DTS ES®
- DTS Neo:6™ (cinema and music)
- DTS 96/24
- MPEG-2 AAC LC
- MPEG-2 (BC) 2 channel
- WMA Pro v7.1

Features

- 200 MHz (5 ns) SIMD SHARC core, capable of 1.2 GFLOPS
- Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 2 Mb SRAM; 4 Mb ROM embedded with industry-standard audio decode and postprocessing algorithms
- 16-bit parallel port
- 22 zero-overhead DMA channels
- Digital applications interface (DAI) enables user-definable access to peripherals, including precision clock generators, IDP, and general-purpose I/O
- 6 serial ports (SPORTs) supporting I²S, left justified sample pair, and TDM modes
- SPI-compatible, port-supporting master and slave modes
- 3 full-featured timers
- Software PLL capable of a variety of multiplier ratios
- 136-ball CSP_BGA (12 mm × 12 mm) and 144-lead LQFP (20 mm × 20 mm) packages
- Industrial grade BGA available
- Core voltage 1.2 V

Applications

- Consumer home theater
- Professional audio
- Automotive audio

Part Number	Max (MHz)	On-Chip Memory SRAM/SROM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21266SKSTZ-1B	150	2/4	144-LQFP	14.24 to 17.80
ADSP-21266SKSTZ-2B	200	2/4	144-LQFP	
ADSP-21266SKBCZ-2B	200	2/4	136-CSP_BGA	
ADSP-21266SKSTZ-1C	150	2/4	144-LQFP	
ADSP-21266SKSTZ-2C	200	2/4	144-LQFP	
ADSP-21266SKBCZ-2C	200	2/4	136-CSP_BGA	
ADSP-21266SKSTZ-1D	150	2/4	144-LQFP	
ADSP-21266SKSTZ-2D	200	2/4	144-LQFP	

NOTES
[1]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
Z = RoHS compliant part.

Customers must be current licensees of Dolby and DTS to obtain samples or purchase the ADSP-21266.

ADSP-21262 SHARC Processor

200 MHz Low Cost, 32-/40-Bit Floating-Point Processor

The ADSP-21262 is a third-generation SHARC programmable digital signal processor operating at up to 200 MHz. The design of the ADSP-21262 is based on a SIMD architecture that efficiently supports execution of 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats.

With its SIMD core operating at 200 MHz (a 5 ns instruction cycle time), the processor actually operates at up to 400 MMACS/1200 MFLOPS. With such a high bandwidth core, the ADSP-21262 is capable of executing 1024-point complex FFT in just 46 μs. This is more than 2.6 times faster than comparatively priced processors and provides optimal performance in audio as well as in broad market processor applications.

Digital Applications Interface (DAI) for Simplified I/O System Development

The ADSP-21262 introduces the DAI, an architecture that enables complete software programmability of various peripherals. The flexibility and ease of use of the SHARC programming model, combined with the DAI, allow manufacturers to deploy one hardware configuration into multiple product offerings with different I/O requirements.

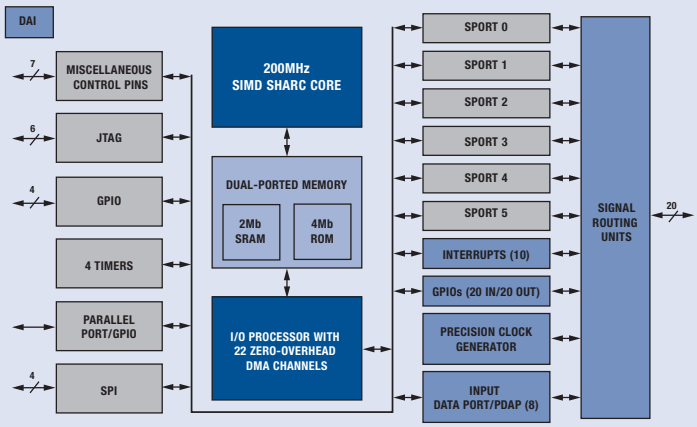
Applications

- Professional audio
- Consumer A/V receivers
- Automotive audio
- Medical appliances
- Voice recognition
- Test and measurement equipment
- Telephony
- Wireless communications

Features

- 200 MHz (5 ns) SIMD SHARC core, capable of 1.2 GFLOPS
- Code compatible with all SHARC Processors
- Pin compatible with all SHARC ADSP-2126x and ADSP-2136x Processors
- Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 2 Mb on-chip, dual-ported SRAM
- 2.4 GBps on-chip bandwidth
- 22 zero-overhead DMA channels
- 6 independent serial ports—supports standard DSP serial, I²S, left justified sample pair, and TDM modes
- SPI-compatible interface and a 16-bit parallel port
- Digital applications interface (DAI)
- 4 timers: 1 core and 3 general-purpose
- 136-ball CSP_BGA (12 mm ×12 mm) and 144-lead LQFP (20 mm × 20 mm) packages available in commercial and industrial temperature ranges
- Core voltage 1.2 V

ADSP-21262 BLOCK DIAGRAM



Part Number[1]	Max (MHz)	On-Chip Memory SRAM/SROM (Mb)	Package	Price Range @ 1k ($U.S.)[2]
ADSP-21262SKBCZ200	200	2/4	136-CSP_BGA	16.95 to 23.85
ADSP-21262SKBC-200	200	2/4	136-CSP_BGA	
ADSP-21262SKSTZ200	200	2/4	144-LQFP	
ADSP-21262SBBCZ150	150	2/4	136-CSP_BGA	
ADSP-21262SBBC-150	150	2/4	136-CSP_BGA	

NOTES
[1]Certain models available in automotive grade temperature range.
[2]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 70°C ambient).
B = industrial temperature (–40°C to +85°C ambient).
Z = RoHS compliant part.

ADSP-21261 SHARC Processor

150 MHz Low Cost, 32-Bit Floating-Point Processor

The ADSP-21261 is the lowest cost member of the third-generation of SHARC programmable digital signal processors. It is based on the SIMD SHARC core that supports execution of 32-bit fixed-point and 32-/40-bit floating-point arithmetic formats.

With its core running at 150 MHz (6.67 ns instruction cycle time), the ADSP-21261 is capable of executing 1024-point complex FFT operations in 61 μs. The processor's single-instruction, multiple-data (SIMD) mode effectively doubles the processor performance.

The ADSP-21261 is designed with a high level of functional integration, including 1 Mb of on-chip, dual-ported SRAM, which enables sustained processor and I/O performance without the need for external memory. System I/O is achieved through four full-duplex serial ports, four timers, a 16-bit parallel port, a serial peripheral interface (SPI), 18 zero-overhead direct memory access (DMA) channels delivering fast data transfers without processor intervention, and an innovative digital applications interface (DAI), which provides the user complete software control through its signal routing unit (SRU).

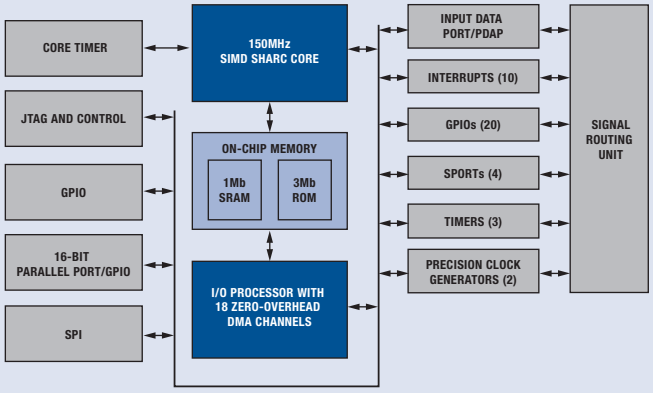
Applications

- Medical appliances
- Test and measurement equipment
- Voice recognition
- Professional audio
- Consumer A/V receivers
- Automotive audio
- Telephony
- Wireless communications

Features

- 150 MHz (6.67 ns) SIMD SHARC core, capable of 900 MFLOPS peak performance
- Code compatible with all SHARC Processors
- Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point data types
- 1 Mb on-chip, dual-ported SRAM
- 18 zero-overhead DMA channels
- 4 independent serial ports that support standard DSP serial mode, I²S mode, left justified sample-pair mode, and TDM mode
- SPI-compatible interface and a 16-bit parallel port
- Digital applications interface (DAI)
- Software configurable PLL providing many possible multiplier ratios
- 4 timers: 1 core and 3 general-purpose
- 136-ball CSP_BGA (12 mm × 12 mm) and 144-lead LQFP (20 mm × 20 mm) packages available in commercial temperature range
- Core voltage 1.2 V

ADSP-21261 BLOCK DIAGRAM



Part Number	Max (MHz)	On-Chip Memory SRAM/SROM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21261SKBC-150	150	1/3	136-CSP_BGA	7.22 to 12.32
ADSP-21261SKBCZ150	150	1/3	136-CSP_BGA	
ADSP-21261SKSTZ150	150	1/3	144-LQFP	

NOTES
[1]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 85°C case).
Z = RoHS compliant part.

ADSP-21161N SHARC Processor

100 MHz Low Cost, 32-Bit Processor

The 32-bit floating-point programmable ADSP-21161N processor is based on a SIMD SHARC architecture and is optimized for single processor and small multiprocessor systems.

The ADSP-21161N core operates at up to 100 MHz and is capable of 600 MFLOPS. The core is supported by 12 GPIO flags, SPI ports, and serial ports, and it supports external SDRAM and SBSRAM, which make the ADSP-21161N an excellent choice for audio and broad market multiprocessing applications.

Benefits

- Cluster multiprocessing and two 100 MBps link ports simplify connection and communication for multiprocessing
- SDRAM controller improves large DRAM bank throughput
- Four serial ports allow 16 channels of data to be transferred in/out of the processor

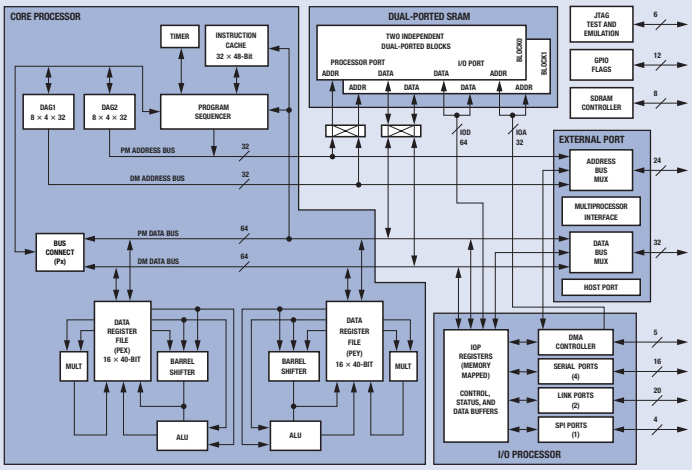
Features

- 100 MHz (10 ns) SIMD SHARC Processor core
- 600 MFLOPS (32-bit floating-point data), 600 MOPS (32-bit fixed-point data)
- Code compatible with ADSP-21x6x SHARC Processors
- Supports IEEE-compatible 32-bit floating-point, 40-bit floating-point, and 32-bit fixed-point math
- Single-cycle instruction execution, including SIMD operations in both computational units
- 1 Mb on-chip, dual-ported SRAM
- 2.4 GBps on-chip data bandwidth
- 14 zero-overhead DMA channels
- 4 synchronous serial ports with I²S support
- Serial ports support 128-channel TDM frames with selection of companding on a per channel basis
- Integrated support for SDRAM and SBSRAM external memories
- Support for single-cycle, 100 MHz instruction execution from 48-bit wide external memories
- Core voltage 1.8 V

Applications

- Speech recognition
- Professional and high end consumer audio
- Automotive entertainment
- Fingerprint recognition
- Digital audio broadcast
- Wireless communications
- Motor control
- Global positioning systems
- Medical equipment
- Telephony
- Test equipment

ADSP-21161N BLOCK DIAGRAM



Part Number	Max (MHz)	On-Chip Memory SRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21161NCCA-100	100	1	225-CSP_BGA	25.86 to 34.13
ADSP-21161NKCA-100	100	1	225-CSP_BGA	
ADSP-21161NCCAZ100	100	1	225-CSP_BGA	
ADSP-21161NKCAZ100	100	1	225-CSP_BGA	

NOTES

[1]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 85°C case).
C = industrial temperature (–40°C to +105°C case).
Z = RoHS compliant part.

www.analog.com/sharc

ADSP-21160 SHARC Processor

100 MHz 32-Bit Processor for Multiprocessing Applications

The ADSP-21160 family introduces single-instruction, multiple-data (SIMD) processing to the SHARC Processor family. While maintaining code compatibility with previous SHARC family members, the SIMD architecture provides up to a 2× increase in performance on a cycle-by-cycle basis. Like all SHARC Processors, the ADSP-21160 offers native support of 32-bit fixed-point and 32-/40-bit floating-point data types.

Designed specifically for multiprocessing applications, the ADSP-21160 offers a balanced architecture with 600 MFLOPS core performance, 4 Mb on-chip SRAM, zero-overhead DMAs, large I/O bandwidth, and multiprocessing support through cluster and link port interfaces.

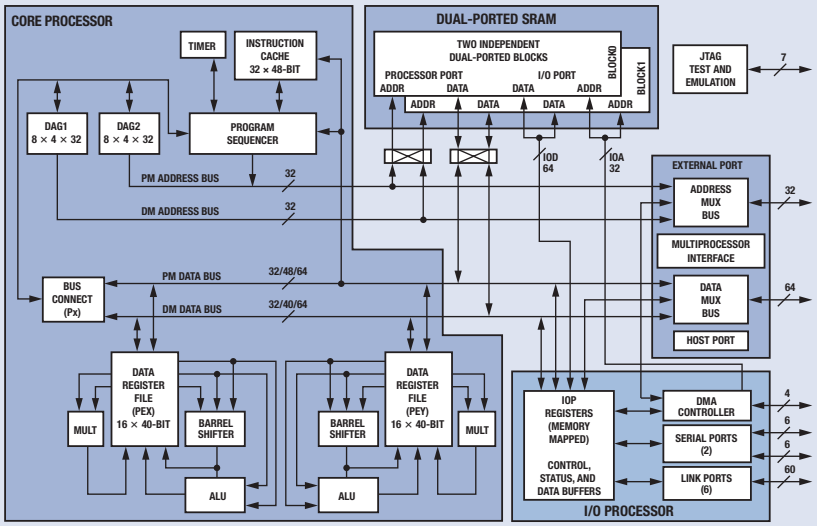
Applications

- Audio
- Medical
- Military
- 3D graphics
- Imaging
- Communications

Features

- Glueless clusters of up to 6 SHARCs
- Link ports for 2D and 3D arrays
- Distributed bus arbitration
- Unified memory space
- Link ports provide up to 80 MBps I/O each
- 320 MBps external port
- Hardware support for semaphores
- 100 MHz (10.5 ns) core instruction rate
- Single-cycle instruction execution, including SIMD operations in both computational units
- 570 MFLOPS peak and 380 MFLOPS sustained performance (based on FIR)
- Dual data address generators (DAGs) with modulo and bit-reverse addressing
- 4 Mb dual-ported SRAM
- Zero-overhead looping and single-cycle loop setup, providing efficient program sequencing
- IEEE 1149.1 JTAG standard test access port and on-chip emulation
- Core voltage 1.8 V to 2.5 V

ADSP-21160 BLOCK DIAGRAM



Part Number	Max (MHz)	On-Chip Memory SRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21160MKB-80	80	4	400-PBGA	167.48 to 184.22
ADSP-21160MKBZ-80	80	4	400-PBGA	
ADSP-21160NCB-100	100	4	400-PBGA	167.48 to 196.93
ADSP-21160NCBZ-100	100	4	400-PBGA	
ADSP-21160NKB-100	100	4	400-PBGA	
ADSP-21160NKBZ-100	100	4	400-PBGA	

NOTES

[1]All pricing is budgetary and subject to change.

K = commercial temperature (0°C to 85°C case).
C = industrial temperature (–40°C to +100°C case).
Z = RoHS compliant part.

ADSP-21065L SHARC Processor

32-Bit Processor

The ADSP-21065L is a broad market, programmable 32-bit SHARC Processor that allows users to program with equal efficiency in both fixed-point and floating-point arithmetic. This programming flexibility, combined with the high performance core and integrated peripherals, make the ADSP-21065L an outstanding price/performance value for a broad base of consumer, communications, automotive, industrial, and computer applications.

The ADSP-21065L is code compatible with the ADI SHARC Processor family, and as such, customers have immediate access to software and hardware development tools from ADI and SHARC third parties.

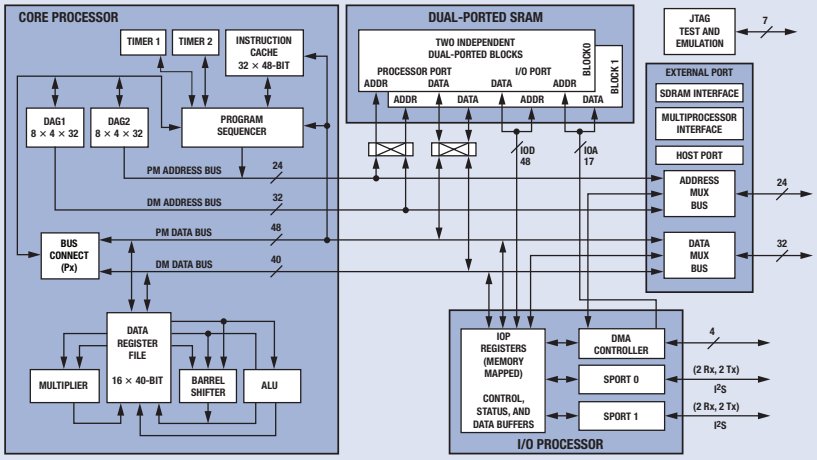
Applications

- Keyless entry using voice analysis/recognition
- Barcode scanners
- Imaging
- Ultrasound equipment
- Digital oscilloscopes
- Fingerprint recognition
- Professional audio
- Automotive audio
- Consumer audio

Features

- 544 kb configurable, dual-ported, on-chip memory
- 64M × 32-bit word external address space
- 198 MFLOPS (32-bit floating-point)
- 198 MOPS (32-bit fixed-point)
- Glueless SDRAM interface
- 2 serial transmit/receive ports support 32-channel TDM
- I^2S mode supports up to 16 channels
- 2 timers with event capture and PWM options
- 12 programmable I/O pins
- 10 DMA channels
- Glueless multiprocessing with 2 ADSP-21065Ls
- Code compatible with all SHARC Processors
- 208-lead MQFP, 196-ball CSP_BGA packages
- Core voltage 3.3 V

ADSP-21065L BLOCK DIAGRAM



Part Number	Max (MHz)	On-Chip Memory SRAM (kb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-21065LKS-240	60	544	208-MQFP	22.58 to 65.84
ADSP-21065LKSZ-240	60	544	208-MQFP	
ADSP-21065LKS-264	66	544	208-MQFP	
ADSP-21065LKSZ-264	66	544	208-MQFP	
ADSP-21065LKCA-240	60	544	196-CSP_BGA	
ADSP-21065LKCAZ-240	60	544	196-CSP_BGA	
ADSP-21065LKCA-264	66	544	196-CSP_BGA	
ADSP-21065LKCAZ-264	66	544	196-CSP_BGA	
ADSP-21065LCS-240	60	544	208-MQFP	
ADSP-21065LCSZ-240	60	544	208-MQFP	
ADSP-21065LCCA-240	60	544	196-CSP_BGA	
ADSP-21065LCCAZ-240	60	544	196-CSP_BGA	

NOTES
[1]All pricing is budgetary and subject to change.

L = indicates 3.3 V operation.
K = commercial temperature (0°C to 85°C case).
C = industrial temperature (–40°C to +100°C case).
Z = RoHS compliant part.

TigerSHARC Processor Family

Highest Performance Processor for Multiprocessor Systems

The TigerSHARC Processor family offers the industry's highest performance per watt and per square inch of board space for the most demanding signal and image processing applications. Its patented link port technology allows glueless interprocessor communication within arrays of two or more TigerSHARC Processors, delivering unbounded performance in terms of MMACS and MFLOPS.

Based on a 128-bit static superscalar architecture, TigerSHARC Processors offer native support of fixed- and floating-point data types and a balanced combination of computational performance, I/O bandwidth, and memory integration. Together, this yields sustained DSP system-level performance that is two to four times greater than conventional DSPs or microprocessors with vector processing units.

By providing native support for 1-bit data formats used for chip-rate processing, TigerSHARC pioneers a new class of software-defined radios and serves applications that were previously the exclusive domain of expensive ASICs (application-specific integrated circuits) and FPGAs (field-programmable gate arrays). And by moving to a software-centric design model, TigerSHARC Processors allow IP reuse, which greatly enhances R&D productivity throughout each successive product generation.

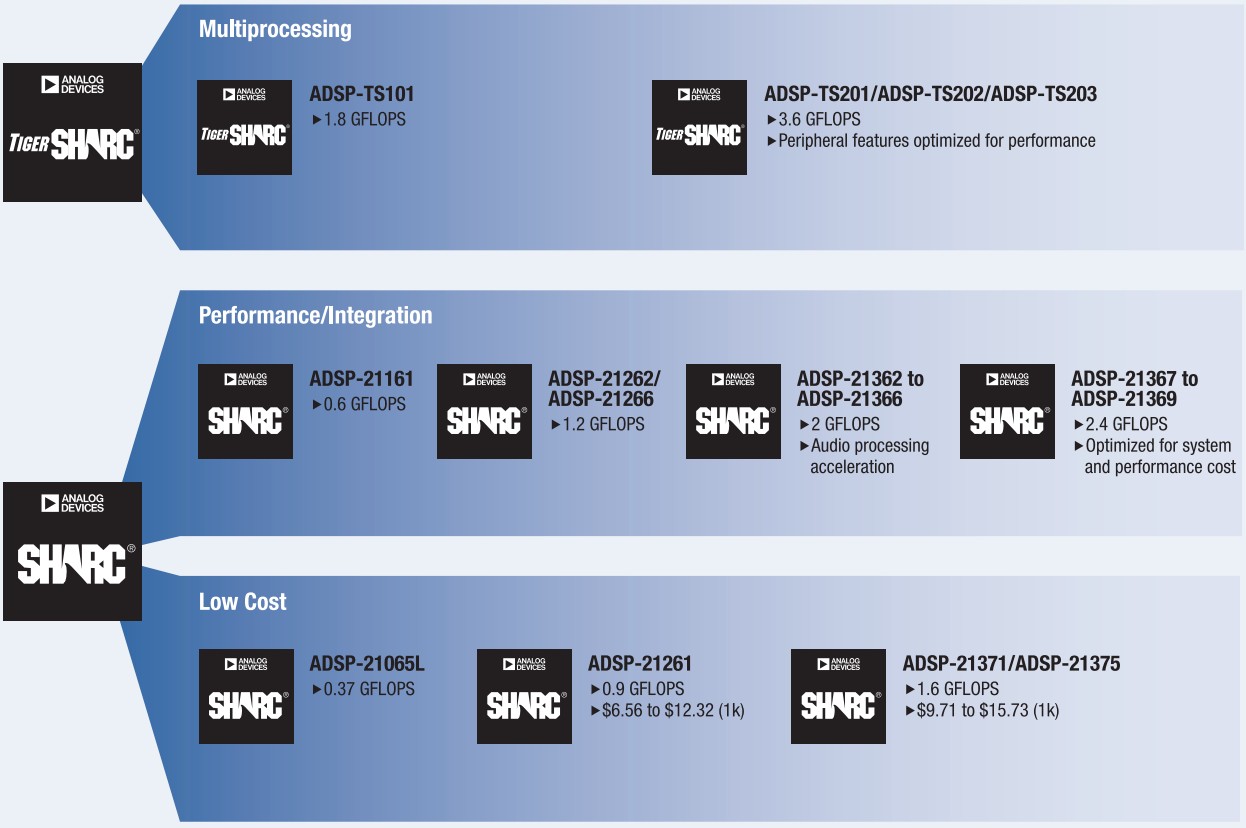
The TigerSHARC Processors provide a broad range of price and performance points to meet the needs of many different applications. The ADSP-TS201S is offered at 500 MHz and 600 MHz with 24 Mb of on-chip memory, while the ADSP-TS202S and ADSP-TS203S are offered at 500 MHz with 12 Mb and 4 Mb of on-chip memory, respectively.

Soft Baseband Platform

The TigerSHARC Processor supports the massive signal processing and memory demands of communications baseband modem implementations. It is the first general-purpose processor capable of homogeneous, low cost, flexible, and scalable baseband implementations without the use of external ASICs or memory, and does not require an internal hardware accelerator.

The TigerSHARC Processor is designed specifically to handle all of the demands of a various baseband implementation from a MIPS, memory, and I/O perspective. This enables a compact, homogeneous implementation with a simple control interface that is flexible, scalable, and low cost.

Floating-Point Roadmap



ADSP-TS203S TigerSHARC Processor

500 MHz Processor with 4 Mb On-Chip DRAM

The ADSP-TS203S TigerSHARC Processor is targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally intensive, real-time functions. The TigerSHARC Processor is well-suited to video applications as well as defense, medical imaging, and industrial instrumentation.

The ADSP-TS203S features a static superscalar architecture that combines RISC, VLIW, and standard DSP functionality. Native support of fixed- and floating-point data types, coupled with leading-edge multiprocessing capabilities, allows the TigerSHARC Processor to offer unrivaled performance. At a 500 MHz clock rate, the ADSP-TS203S offers the industry's highest 16-bit fixed-point and 32-bit floating-point performance. The ADSP-TS203S has a 32-bit floating-point 1024-point complex FFT time of 18.8 μs and provides 1000 MFLOPS per watt.

ADSP-TS203S Performance

- 500 MHz, 2 ns instruction rate processor core
- Executes eight 16-bit MACs with 40-bit accumulation per cycle or two 32-bit MACs with 80-bit accumulation per cycle
- Executes six single-precision floating-point, or twenty-four 16-bit fixed-point, operations per cycle (3.0 GFLOPS or 12.0 GOPS performance)
- 2-cycle, interlocked execution pipe
- Parallelism allows the execution of up to four 32-bit instructions per cycle

Features

- Static superscalar architecture that supports 1-, 8-, 16-, and 32-bit fixed-point as well as floating-point data processing
- High performance 500 MHz, 2 ns instruction rate processor core
- 4 Mb on-chip embedded DRAM internally organized in six banks with user-defined partitioning
- 10-channel, zero-overhead DMA controller
- 4 internal 128-bit wide internal buses providing a total memory bandwidth of 32 GBps
- Single-instruction, multiple-data (SIMD) operation supported by two computation blocks, each with an ALU, multiplier, shifter, and 32-word register file
- 2 LVDS link ports with each operating up to 250 MBps per direction for serial interfacing
- 32-bit cluster bus with operation up to 500 MBps for parallel interfacing
- Assembly and C language programmability
- Core voltage 1.05 V

Applications

- Video
- Medical imaging
- Industrial instrumentation
- Military

Part Number	Max (MHz)	On-Chip Memory DRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-TS203SABP-050	500	4	576-PBGA	177.00 to 194.70
ADSP-TS203SABPZ050	500	4	576-PBGA	

NOTES
[1]All pricing is budgetary and subject to change.

A = industrial temperature (–40°C to +85°C case).
Z = RoHS compliant part.

ADSP-TS202S TigerSHARC Processor

500 MHz Processor with 12 Mb On-Chip DRAM

The ADSP-TS202S TigerSHARC Processor is targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally intensive, real-time functions. The TigerSHARC Processor is well-suited to video and communication applications as well as defense, medical imaging, and industrial instrumentation.

The ADSP-TS202S features a static superscalar architecture that combines RISC, VLIW, and standard DSP functionality. Native support of fixed- and floating-point data types, coupled with leading-edge multiprocessing capabilities, allows the TigerSHARC Processor to offer unrivaled performance. At a 500 MHz clock rate, the ADSP-TS202S offers the industry's highest 16-bit fixed-point and 32-bit floating-point performance. The ADSP-TS202S has a 32-bit floating-point 1024-point complex FFT time of 18.8 μs and provides 1000 MFLOPS per watt.

ADSP-TS202S Performance

- 500 MHz, 2 ns instruction rate processor core
- Executes eight 16-bit MACs with 40-bit accumulation per cycle or two 32-bit MACs with 80-bit accumulation per cycle
- Executes six single-precision floating-point, or twenty-four 16-bit fixed-point, operations per cycle (3.0 GFLOPS or 12.0 GOPS performance)
- 2-cycle, interlocked execution pipe
- Parallelism allows the execution of up to four 32-bit instructions per cycle

Features

- Static superscalar architecture that supports 1-, 8-, 16-, and 32-bit fixed-point as well as floating-point data processing
- High performance 500 MHz, 2 ns instruction rate processor core
- 12 Mb on-chip embedded DRAM internally organized in six banks with user-defined partitioning
- 14-channel, zero-overhead DMA controller
- 4 internal 128-bit wide internal buses, providing a total memory bandwidth of 32.0 GBps
- SIMD operation supported by two computation blocks, each with an ALU, multiplier, shifter, and 32-word register file
- 4 LVDS link ports with each operating up to 500 MBps per direction for serial interfacing
- Configurable cluster bus (32- or 64-bit) with operation up to 1 GBps for parallel interfacing
- Assembly and C language programmability
- Core voltage 1.05 V

Applications

- Communications
- Video
- Medical imaging
- Industrial and instrumentation
- Military

Part Number	Max (MHz)	On-Chip Memory DRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-TS202SABP-050	500	12	576-PBGA	201.00 to 221.10
ADSP-TS202SABPZ050	500	12	576-PBGA	

NOTES
[1]All pricing is budgetary and subject to change.

A = industrial temperature (–40°C to +85°C case).
Z = RoHS compliant part.

ADSP-TS201S TigerSHARC Processor

600 MHz Processor with 24 Mb On-Chip DRAM

The ADSP-TS201S is targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally intensive, real-time functions. The TigerSHARC Processor is well-suited to video and communication markets, including the 3G cellular and broadband wireless base stations, as well as defense, medical imaging, and industrial instrumentation.

The ADSP-TS201S features a static superscalar architecture that combines RISC, VLIW, and standard DSP functionality. Native support of fixed- and floating-point data types, coupled with leading-edge multiprocessing capabilities, allows the TigerSHARC Processor to offer unrivaled performance. At a 600 MHz clock rate, the ADSP-TS201S offers the industry's highest 16-bit fixed-point and 32-bit floating-point performance. The ADSP-TS201S has a 32-bit floating-point 1024-point complex FFT time of 15.7 μs and provides 1000 MFLOPS per watt.

ADSP-TS201S Performance

- Executes eight 16-bit MACs with 40-bit accumulation per cycle or two 32-bit MACs with 80-bit accumulation per cycle
- Executes six single-precision floating-point, or twenty-four 16-bit fixed-point, operations per cycle (3.6 GFLOPS or 14.4 GOPS)
- 2-cycle, interlocked execution pipe
- Parallelism allows the execution of up to four 32-bit instructions per cycle

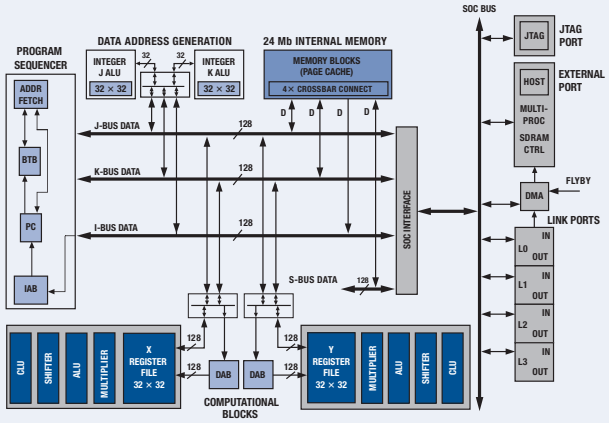
Applications

- Wireless infrastructure
- Performance driven embedded applications
  - Military hardware
  - Medical equipment
  - Industrial instrumentation
  - Software-defined radios

Features

- Static superscalar architecture that supports 1-, 8-, 16-, and 32-bit fixed-point as well as floating-point data processing
- High performance 600 MHz, 1.67 ns instruction rate processor core
- 24 Mb on-chip embedded DRAM internally organized in six banks with user-defined partitioning
- 14-channel, zero-overhead DMA controller
- Enhanced communications instruction set for wireless infrastructure applications allows for the TigerSHARC Processor to offer complete baseband processing
- 4 internal 128-bit wide internal buses, providing a total memory bandwidth of 38.4 GBps
- Software radio approach allows for the adoption of a single platform for multiple wireless telecommunication standards
- SIMD operation supported by two computation blocks each with an ALU, multiplier, shifter, and 32-word register file
- 4 LVDS link ports with each operating up to 500 MBps per direction for serial interfacing
- Configurable cluster bus (32- or 64-bit) with operation up to 1 GBps for parallel interfacing
- Assembly and C language programmability
- Core voltage 1.05 V (500 MHz) or 1.2 V (600 MHz)

ADSP-TS201S BLOCK DIAGRAM



Part Number	Max (MHz)	On-Chip Memory DRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-TS201SABP-050	500	24	576-PBGA	242.00 to 319.44
ADSP-TS201SABPZ050	500	24	576-PBGA	
ADSP-TS201SABP-060	600	24	576-PBGA	
ADSP-TS201SABPZ060	600	24	576-PBGA	
ADSP-TS201SYBP-050	500	24	576-PBGA	
ADSP-TS201SYBPZ050	500	24	576-PBGA	

NOTES

[1]All pricing is budgetary and subject to change.

A = industrial temperature (–40°C to +85°C case).
Y = automotive temperature (–40°C to +105°C case).
Z = RoHS compliant part.

ADSP-TS101S TigerSHARC Processor

300 MHz Processor with 6 Mb On-Chip SRAM

The ADSP-TS101S is the first member of the TigerSHARC Processor family. It is targeted at numerous signal processing applications that rely on multiple processors working together to execute computationally intensive, real-time functions.

The ADSP-TS101S features a static superscalar architecture that combines RISC, VLIW, and standard DSP functionality. Native support of fixed- and floating-point data types, coupled with leading-edge multiprocessing capabilities, allows the TigerSHARC Processor to offer unrivaled performance. At a 300 MHz clock rate, the ADSP-TS101S offers the 16-bit fixed-point performance and a 32-bit floating-point 1024-point complex FFT time of 32.5 μs, and 1000 MFLOPS per watt.

ADSP-TS101S Performance

- Executes eight 16-bit MACs with 40-bit accumulation per cycle or two 32-bit MACs with 80-bit accumulation per cycle
- Executes six single-precision floating-point, or twenty-four 16-bit fixed-point, operations per cycle (1800 MFLOPS or 7.2 GOPS performance)
- Parallelism allows the execution of up to four 32-bit instructions per cycle

Applications

- Wireless infrastructure
- Medical, CT, ultrasound
- Sonar and radar systems
- Flight simulators
- Infrastructure equipment
- Military smart munitions
- Test equipment
- Imaging, printers
- Wireless broadband access
- Industrial applications

Features

- Static superscalar architecture supports 1-, 8-, 16-, and 32-bit fixed-point as well as floating-point data processing
- SIMD operation supported by two computation blocks, each with an ALU, multiplier, shifter, and 32-word register file
- Assembly and C language programmability
- Up to 300 MHz, 3.3 ns instruction rate processor core
- 6 Mb on-chip SRAM internally organized in three banks with user-defined partitioning
- 14-channel, zero-overhead DMA controller
- 4 LVTLL link ports operating up to 250 MBps for serial interfacing
- Configurable cluster bus (32- or 64-bit) with operation up to 800 MBps for parallel interfacing
- Enhanced communications instruction set for wireless infrastructure applications for complete baseband processing
- 3 internal 128-bit wide internal buses, providing a total memory bandwidth of 14.4 GBps
- Software radio approach allows for the adoption of a single platform for multiple wireless telecommunication standards
- Core voltage 1.2 V

Part Number	Max (MHz)	On-Chip Memory SRAM (Mb)	Package	Price Range @ 1k ($U.S.)[1]
ADSP-TS101SAB1-000	250	6	625-PBGA	186.00 to 244.20
ADSP-TS101SAB1Z000	250	6	625-PBGA	
ADSP-TS101SAB2-000	250	6	484-PBGA	
ADSP-TS101SAB2Z000	250	6	484-PBGA	
ADSP-TS101SAB1-100	300	6	625-PBGA	
ADSP-TS101SAB1Z100	300	6	625-PBGA	
ADSP-TS101SAB2-100	300	6	484-PBGA	
ADSP-TS101SAB2Z100	300	6	484-PBGA	

NOTES

[1]All pricing is budgetary and subject to change.

A = industrial temperature (–40°C to +85°C case).
Z = RoHS compliant part.

Literature Guide

Title	Where to Order	Publication Number
Embedded Processing and DSP Technical Documentation CD	www.analog.com/processors	CD05962-2.5-10/07(B)
Blackfin Processor Data Sheets		
ADSP-BF522/ADSP-BF523/ADSP-BF524/ADSP-BF525/ADSP-BF526/ADSP-BF527	www.analog.com/processors	Preliminary
ADSP-BF522C/ADSP-BF523C/ADSP-BF524C/ADSP-BF525C/ADSP-BF526C/ADSP-BF527C	www.analog.com/processors	Preliminary
ADSP-BF531/ADSP-BF532/ADSP-BF533	www.analog.com/processors	
ADSP-BF534/ADSP-BF536/ADSP-BF537	www.analog.com/processors	
ADSP-BF535	www.analog.com/processors	
ADSP-BF538/ADSP-BF538F	www.analog.com/processors	
ADSP-BF539/ADSP-BF539F	www.analog.com/processors	
ADSP-BF542/ADSP-BF544/ADSP-BF548/ADSP-BF549	www.analog.com/processors	Preliminary
ADSP-BF561	www.analog.com/processors	
Blackfin Processor, Development Board, and Emulator Publications		
ADSP-BF533 Blackfin Processor Hardware Reference	www.analog.com/processors	82-002005-01
ADSP-BF535 Blackfin Processor Hardware Reference	www.analog.com/processors	82-000410-13
ADSP-BF537 Blackfin Processor Hardware Reference	www.analog.com/processors	82-000555-01
ADSP-BF538/ADSP-BF538F Blackfin Processor Hardware Reference	www.analog.com/processors	82-000002-01
ADSP-BF54x Blackfin Processor Peripheral Hardware Reference	www.analog.com/processors	82-000001-01
ADSP-BF54x Blackfin Processor Hardware Reference	www.analog.com/processors	82-000000-01
ADSP-BF561 Blackfin Processor Hardware Reference	www.analog.com/processors	82-000561-01
Getting Started with Blackfin Processors	www.analog.com/processors	82-000850-01
ADSP-BF53x/BF56x Blackfin Processor Programming Reference	www.analog.com/processors	82-000556-01
ADSP-BF533 EZ-KIT Lite Evaluation System Manual	www.analog.com/processors	82-000730-01
ADSP-BF537 EZ-KIT Lite Evaluation System Manual	www.analog.com/processors	82-000865-01
ADSP-BF538 EZ-KIT Lite Evaluation System Manual	www.analog.com/processors	82-000945-01
Getting Started with ADSP-BF537 EZ-KIT Lite	www.analog.com/processors	82-000865-02
ADSP-BF548 EZ-KIT Lite Manual	www.analog.com/processors	82-000206-01
ADSP-BF561 EZ-KIT Lite Evaluation System Manual	www.analog.com/processors	82-000811-01
Blackfin EZ-Extender Manual	www.analog.com/processors	82-000735-01
Blackfin A-V EZ-Extender Manual	www.analog.com/processors	82-000870-01
Blackfin USB-LAN EZ-Extender Manual	www.analog.com/processors	82-000845-01
Blackfin FPGA EZ-Extender Manual	www.analog.com/processors	82-000920-01
Blackfin Audio EZ-Extender Manual	www.analog.com/processors	82-000195-01
HPUSB, USB, HPPCI, and MSP430 Emulator User's Guide	www.analog.com/processors	82-000760-01
VisualDSP++ for Blackfin Processors		
Complete Set of ADSP-BFxxx VisualDSP++ Manuals—includes the following:	From ADI Sales and Dist.	
VisualDSP++ 5.0 Getting Started Guide	www.analog.com/processors	82-000420-01
VisualDSP++ 5.0 User's Guide	www.analog.com/processors	82-000420-02
VisualDSP++ 5.0 C/C++ Compiler and Library Manual	www.analog.com/processors	82-000410-03
VisualDSP++ 5.0 Assembler and Preprocessor Manual	www.analog.com/processors	82-000420-04
VisualDSP++ 5.0 Linker and Utilities Manual	www.analog.com/processors	82-000420-03
VisualDSP++ 5.0 Product Release Bulletin	www.analog.com/processors	82-000420-06
VisualDSP++ 5.0 Kernel VDK User's Guide	www.analog.com/processors	82-000420-07
VisualDSP++ 5.0 Loader and Utilities Manual	www.analog.com/processors	82-000450-01
VisualDSP++ 5.0 Device Drivers and Systems Services Manual	www.analog.com/processors	82-000430-01
VisualDSP++ 5.0 Quick Installation Reference Card	www.analog.com/processors	82-000420-08
VisualDSP++ 5.0 Licensing Guide	www.analog.com/processors	82-002035-01
VisualAudio for Blackfin Processors		
VisualAudio Designer User's Guide	www.analog.com/visualaudio	
Getting Started with VisualAudio 2.5	www.analog.com/visualaudio	
VisualAudio 2.5 Quick Start Guide	www.analog.com/visualaudio	
VisualAudio Module Library Reference Manual	www.analog.com/visualaudio	
VisualAudio Module Pack Reference Manuals	www.analog.com/visualaudio	
VisualAudio Platform Reference Manuals	www.analog.com/visualaudio	
VisualAudio Advanced Designer Application Manuals	www.analog.com/visualaudio	
Audio Programmer Manuals	www.analog.com/visualaudio	
Embedded Engineer Manuals	www.analog.com/visualaudio	

Literature Guide

Title	Where to Order	Publication Number
SHARC Processor Data Sheets		
ADSP-21060/ADSP-21060L	www.analog.com/processors	
ADSP-21061/ADSP-21061L	www.analog.com/processors	
ADSP-21062/ADSP-21062L	www.analog.com/processors	
ADSP-21065L	www.analog.com/processors	
ADSP-21060C/ADSP-21060LC	www.analog.com/processors	
ADSP-21160M	www.analog.com/processors	
ADSP-21160N	www.analog.com/processors	
ADSP-21161N	www.analog.com/processors	
ADSP-21261	www.analog.com/processors	
ADSP-21262	www.analog.com/processors	
ADSP-21266	www.analog.com/processors	
ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366	www.analog.com/processors	
ADSP-21367/ADSP-21368/ADSP-21369	www.analog.com/processors	
ADSP-21371	www.analog.com/processors	Preliminary
ADSP-21375	www.analog.com/processors	Preliminary
SHARC Processor, Development Board, and Emulator Publications		
Getting Started with SHARC Processors	www.analog.com/processors	82-003536-01
ADSP-2106x SHARC Processor Family User's Manual	www.analog.com/processors	82-000795-03
ADSP-21065L SHARC Processor User's Manual	www.analog.com/processors	82-001833-01
ADSP-21065L SHARC Processor Technical Reference	www.analog.com/processors	82-001903-01
ADSP-21160 SHARC Processor Hardware Reference	www.analog.com/processors	82-001966-01
ADSP-21160 SHARC Processor Instruction Set Reference	www.analog.com/processors	82-001967-01
ADSP-21161 SHARC Processor Hardware Reference	www.analog.com/processors	82-001944-01
ADSP-2126x SHARC Processor Core Manual	www.analog.com/processors	82-001999-01
ADSP-2126x SHARC Processor Peripheral Manual	www.analog.com/processors	82-002002-01
ADSP-2136x SHARC Processor Programming Reference	www.analog.com/processors	82-000500-01
ADSP-2136x SHARC Processor Hardware Reference (ADSP-21362/ADSP-21363/ADSP-21364/ADSP-21365/ADSP-21366)	www.analog.com/processors	82-000501-01
ADSP-21368 SHARC Processor Hardware Reference (ADSP-21367/ADSP-21369/ADSP-21371/ ADSP-21375)	www.analog.com/processors	82-000100-01
ADSP-21061/21065L/21160M EZ-KIT Lite Installation Procedure	www.analog.com/processors	84-001970-01
ADSP-21160 EZ-KIT Lite Evaluation Manual	www.analog.com/processors	82-000513-01
ADSP-21161N EZ-KIT Lite Evaluation Manual	www.analog.com/processors	82-000530-01
ADSP-21262 EZ-KIT Lite Evaluation Manual	www.analog.com/processors	82-000800-01
ADSP-21364 SHARC EZ-KIT Lite Evaluation Manual	www.analog.com/processors	82-000840-01
ADSP-21369 EZ-KIT Lite Evaluation System Manual	www.analog.com/processors	82-000196-01
ADSP-21375 EZ-KIT Lite Manual	www.analog.com/processors	82-000940-02
SHARC EZ-Extender Manual	www.analog.com/processors	82-000805-01
SHARC USB EZ-Extender Manual	www.analog.com/processors	82-000197-01
HPUSB, USB, HPPCI, and MSP430 Emulators User's Guide	www.analog.com/processors	82-000760-01
VisualDSP++ for SHARC Processors		
Complete Set of SHARC VisualDSP++ Manuals—includes the following:	From ADI Sales and Dist.	
VisualDSP++ 5.0 Getting Started Guide	www.analog.com/processors	82-000420-01
VisualDSP++ 5.0 User's Guide	www.analog.com/processors	82-000420-02
VisualDSP++ 5.0 Assembler and Preprocessor Manual	www.analog.com/processors	82-000420-04
VisualDSP++ 5.0 C/C++ Compiler Manual	www.analog.com/processors	82-001963-02
VisualDSP++ 5.0 Linker and Utilities Manual	www.analog.com/processors	82-000420-03
VisualDSP++ 5.0 Kernel VDK User's Guide	www.analog.com/processors	82-000420-07
VisualDSP++ 5.0 Product Release Bulletin	www.analog.com/processors	82-000420-06
VisualDSP++ 5.0 Loader and Utilities Manual	www.analog.com/processors	82-000450-01
VisualDSP++ 5.0 Quick Installation Reference Card	www.analog.com/processors	82-000420-08
VisualDSP++ 5.0 Licencing Guide	www.analog.com/processors	82-002035-01
VisualDSP++ 5.0 Run-time Library Manual	www.analog.com/processors	82-000420-09
VisualAudio for SHARC Processors		
VisualAudio Designer User's Guide	www.analog.com/visualaudio	
Getting Started with VisualAudio 2.5	www.analog.com/visualaudio	
VisualAudio Module Library Reference Manual	www.analog.com/visualaudio	
Audio Programmer Manuals	www.analog.com/visualaudio	
VisualAudio 2.5 Quick Start Guide	www.analog.com/visualaudio	
VisualAudio Module Pack Reference Manuals	www.analog.com/visualaudio	
VisualAudio Platform Reference Manuals	www.analog.com/visualaudio	
Advanced Designer Application Manuals	www.analog.com/visualaudio	
Embedded Engineer Manuals	www.analog.com/visualaudio	

Literature Guide

Title	Where to Order	Publication Number
TigerSHARC Processor Data Sheets		
ADSP-TS101S	www.analog.com/processors	
ADSP-TS201S	www.analog.com/processors	
ADSP-TS202S	www.analog.com/processors	
ADSP-TS203S	www.analog.com/processors	
TigerSHARC Processor, Development Board, and Emulator Publications TigerSHARC Processor Data Sheets		
ADSP-TS101 TigerSHARC Hardware Reference	www.analog.com/processors	82-001996-01
ADSP-TS101 TigerSHARC Processor Programming Reference	www.analog.com/processors	82-001997-01
ADSP-TS201 TigerSHARC Processor Hardware Reference	www.analog.com/processors	82-000815-01
ADSP-TS201 TigerSHARC Programming Reference	www.analog.com/processors	82-000810-01
ADSP-TS101 EZ-KIT Lite Manual	www.analog.com/processors	82-000635-01
ADSP-TS201S EZ-KIT Lite Evaluation System Manual	www.analog.com/processors	82-000770-01
HPUSB, USB, HPPCI, and MSP430 Emulators User's Guide	www.analog.com/processors	82-000760-01
VisualDSP++ for TigerSHARC Processors		
Complete Set of TigerSHARC VisualDSP++ Manuals—includes the following:	From ADI Sales and Dist.	
VisualDSP++ 5.0 User's Guide	www.analog.com/processors	82-000420-02
VisualDSP++ 5.0 Assembler and Preprocessor Manual	www.analog.com/processors	82-000420-04
VisualDSP++ 5.0 C/C++ Compiler and Library Manual	www.analog.com/processors	82-000336-03
VisualDSP++ 5.0 Linker and Utilities Manual	www.analog.com/processors	82-000420-03
VisualDSP++ 5.0 Kernel VDK User's Guide	www.analog.com/processors	82-000420-07
VisualDSP++ 5.0 Getting Started Guide	www.analog.com/processors	82-000420-01
VisualDSP++ 5.0 Product Release Bulletin	www.analog.com/processors	82-000420-06
VisualDSP++ 5.0 Loader and Utilities Manual	www.analog.com/processors	82-000450-01
VisualDSP++ 5.0 Quick Installation Reference Card	www.analog.com/processors	82-000420-08
VisualDSP++ 5.0 Licensing Guide	www.analog.com/processors	82-002035-01

ADI Complementary Parts Guide

Supervisory Devices and DSP Processors

ADI Processor Family	DSP Supply Voltage	Reset Generators Only		With Open-Drain Output		
ADSP-BF5xx Blackfin Platform						
ADSP-BF531	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	— ADM809(T/S/R/Z)	— ADM1815	— ADM803(T/S/R/Z)	— ADM8617(S/R)	— ADM1816/ADM1818[1]
ADSP-BF532	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	— ADM809(T/S/R/Z)	— ADM1815	— ADM803(T/S/R/Z)	— ADM8617(S/R)	— ADM1816/ADM1818[1]
ADSP-BF533	0.8 V to 1.4 V core 2.5 V to 3.3 V I/O	— ADM809(T/S/R/Z)	— ADM1815	— ADM803(T/S/R/Z)	— ADM8617(S/R)	— ADM1816/ADM1818[1]
ADSP-BF534	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	— ADM809(T/S/R/Z)	— ADM1815	— ADM803(T/S/R/Z)	— ADM8617(S/R)	— ADM1816/ADM1818
ADSP-BF535	1.0 V to 1.6 V core 2.5 V to 3.3 V I/O	— ADM809(T/S/R/Z)	— ADM1815	— ADM803(T/S/R/Z)	— ADM8617(S/R)	— ADM1816/ADM1818[1]
ADSP-BF536	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	— ADM809(T/S/R/Z)	— ADM1815	— ADM803(T/S/R/Z)	— ADM8617(S/R)	— ADM1816/ADM1818
ADSP-BF537	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	— ADM809(T/S/R/Z)	— ADM1815	— ADM803(T/S/R/Z)	— ADM8617(S/R)	— ADM1816/ADM1818[1]
ADSP-BF561	0.8 V to 1.4 V core 2.5 V to 3.3 V I/O	— ADM809(T/S/R/Z)	— ADM1815	— ADM803(T/S/R/Z)	— ADM8617(S/R)	— ADM1816/ADM1818[1]
ADSP-TSxxx TigerSHARC Platform[2]						
ADSP-TS101S	1.2 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-TS201S	1.05 V core 2.5 V I/O	— ADM809(Z)	— ADM1815(R23/R22)	— ADM803(Z)	— ADM8617(Z)	— ADM1816/ADM1818(R23/R22)[1]
ADSP-TS202S	1.05 V core 2.5 V I/O	— ADM809(Z)	— ADM1815(R23/R22)	— ADM803(Z)	— ADM8617(Z)	— ADM1816/ADM1818(R23/R22)[1]
ADSP-TS203S	1.05 V core 2.5 V I/O	— ADM809(Z)	— ADM1815(R23/R22)	— ADM803(Z)	— ADM8617(Z)	— ADM1816/ADM1818(R23/R22)[1]
ADSP-21xxx SHARC Platform						
ADSP-21065L	3.3 V core 3.3 V I/O	ADM809(T/S) ADM809(T/S)	ADM1815(5/10) ADM1815(5/10)	ADM803(T/S) ADM803(T/S)	ADM8617(R) ADM8617(R)	ADM1816/ADM1818(5/10)[1] ADM1816/ADM1818(5/10)[1]
ADSP-21160M	2.5 V core 3.3 V I/O	ADM809(Z) ADM809(T/S)	ADM1815(R23/R22) ADM1815(5/10)	ADM803(Z) ADM803(T/S)	— ADM8617(R)	ADM1816/ADM1818(R23/R22)[1] ADM1816/ADM1818(5/10)[1]
ADSP-21160N	1.8 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-21161N	1.8 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-21261 ADSP-21262	1.2 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-21266	1.2 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-21267	1.2 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-21363 ADSP-21364	1.2 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-21365 ADSP-21366	1.2 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-21367 ADSP-21368 ADSP-21369	1.2 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	— ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-21xx Platform						
ADSP-2184N	1.8 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	ADM8617(W) ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-2185M	2.5 V core 3.3 V I/O	ADM809(Z) ADM809(T/S)	ADM1815(R23/R22) ADM1815(5/10)	ADM803(Z) ADM803(T/S)	ADM8617(Z) ADM8617(R)	ADM1816/ADM1818(R23/R22)[1] ADM1816/ADM1818(5/10)[1]
ADSP-2185N	1.8 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	ADM8617(W) ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-2186M	2.5 V core 3.3 V I/O	ADM809(Z) ADM809(T/S)	ADM1815(R23/R22) ADM1815(5/10)	ADM803(Z) ADM803(T/S)	ADM8617(Z) ADM8617(R)	ADM1816/ADM1818(R23/R22)[1] ADM1816/ADM1818(5/10)[1]
ADSP-2186N	1.8 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	ADM8617(W) ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-2187N	1.8 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	ADM8617(W) ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-2188M	2.5 V core 3.3 V I/O	ADM809(Z) ADM809(T/S)	ADM1815(R23/R22) ADM1815(5/10)	ADM803(Z) ADM803(T/S)	ADM8617(Z) ADM8617(R)	ADM1816/ADM1818(R23/R22)[1] ADM1816/ADM1818(5/10)[1]
ADSP-2188N	1.8 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	ADM8617(W) ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-2189M	2.5 V core 3.3 V I/O	ADM809(Z) ADM809(T/S)	ADM1815(R23/R22) ADM1815(5/10)	ADM803(Z) ADM803(T/S)	ADM8617(Z) ADM8617(R)	ADM1816/ADM1818(R23/R22)[1] ADM1816/ADM1818(5/10)[1]
ADSP-2189N	1.8 V core 3.3 V I/O	— ADM809(T/S)	— ADM1815(5/10)	— ADM803(T/S)	ADM8617(W) ADM8617(R)	— ADM1816/ADM1818(5/10)[1]
ADSP-2191M	2.5 V core 3.3 V I/O	ADM809(Z) ADM809(T/S)	ADM1815(R23/R22) ADM1815(5/10)	ADM803(Z) ADM803(T/S)	ADM8617(Z) ADM8617(R)	ADM1816/ADM1818(R23/R22)[1] ADM1816/ADM1818(5/10)[1]
ADSP-2196M	2.5 V core 3.3 V I/O	ADM809(Z) ADM809(T/S)	ADM1815(R23/R22) ADM1815(5/10)	ADM803(Z) ADM803(T/S)	ADM8617(Z) ADM8617(R)	ADM1816/ADM1818(R23/R22)[1] ADM1816/ADM1818(5/10)[1]

NOTES

[1]Weak internal pull-up which can be overdriven by external resistor.

[2]DSP eDRAM Voltage = 1.5 V (nominal).

With Manual Reset			With Watchdog		With Manual Reset and Watchdog			
— ADM811(T/S/R/Z)	— ADM6711/ADM6713(T/S/R/Z)	— ADM6315(31/29/26)	— ADM706T/S/R	— ADM8616(R/S/T/Y/Z)	— ADM823(R/S/T/Y/Z)	— ADM6316CY29	— ADM6320CY29	— ADM6823(R/S/T/Y/Z)
— ADM811(T/S/R/Z)	— ADM6711/ADM6713(T/S/R/Z)	— ADM6315(31/29/26)	— ADM706T/S/R	— ADM8616(R/S/T/Y/Z)	— ADM823(R/S/T/Y/Z)	— ADM6316CY29	— ADM6320CY29	— ADM6823(R/S/T/Y/Z)
— ADM811(T/S/R/Z)	— ADM6711/ADM6713(T/S/R/Z)	— ADM6315(31/29/26)	— ADM706T/S/R	— ADM8616(R/S/T/Y/Z)	— ADM823(R/S/T/Y/Z)	— ADM6316CY29	— ADM6320CY29	— ADM6823(R/S/T/Y/Z)
— ADM811(T/S/R/Z)	— ADM6711/ADM6713(T/S/R/Z)	— ADM6315(31/29/26)	— ADM706T/S/R	— ADM8616(R/S/T/Y/Z)	— ADM823(R/S/T/Y/Z)	— ADM6316CY29	— ADM6320CY29	— ADM6823(R/S/T/Y/Z)
— ADM811(T/S/R/Z)	— ADM6711/ADM6713(T/S/R/Z)	— ADM6315(31/29/26)	— ADM706T/S/R	— ADM8616(R/S/T/Y/Z)	— ADM823(R/S/T/Y/Z)	— ADM6316CY29	— ADM6320CY29	— ADM6823(R/S/T/Y/Z)
— ADM811(T/S/R/Z)	— ADM6711/ADM6713(T/S/R/Z)	— ADM6315(31/29/26)	— ADM706T/S/R	— ADM8616(R/S/T/Y/Z)	— ADM823(R/S/T/Y/Z)	— ADM6316CY29	— ADM6320CY29	— ADM6823(R/S/T/Y/Z)
— ADM811(T/S/R/Z)	— ADM6711/ADM6713(T/S/R/Z)	— ADM6315(31/29/26)	— ADM706T/S/R	— ADM8616(R/S/T/Y/Z)	— ADM823(R/S/T/Y/Z)	— ADM6316CY29	— ADM6320CY29	— ADM6823(R/S/T/Y/Z)
— ADM811(T/S/R/Z)	— ADM6711/ADM6713(T/S/R/Z)	— ADM6315(31/29/26)	— ADM706T/S/R	— ADM8616(R/S/T/Y/Z)	— ADM823(R/S/T/Y/Z)	— ADM6316CY29	— ADM6320CY29	— ADM6823(R/S/T/Y/Z)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	— ADM6823(T/S/R)
— ADM811(Z)	— ADM6711/ADM6713(Z)	— —	— —	— ADM8616(Z/Y)	— ADM823(Z/Y)	— —	— —	— ADM6823(Z/Y)
— ADM811(Z)	— ADM6711/ADM6713(Z)	— —	— —	— ADM8616(Z/Y)	— ADM823(Z/Y)	— —	— —	— ADM6823(Z/Y)
— ADM811(Z)	— ADM6711/ADM6713(Z)	— —	— —	— ADM8616(Z/Y)	— ADM823(Z/Y)	— —	— —	— ADM6823(Z/Y)
ADM811(T/S) ADM811(T/S)	ADM6711/ADM6713(T/S) ADM6711/ADM6713(T/S)	ADM6315(31/29) ADM6315(31/29)	ADM706T/S ADM706T/S	ADM8616(T/S/R) ADM8616(T/S/R)	ADM823(T/S/R) ADM823(T/S/R)	ADM6316CY29 ADM6316CY29	ADM6320CY29 ADM6320CY29	ADM6823(T/S/R) ADM6823(T/S/R)
ADM811(Z) ADM811(T/S)	ADM6711/ADM6713(Z) ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	ADM8616(Z/Y) ADM8616(T/S/R)	ADM823(Z/Y) ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(Z/Y) ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(W/V) ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(W/V) ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	— ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	— ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	— ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	— ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	— ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	— ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(W/V) ADM6823(T/S/R)
ADM811(Z) ADM811(T/S)	ADM6711/ADM6713(Z) ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	ADM8616(Z/Y) ADM8616(T/S/R)	ADM823(Z/Y) ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(Z/Y) ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(W/V) ADM6823(T/S/R)
ADM811(Z) ADM811(T/S)	ADM6711/ADM6713(Z) ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	ADM8616(Z/Y) ADM8616(T/S/R)	ADM823(Z/Y) ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(Z/Y) ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(W/V) ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(W/V) ADM6823(T/S/R)
ADM811(Z) ADM811(T/S)	ADM6711/ADM6713(Z) ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	ADM8616(Z/Y) ADM8616(T/S/R)	ADM823(Z/Y) ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(Z/Y) ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(W/V) ADM6823(T/S/R)
ADM811(Z) ADM811(T/S)	ADM6711/ADM6713(Z) ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	ADM8616(Z/Y) ADM8616(T/S/R)	ADM823(Z/Y) ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(Z/Y) ADM6823(T/S/R)
— ADM811(T/S)	— ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	— ADM8616(T/S/R)	— ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(W/V) ADM6823(T/S/R)
ADM811(Z) ADM811(T/S)	ADM6711/ADM6713(Z) ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	ADM8616(Z/Y) ADM8616(T/S/R)	ADM823(Z/Y) ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(Z/Y) ADM6823(T/S/R)
ADM811(Z) ADM811(T/S)	ADM6711/ADM6713(Z) ADM6711/ADM6713(T/S)	— ADM6315(31/29)	— ADM706T/S	ADM8616(Z/Y) ADM8616(T/S/R)	ADM823(Z/Y) ADM823(T/S/R)	— ADM6316CY29	— ADM6320CY29	ADM6823(Z/Y) ADM6823(T/S/R)

ADI Complementary Parts Guide

Power Management and DSP Processors

			Recommended ADI Power Management Devices for Maximum DSP Core and I/O Currents			
			1 DSP		2 or More DSPs	
ADI Processor Family	DSP Supply Voltage (nom)	Max Supply Current[1]	LDO	DC-to-DC Switching Regulator/Controller	LDO	DC-to-DC Switching Regulator/Controller
ADSP-BF5xx Blackfin Platform						
ADSP-BF531	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	55 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-BF532	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	55 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-BF533	0.8 V to 1.4 V core 2.5 V to 3.3 V I/O	55 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-BF534	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	55 mA	ADP1710	ADP2102	ADP1712	ADP2102
ADSP-BF535	1.0 V to 1.6 V core 2.5 V to 3.3 V I/O	650 mA 100 mA	ADP1706 ADP1710	ADP2105 ADP2102	ADP3339 ADP1712	ADP2106 ADP2102
ADSP-BF536	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	55 mA	ADP1710	ADP2102	ADP1712	ADP2102
ADSP-BF537	0.8 V to 1.2 V core 2.5 V to 3.3 V I/O	55 mA	ADP1710	ADP2102	ADP1712	ADP2102
ADSP-BF561	0.8 V to 1.4 V core 2.5 V to 3.3 V I/O	75 mA[2]	ADP1710	ADP2102	ADP1712	ADP2102
ADSP-TSxxx TigerSHARC Platform[3]						
ADSP-TS101S	1.2 V core 3.3 V I/O	1.6 A 137 mA	— ADP1715	ADP1821 ADP2105	— ADP1706	ADP1821 ADP2105
ADSP-TS201S	1.05 V core 2.5 V I/O	2.5 A 137 mA	— ADP1715	ADP1821 ADP2105	— ADP1706	ADP1821 ADP2105
ADSP-TS202S	1.05 V core 2.5 V I/O	2.5 A 137 mA	— ADP1715	ADP1821 ADP2105	— ADP1706	ADP1821 ADP2105
ADSP-TS203S	1.05 V core 2.5 V I/O	2.5 A 137 mA	— ADP1715	ADP1821 ADP2105	— ADP1706	ADP1821 ADP2105
ADSP-21xxx SHARC Platform						
ADSP-21065L	3.3 V core 3.3 V I/O	275 mA 21 mA	ADP1706 ADP1715	ADP2102	ADP1706 ADP1710	ADP2105 ADP2102
ADSP-21160M	2.5 V core 3.3 V I/O	875 mA 41 mA	ADP1706 ADP1710	ADP2105 ADP2102	— ADP1715	ADP2107 ADP2102
ADSP-21160N	1.8 V core 3.3 V I/O	875 mA 72 mA	ADP1706 ADP1715	ADP2105 ADP2102	— ADP1710	ADP2107 ADP2102
ADSP-21161N	1.8 V core 3.3 V I/O	550 mA 56 mA	ADP1706 ADP1710	ADP2105 ADP2102	ADP3339 ADP1710	ADP2106 ADP2102
ADSP-21261 ADSP-21262	1.2 V core 3.3 V I/O	940 mA 60 mA	ADP1706 ADP1710	ADP2105 ADP2102	— ADP1710	ADP2107 ADP2102
ADSP-21266	1.2 V core 3.3 V I/O	940 mA 60 mA	ADP1706 ADP1710	ADP2105 ADP2102	— ADP1710	ADP2107 ADP2102
ADSP-21367 ADSP-21368 ADSP-21369	1.2 V core 3.3 V I/O	940 mA 60 mA	ADP1706 ADP1710	ADP2105 ADP2102	— ADP1710	ADP2107 ADP2102
ADSP-21xx Platform						
ADSP-2184N	1.8 V core 3.3 V I/O	25 mA 14 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2185M	2.5 V core 3.3 V I/O	38 mA 12 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2185N	1.8 V core 3.3 V I/O	25 mA 14 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2186M	1.8 V core 3.3 V I/O	38 mA 12 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2186N	1.8 V core 3.3 V I/O	25 mA 14 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2187N	1.8 V core 3.3 V I/O	26 mA 14 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2188M	2.5 V core 3.3 V I/O	44 mA 12 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2188N	1.8 V core 3.3 V I/O	25 mA 14 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2189M	2.5 V core 3.3 V I/O	32 mA 15 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2189N	1.8 V core 3.3 V I/O	26 mA 14 mA	ADP1710	ADP2102	ADP1710	ADP2102
ADSP-2191M	2.5 V core 3.3 V I/O	184 mA 14 mA	ADP1712 ADP1710	ADP2102	ADP1715 ADP1710	ADP2102
ADSP-2196M	2.5 V core 3.3 V I/O	184 mA 14 mA	ADP1712 ADP1710	ADP2102	ADP1715 ADP1710	ADP2102

[1]Based on DSP nominal supply voltage. Refer to data sheet for other conditions.
[2]On-chip voltage regulation.
[3]DSP eDRAM voltage = 1.5 V (nominal).

Notes

Notes

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