2008.01





## Renesas MCU M16C Family (R32C/M32C/M16C/R8C)



# M16C Family (R32C/M32C/M16C/R8C) **Powerful Processor Easy to Use**

**Renesas**Technology www.renesas.com

# World's No. 1\* Flash MCUs !!

World's No. 1 **Flash MCUs** Proof No. 1

### **Total shipments of** 1.000.000.000 units!!

Thanks to strong demand, total flash MCU shipments reached the 1 billion mark in March 2007. Renesas flash MCUs are used in a wide range of consumer, industrial and automotive applications.

World's No. 1 Flash MCUs Proof No. 2

### **No. 1** lineup of flash MCUs with over 300 products in 30 series!!

Divided into high-end, middle, and low-end classes, the flash MCU lineup is built on the most advanced technology. Flexible support is provided for increasingly large and complex software.

World's No. 1 Flash MCUs Proof No. 3

### High-speed flash memory supporting up to 100MHz operation!!

Renesas flash technology provides direct memory access and no-wait-state operation at up to 100MHz to bring out the full capabilities of the MCU.



### World's No. 1 Flash MCUs Proof No. 4

### World's No. 1 Flash MCUs Proof No. 5

Flash MCU technology supports high-speed programming at a rate of 512KB every 20 seconds (total time required for reprogramming, including erasing and programming).

### World's No. 1 Flash MCUs **Proof No. 6**

Renesas delivers seamless integrated development environments and up-to-date technical information for 8-bit to 32-bit MCUs alongside a guick and responsive support system.

### Exceeding expectations for flash MCUs— FLASH & FLEXIBLE.

MCUs with embedded flash memory are now the main focus of MCU system development. Since its introduction, Flash MCUs from Renesas has been the industry leader in this product category. Over 300 individual products in 30 series are available, with processors ranging from 8 to 32 bits. Total shipments reached 1,000 million units in March 2007, making Renesas MCU the world's No. 1 flash MCU. With a wide selection of development tools from Renesas and our partner companies as well as comprehensive Web based support, it is now easier than ever to develop products around Flash MCU, and new advances are being made continuously

\*No,1 in total units shipped as of June 2007 (Renesas statistics)

### Rewriting possible during operation, and program/erase cycles increased to 100,000!

E2dataFlash substantially improves the functionality and performance of data flash, allowing data to be rewritten independently while the MCU is operating. Guaranteed program/erase cycles have been increased to 100,000, and data save times are two orders of magnitude faster than external E2PROM. (E2dataFlash: E2PROM emulation data flash memory)

### **40µsec**./byte high-speed flash programming!!

### Comprehensive support and **Service** to assist developers!!

# index Roadmap CPU Architecture Concepts Product Lineup Development Tools Development Tools from **Renesas Partners** Middleware/ Demo Sets Functions/ Application Fields Memory Capacity Product No. Table Support System



supporting a wide range of applications.



Series Comparison							
CPU Core	R8C	M16	C/60	M16C/80	M32	C/80	R32C/100
Address Space		1MB		16MB			4GB
DMA	No 2 to 4ch		4ch				
DMA II	No Yes			Yes			
Operation Instructions	16-Bit Operation Instructions			32-Bit Operation Instructions			
Barrel Shifter	No			Yes			
Series	R8C/Tiny	M16C/Tiny	M16C/6X	M16C/80	M32C/8X	M32C/9X	R32C/1XX
Max. Operating Frequency	20MHz	24MHz	24 to 32MHz	20MHz	32MHz	64MHz	64MHz
Max. On-Chip Memory	128KB	128KB	512KB	256KB	1MB	512KB	1MB
External Bus Extension	N	No Yes					
Other	8bit I/O		8bit + 16bit I/C	)	Intellig	ent I/O	FPU



#### 

# **CPU Architecture**

The register layout and addressing of the M16C Family are optimized for embedded applications. Naturally, development using high-level languages (C, C++) is supported.

### R32C/M32C Register Model



#### R32C/M32C Register Model (DMA Related)



#### **DMA** Function



#### **Basic Instructions**

are executed in one cycle.	Туре	Instruction	Function	Туре	Instruction	Function
-		ABS	Absolute value		BCLR	Clear bit
		ADC	Add with carry	<b>D</b> <sup>14</sup>	BNOT	Invert bit
		ADCF	Add carry flag	BIL	BNTST	Test inverted bit
		ADD	Add without carry	manipulation	BSET	Set bit
		CMP	Compare		BTST	Test bit
	Arithmetic	DEC	Decrement		ROLC	Rotate left with carry
	74141110400	EXTS	Extend sign	Shift	RORC	Rotate right with carry
		EXTZ	Extend zero		ROT	Rotate
		INC	Increment	d his shift	SHA	Shift arithmetic
		NEG	Two's complement	I-DIT SHIT	SHL	Shift logical
		SBB	Subtract with borrow		FCLR	Clear flag register bit
		SBU	Subtract without borrow		FSET	Set flag register bit
		AND	Logical AND		INDEX	Index
		NOT	Invert all bits		INTO	Interrupt on overflow
	Logic	OR	Logical OR	Other	Jcnd	Jump on condition
		TST	Test		LDC	Transfer to control register
		XOR	Exclusive OR		NOP	No operation
		MOV	Transfer		PUSHC	Save control register
	Transfer	PUSH	Save		SCcnd	Store on condition
		PUSHM	Save multiple registers			

#### Advanced Instructions (Enhanced 32-Bit Instructions - R32C/100)

The R32C/100 CPU core features enhanced 32-bit instructions and many instructions with advanced functionality.

Category	Instruction	Description
	ADSF	Sign flag add
	EDIV	Signed divide (64 $\div$ 32 $\rightarrow$ 32-bit)
	EDIVU	Unsigned divide (64 $\div$ 32 $\rightarrow$ 32-bit)
Arithmetic instructions	EDIVX	Signed divide (32 $\div$ 32 $\rightarrow$ 32-bit)
	EMUL	Signed multiply (32 $\div$ 32 $\rightarrow$ 64-bit)
	MULX	Multiply with rounding
	EMULU	Unsigned multiply (32 $\div$ 32 $\rightarrow$ 64-bit)
	ADDF	Floating point add
	CMPF	Floating point compare
	CNVIF	Convert integer $\rightarrow$ floating point number
Floating point operation instructions	DIVF	Floating point divide
	MULF	Floating point multiply
	ROUND	Convert floating point number $\rightarrow$ integer
	SUBF	Floating point subtract
		Search until data matching search string
	SUNTIL	found
		Search until data not matching search
	SWHILE	string found
High-level language support instructions	EXITI	Release interrupt stack frame
Other	STOP	Stop

### Enhanced Multiply and Accumulate Instruction



# **Concepts Security Functions**

The M16C Family incorporates a number of security functions to prevent unauthorized access to its internal ROM contents.

### Flash Memory ROM Code Protection

During parallel programming, the ROM protection bits prevent reading or overwriting of on-chip flash memory. It is not even possible to read the contents of flash memory using an external flash programmer. (The protect bits can only be changed by serial programming.)



#### Flash Memory ID Code Protection



#### Prevention of Reading On-Chip Flash Memory



Details: ROM correction: The M16C Family has a function that allows program correction of up to four locations using address match interrupts.

# **Concepts Excellent Reliability**

The M16C Family incorporates many design features to ensure reliable operation under a variety of conditions.

### On-Chip Oscillator with Fail Safe Feature

#### Enhanced Reliability with On-Chip Oscillator and Oscillation Stop Detection Circuit



Other reduces
 It is possible to use software to halt XIN oscillator input and MCU can operate using the high-speed on-chip oscillator instead. (This also reduces power consumption.)
 The watchdog timer can operate independently using the separate low-speed (125kHz) on-chip ascillator.

### Protecting Critical Registers



#### Grouping Together of Important Pins



# **Concepts** Low-Power Operation

M16C MCUs are designed to minimize power consumption.

### Low-Current Consumption through Advanced Processes



#### **Multiple Power Management Functions**



#### **Reduced Load Capacitance**



# **Concepts** Low EMI/Excellent EMS

The M16C Family is designed to maximize EMI/EMS performance. This reduces costs associated with EMI/EMS countermeasures for application developers.

### Low Electromagnetic Interference (EMI)



Note: Evaluation is also performed using the VDE and TEM cell methods. Only products that meet uniform standards are produced in volume.

### Excellent Ability to Withstand Noise (EMS)



#### Short Distance between VCC and VSS

The VCC and VSS pins are arranged close together on M16C MCUs to prevent noise from entering via the VCC and ground wiring. Internal parasitic capacitors provide further protection against noise at the VCC and VSS pins. This design also helps suppress unwanted noise emission from the chip itself.



# **Concepts Excellent Compatibility**

The M16C Family provides compatibility in all aspects, allowing easy transition to higher end models.

#### Pin Compatible



#### Compatible Peripheral Functions



can be initiated by peripheral I/O requests.

### Advantages of Compatibility



# **Concepts High-Speed Processing**

The M16C Family provides high-speed processing under a variety of conditions.

### R32C CPU Core Pipeline



#### High-Speed Interrupt Processing (R32C/M32C)



#### Floating Point Instructions (R32C)

The R32C incorporates a single-precision 32-bit FPU and supports floating point instructions.



Underflow

# **Concepts** Abundant Peripheral Functions

The M16C Family includes high-performance on-chip functions for a variety of applications.

#### Block Diagram - R32C/111



#### Serial Interface



#### I<sup>2</sup>C Bus Interface

#### The I<sup>2</sup>C Bus is supported as a serial interface.

#### M16C/62P, M16C/64, M16C/65, M32C, R32C Supported MCUs M16C/65, M16C/Tiny, R8C/Tiny Communication control method Partial software control Hardware control Start condition overlap detection No detection Detection supported Arbitration lost detection Requires flag to be initialized for each byte Does not require flag to be initialized for each byte Slave address match determination Match determination by software Match determination by hardware, interrupt generated only on match Initial acknowledge generation Generated by software after slave address determined Automatic processing by hardware Timeout detection function None Supported (dedicated timer) 384 kbps 400 kbps Max. communication speed (max. value of I<sup>2</sup>C Bus standard high-speed mode) (because the SCL low duration $\ge$ 1.3 $\mu$ s standard is not met at faster speeds)

#### A/D Converter



# **Concepts** Abundant Peripheral Functions

#### Highly Functional Timers

M16C MCUs have input and output timers that are used in combination with other peripheral functions.



#### Intelligent I/O

I/O ports can be configured to implement different peripheral functions.



Signal Delay Caused by Digital Filter (Max. 3.5 Cycles of Filter Clock)

#### **Bus Control**



# **Concepts** Abundant Peripheral Functions

### PLL Oscillator Circuit and Oscillation Stop Detection Circuit



### **On-Chip Oscillator Startup**



#### High-Precision High-Speed On-Chip Oscillator





#### Watchdog Timer



#### Other Functions



# Lineup of Products with On-Chip Flash Memory

All series in the M16C Family include products with on-chip flash memory.

### Features of M16C MCUs with On-Chip Flash Memory

#### 1. High-Speed Programming/Erasing

Programming 256KB of flash memory takes only four seconds (serial rewrite mode). This greatly reduces the programming burden in the volume production process. (M16C/62P)

#### 2. High Reliability

High data storage reliability, erasing reliability, and programming reliability help prevent problems following mounting.

#### 3. ROM Code Protect Function

High-level security functionality is built in.

#### 4. Support for On-Line Programming (CPU Rewrite Mode)

High-level security functionality is built in.

#### 5. Support for Data Flash Memory

Products are available with extra-high guaranteed write/erase counts up to 10,000 times



#### List of Flash Programmers

Manufacturer	Product Model	Writing Method	
BPM Microsystems	BP-2610, BP-2710, BP-2710M	Parallel (Gang)	
Data 1/O Corporation	UNISITE, 3980 (3900), Optima, Dual, Qctal, PP100	Parallel (Gang)	
Data 1/O Corporation	Image Writer	Serial	
System General Corp.	T9600	Parallel (Gang)	
Suppy Gikon Inc	S550-MFW-1U	Parallel (Gang) and Serial	
Sunny Giken Inc.	S550-SFW1U	Serial	
Yokogawa Digital Computer Corporation	NET IMPRESS	Serial	
	R0E00008AKCE00(E8a)	Serial	
Renesas Solutions Corp.	M3A-0665	Serial	
	M3A-0806	Serial	

Please contact the writer manufacturer for information on MCU compatibility.

#### **On-Chip Flash Memory Functions**

#### Flash Programming Mode



Program

Program Moved to RAM Periph

Processing in Response

to Interrupts

erial Rewrit Program

Interrupt Processing Program



M32C/100 Series

#### R32C/100 Series Roadmap RENESAS 144pin **R32C FlexRay Next-Generation Automotive Network** In annin **On-Chip Version** 100pin 💻 144pin 🗐 **CAN Automotive Network On-Chip** In Iannin Versions Planning 100pin – 144pin Development 100pin For consumer and industrial applications For consumer and industrial applications R32C/116, 117, 118 8+8KB 512KB+8KB 640KB+8KB KB 40KB 48KB R32C/111 48MHz 256KB+8KB 384KB+8KB 512KB+8KB 40KB, 63KB 40KB, 63KB 40KB, 63KB 48MHz

### R32C/111 Group Features

- 32-bit CICS MCUs inheriting the M16C/M32C features and employing R32C/100 Series CPU core.
- 32-bit barrel shifter, 32-bit multiplier, and high-precision FPU on-chip
- Performs 32-bitx32-bit multiply-accumulate operations in one clock cycle.
- Register bit length extended from M32C/80 and number of registers increased.
- 64-bit internal memory bus
- Short jumps with no penalty
- Enhanced Communication Function (SIO x 9 channels)

#### R32C/111 Block Diagram



Flash



M32C/100 Series

### R32C/100 Series Performance (On-Chip ROM/RAM)



### R32C/100 CPU Core Performance Overview

Item	M32C/80	R32C/100	
Basic instructions	108 instructions	108 instructions	
Hardware multiplier	16 × 16 = 32	$32 \times 32 = 64$	
Multiply and accumulate	16 × 16 + 48 = 48	$32 \times 32 + 64 = 64$	
FPU	No	Yes (IEEE 754 single-precision)	
Barrel shifter	16-bit	32-bit	
Address match interrupt	8 points settable	No	
DMA transfer unit	8-bit, 16-bit	8-bit, 16-bit, <mark>32-bit</mark>	
DMA transfer space	Fixed address from 16Mbyte user-specified space (16Mbyte space) 16Mbyte user-specified space from fixed address (16Mbyte space)	User-specified 64MB space from 64MB (0000000h-01FFFFFh) and (FE000000h-FFFFFFFh) user-specified space	
DMA transfer address direction	Forward direction, fixed (not possible to set both transfer source and destination to forward direction or to fixed)	Forward direction, fixed (possible to set both transfer source and destination to forward direction or to fixed)	
DMAC II transfer space	64 Kbytes	User-specified 64MB space from 64MB (0000000h-01FFFFFh) and (FE000000h-FFFFFFFh) user-specified space	

M16C/64, 65 Series

#### M16C/64, 65 Series Roadmap



#### M16C/64, 65 Series Features

- Continuation of features from M16C/62P
  - Maintains compatibility with M16C and M32C (pin compatibility, compatibility with peripheral functions).
  - Retains features such as low EMI noise and low current consumption.
- Improved performance
  - Faster operation :24MHz (M16C/62P)  $\rightarrow$  25MHz (M16C/64)  $\rightarrow$  32MHz (M16C/65)
  - Lower voltage (2.7 V to 5.5 V)
- Contributions to reduced system cost
  On-chip power-on reset function (M16C/65)
  - → Enables elimination of external reset IC/circuit. - High-speed (32MHz)/high-precision (±1.0%: target) on-chip oscillator (M16C/65)
  - $\rightarrow$  Enables elimination of external oscillator.
- Other main performance and function enhancements - Improved DMA (2 channels (M16C/62P)
  - $\rightarrow$  4 channels (M16C/64, M16C/65))
  - Improved serial communication (5 channels (M16C/62P) → 8 channels @100 pins (M16C/64, M16C/65))
  - Faster A/D conversion (2.75 μs @12MHz (M16C/62P) → 1.72 μs @25MHz (M16C/64, M16C/65))
  - On-chip realtime clock (1-week timer (M16C/65))

#### M16C/64 Block Diagram



#### M16C/65 Block Diagram (100-Pin Version)



M16C/64 Series



### M16C/64 and M16C/65 New Functions

Item	M16C/62P	M16C/64	M16C/65	
Max. CPU speed	24MHz (VCC = 3.0 to 5.5V)	<b>25MHz</b> (VCC = <b>2.7</b> to 5.5V)	<b>32MHz</b> (VCC = <b>2.7</b> to 5.5V)	
I <sup>2</sup> C Bus	Simple I <sup>2</sup> C Bus	Simple I <sup>2</sup> C Bus	Multimaster I <sup>2</sup> C Bus	New function
Realtime clock	No	No	Yes	New  function
8-bit PWM	No	No	2 channels	New  function
UART	3 channels	6 channels		↑ More channels
DMA	2 channels (24 sources)	4 channels (43 sources)		↑ More channels
External interrupts	6 interrupts	8 interrupts		More  interrupts
Port 8_5	Input only	I/O (N channel open drain output)		More output  support ports
Timer clock source	f64 not settable	f64 settable		New function
Flash memory erase suspend	No	No	Yes	↑ New function
Flash memory user boot area	No	No	Yes	New function

### M16C/62P, M16C/64, and M16C/65 Specification Comparison

Item M16C/62P (100-pin version)		M16C/62P (100-pin version)	M16C/64 (100-pin version)	M16C/65 (100-pin version)	
Basic instruction	ns	91 instructions	←	←	
Min. instruction time		41.6ns (24MHz, 0 wait states, VCC = 3.0 to 5.5V)	40ns (25MHz, 0 wait states, VCC = 2.7 to 5.5V)	31.2ns (32MHz, 0 wait states, VCC = 2.7 to 5.5V)	
		100ns (10MHz, 0 wait states, VCC = 2.7 to 5.5V)			
Memory	ROM	ROM-less, 48KB, 64KB, 96KB, 128KB, 192KB, 256KB, 320KB, 384KB, 512KB	128KB, 256KB, 512KB	128KB, 256KB, 384KB, 512KB, 640KB, 768KB	
	RAM	4KB, 5KB, 10KB, 12KB, 16KB, 20KB, 24KB, 31KB	12KB, 16KB, 31KB	12KB, 20KB, 31KB, 47KB	
I/O ports	P0 to P10	8-bit × 10, 7-bit × 1	8-bit × 11 (N channel O.D. × 3 (P70, P71, P85)	←	
Input ports	P85	1-bit × 1	-		
Timers		11 (timer A × 5, timer B × 6)	←	←	
PWM		_	_	8-bit × 2 channels	
RTC		_		1 channel (1 week)	
Serial interface		Synchronous/asynchronous × 3 channels (I <sup>2</sup> C Bus and IEBus support × 3 channels), synchronous × 2 channels	Synchronous/asynchronous × 6 channels (I <sup>2</sup> C Bus and IEBus support × 6 channels), synchronous × 2 channels	←	
Multimaster I <sup>2</sup> C	Bus	_	-	1 channel	
A/D converter		10-bit x max. 26 channels, ±3 LSB (at 10-bit, 5V), ±2 LSB (at 8-bit)	10-bit x max. 26 channels, ±3 LSB (at 3V and 5V)	←	
		Resolution: 8-bit or 10-bit	Resolution: 10-bit		
		Conversion speed (10-bit): 2.75 µs at 5V/oAD 12MHz	Conversion speed (10-bit): 1.72 µs at 5V/oAD 25MHz		
		(single, repeat, single sweep, repeat sweep 0, 1)	(single, repeat, single sweep, repeat sweep 0, 1)		
D/A converter		8-bit × 2	<i>←</i>	←	
DMAC		2 channels	4 channels	←	
CRC		Yes	←	With SFR access monitor function	
Watchdog timer		15-bit × 1 channel (with prescaler)	15-bit × 1 channel (with prescaler)	←	
			Reset start function selectable		
External interru	pts	NMI, INT0, INT1, INT2, INT3, INT4, INT5, key input (8 sources)	NMI, INTO, INT1, INT2, INT3, INT4, INT5, INT6, INT7, key input (10 sources)	←	
Address match	circuits	4	←	←	
Remote control re	eception circuit	—	—	Yes	
CEC circuit		—	—	Yes	
Clock generator	r circuit	4 circuits: PLL on-chip oscillator (1MHz), XIN, XCIN	4 circuits: PLL low-speed (125kHz) on-chip oscillator, XIN, XCIN	5 circuits: PLL high-speed, high-precision (32MHz at ±1.0%)	
, e		(built-in feedback resistor, external ceramic resonator or crystal	(built-in feedback resistor, external ceramic resonator or crystal oscillator)	on-chip oscillator, low-speed (125kHz) on-chip oscillator, XIN, XCIN	
		oscillator)		(built-in feedback resistor, external ceramic resonator or crystal oscillator)	
Voltage drop detection circuit		Yes (selectable between 2 values/optional)	Yes (selectable between 2 values)	Yes (selectable among 3 values)	
Power-on reset		_	_	Yes	
Power supply voltage		3.0 to 5.5V (24MHz), 2.7 to 5.5V (10MHz)	2.7 to 5.5V (25MHz)	2.7 to 5.5V (32MHz)	
Package		80-pin (0.65mm pin pitch), 100-pin (0.5/0.65mm pin pitch),	100-pin (0.5/0.65mm pin pitch)	80-pin (0.65mm pin pitch), 100-pin (0.5/0.65mm pin pitch),	
-		128-pin (0.5mm pin pitch)		128-pin (0.5mm pin pitch)	
Operating modes		Single-chip, memory expansion, microprocessor	<i>←</i>	←	
Tools		For M16C/62P	E100, E8a	<i>←</i>	

M32C/80 Series

### M32C/80 Series Roadmap



#### M32C/80 Series Features

- Downward compatible with M16C/80, allowing easy switchover if faster operation is required (32MHz@5V).
- Four basic arithmetic operation and transfer instructions are 32-bit, and 32-bit multiply, divide, and fast shift (using on-chip barrel shifter) instructions provide high-speed operation processing.
- In addition to dedicated timer and SIO functions using intelligent I/O, additional PWM and SIO functions can be implemented.
   On-chip CAN (max. 2 channels: M32C/85, M32C/87, max. 3 channels: M32C/88) provides support for a range of applications.
- On-chip input-capture timer and output-compare timer, with support for sensor input, are ideal for applications such as motor control.

#### M32C/87 Block Diagram



IC:Input Capture OC:Output Compare

M32C/80 Series

### M32C/80 Series Memory Lineup



M16C/Tiny Series





M16C/Tiny Series

#### M16C/26A Group Features

- Small foot print (7mm square, 48pins) and high-speed operation (20MHz@5V).
- Instructions and peripheral functions are compatible with M16C/62P for easy program portability.
- 3-phase motor control timer, enabling motor control in compact products.
- Data flash area can be used in place of external EEPROM.
- Higher frequency version (24MHz@5V) also available (M16C/26B).

#### M16C/26A Block Diagram



\* M16C/26B uses PLL for 24MHz operation.

#### M16C/28 Group Features

- Small foot print and high-speed operation (20MHz@5V)
- Instructions and peripheral functions are compatible with M16C/62P for easy program portability.
- 3-phase motor control timer, enabling motor control in compact products.
- Support for max. 2 I<sup>2</sup>C-bus channels using multimaster I<sup>2</sup>C-bus
- Data flash area can be used in place of external EEPROM.
- Higher frequency version (24MHz@5V) also available (M16C/28B).
- Small package (7mmx7mm: 85pins) available for flash versions only (except for 128KB products of M16C/28 and M16C/28B).

### M16C/28 Block Diagram

#### PLL TimerA 5ch M16C/60 **CPU** Core On-Chip Osc TimerB 3ch 20MHz/ 24MHz Sub Clock 32kHz Three-phase Motor Cont. Multiplier WDT CRC Interrupt **ROM Correction** RAM Max 12KB 10bit A/D Max 27ch SIO/UABT 3ch(l<sup>2</sup>C/IE-bus) IC/OC 8cl ROM Max 128KB MASK/Flash With Protect SIO Max 2ch DMAC Multimaster I<sup>2</sup>C \* M16C/28B uses PLL for 24MHz operation. IC:Input Capture OC:Output Compare

#### M16C/29 Group Features

- Adds CAN 2.0B to M16C/28. Compatible with M16C/28.
- Small mounting area and high-speed operation (20MHz@5V)
- Instructions and peripheral functions are compatible with M16C/62P for easy program portability.
- Retains 3-phase motor control timer, enabling motor control in compact products.
- Input-capture and output-compare functions for more flexible signal control
- Support for max. 2 I<sup>2</sup>C-bus channels using multimaster I<sup>2</sup>C-bus
- Data flash area can be used in place of external EEPROM.

#### M16C/29 Block Diagram

	PLL	TimerA 5ch	
M16C/60 CPU Core	On-Chip Osc	TimerB 3ch	
20101112	Sub Clock 32kHz	Three-phase	
Multiplier	WDT	Motor Cont.	
Interrupt	CRC	ROM Correction	
RAM Max 12KB	10bit A/D Max 27ch	SIO/UART 3ch(l <sup>2</sup> C/IE-bus)	
ROM Max 128KB	IC/OC 8ch	SIO Max 2ch	
With Protect	LVD	Multimaster I <sup>2</sup> C	
	DMAC	CAN 2.0B 1ch	

M16C/62

#### M16C/62 Roadmap



#### M16C/62P Group Features

- Wide range of memory options (ROM/RAM: ROM Less/4KB to 512KB/31KB)
- Supports 3V and 5V peripheral power supplies, allowing direct connection to 3V memory and 5V devices.
- SIO (3 channels) supports a subset of the IEBus and I<sup>2</sup>C-bus standards, allowing connection of a large number of devices.
- Insertion of from 0 to 3 wait states can be selected, allowing connection of slower devices.
- Enhanced watchdog timer, oscillation stop detection circuit, and new reset circuit on-chip

#### M16C/62P Block Diagram







#### M16C/6NK Group Features

- Retains the features of the M16C/62P (CPU core, low power consumption, EMI characteristics, peripheral functions) and adds CAN (2.0B) support.
- M16C/6NK, M16C/6NM: CAN 2.0B 2 channels, M16C/6NL, M16C/6NN: CAN 2.0B 1 channel
- Additional communication functions (CAN, serial interface: 5 channels (M16C/6NK, M16C/6NL)/ 7 channels (M16C/6NM, M16C/6NL)/
- 7 channels (M16C/6NM, M16C/6NN)
- Improved failsafe functions such as enhanced watchdog timer and oscillation stop detection circuit, additional external interrupts (9 channels: M16C/6NM, M16C/6NN)

#### M16C/6NK Block Diagram





M16C/30P Group

### M16C/30P Group Roadmap



### M16C/30P Group Features

- Compatible with M16C/62P while achieving lower cost through reduced functions and ROM/RAM capacity.
- Operating frequency of 16MHz (3V to 5V)
- Reduced peripheral functions (timer: 6 channels, SIO: 3 channels, A/D; 18 channels), limited to most commonly used functions.
- Package: 100-pin package only.
- Support for single-chip, memory expansion, and microprocessor modes
- Wide variety of on-chip memory options: Mask ROM, flash, one time flash and ROM Less versions available.
- Compatible with development support tools for the M16C/62P.

#### M16C/30P Block Diagram





M16C/39P Group

### M16C/39P Group Roadmap (Development Use Only) M16C/39P 128KB 192KB 16MHz@3.0 to 5.5V 5KB 6KB 10MHz@2.7 to 5.5V Mask

#### M16C/39P Group Features

- SiP combining M16C/30P general MCU and VFD controller/driver
- Retains features of the M16C/62P while slimming down ROM/RAM and peripheral functions.
- 34 user-configurable high-voltage ports (setting support for 2 to 16 digits)
- Dimmer function, variable frame cycle SiP: Solution Integrated Product™

#### M16C/39P Block Diagram



\*1. One of the three SIO channels is used for VFD control. Therefore, two SIO channels are available to the user.



ASSP

#### M16C/6V, M16C/6H Roadmap



#### M16C/6V Group Features

- On-chip OSD or data slicer for control of closed caption function or TV with ID1 function
- Memory options from 256KB to 512KB
- OSD supports display of 636 to 890 characters: 32 characters×16 lines or 40 characters×16 lines.
- Retains the features of the M16C/62P (low power consumption, EMI/EMS characteristics, peripheral functions).

#### M16C/6V7 Block Diagram



#### M16C/6H Group Features

- MCU with on-chip multi-slicer with worldwide compatibility and designed for DVD/HDD recorders.
- Support for TELETEXT, PDC, VPS, EPG-J, XDS, WSS, VideoID, etc.
- Retains the features of the M16C/62P (low power consumption, EMI/EMS characteristics, peripheral functions).

#### M16C/6H7 Block Diagram



ASSP

#### M16C/6S Group Features

- MCU with on-chip power line modem developed by Yitran (IT800) for power line communication
- Uses frequency band from 100kHz to 400kHz for power line communication, enabling a data transfer rate of 7.5kbps.
- Retains the features of the M16C/62P (low power consumption, EMI/EMS characteristics, peripheral functions).

#### M16C/6S Block Diagram



#### M16C/24 Group Features

- On-chip USB controller with full-speed support
- USB pull-up power supply circuit, USB clock generator circuit, many USB control functions
- Audio interface function implemented through addition of multi-bit serial I/O, memory card interface enhanced by strengthened CRC calculation function.
- Retains the features of the M16C/62P (low power consumption, EMI/EMS characteristics, peripheral functions).

#### M16C/24 Block Diagram



**R8C/Tiny Series** 



#### R8C/18-1B Group Features

- High-precision, high-speed on-chip oscillator (8MHz)
- On-chip multimaster I<sup>2</sup>C-bus
- On-chip clock-synchronous serial I/O with chip select
- Data flash area can be used in place of external EEPROM. R8C/19 Group, R8C/1B Group
- On-chip switchable sink or source-type large-current drive ports.
  On-chip power-on reset function and voltage detection function
- eliminate need for separate reset IC.
- 20pin Packages

#### R8C/18-1B Block Diagram



**R8C/Tiny Series** 

#### R8C/20-23 Group Features

- R8C/Tiny Series for automotive applications
- CAN 2.0B added. Upward compatible with R8C/22 Group, R8C/23 Group, R8C/20 Group, and R8C/21 Group.
- Support for high-temperature operation
  D version: -40 to 85°C
- J version : -40 to 85°C
- K version : -40 to 125°C
- Support for high-speed operation
- D version : VCC = 2.7 to 3.0V (f(XIN) = 10MHz) D version : VCC = 3.0 to 5.5V (f(XIN) = 20MHz) J version : VCC = 2.7 to 3.0V (f(XIN) = 10MHz) J version : VCC = 3.0 to 5.5V (f(XIN) = 20MHz) K version : VCC = 2.7 to 3.0V (f(XIN) = 10MHz)
- K version : VCC = 3.0 to 5.5V (f(XIN) = 16MHz)
- High-precision, high-speed on-chip oscillator (40MHz)
- Data flash area can be used in place of external EEPROM. (R8C/21 Group, R8C/23 Group)
- On-chip power-on reset function and voltage detection function eliminate need for separate reset IC.
- 48pin Packages

#### R8C/24-25 Group Features

- Support for low-voltage operation VCC = 2.2 to 5.5V (f(XIN) = 5MHz) VCC = 2.7 to 5.5V (f(XIN) = 10MHz)
  - VCC = 3.0 to 5.5V (f(XIN) = 20MHz)
- High-precision, high-speed on-chip oscillator (40MHz)
- On-chip subclock oscillator circuit (32.768kHz)
- On-chip timer RD for motor control
- On-chip multimaster I<sup>2</sup>C-bus
- On-chip clock-synchronous serial I/O with chip select
- Data flash area can be used in place of external EEPROM. (R8C/25 Group)
- On-chip power-on reset function and voltage detection function eliminate need for separate reset IC.
- On-chip switchable sink- or source-type large-current drive ports.
- 52pin Packages

#### R8C/26-29 Group Features

- Support for low-voltage operation
- VCC = 2.2 to 5.5V (f(XIN) = 5MHz) (N and D versions)
- VCC = 2.7 to 5.5V (f(XIN) = 10MHz)
- VCC = 3.0 to 5.5V (f(XIN) = 16MHz) (K version)
- VCC = 3.0 to 5.5V (f(XIN) = 20MHz) (other than K version)
- High-precision, high-speed on-chip oscillator (40MHz)
- On-chip subclock oscillator circuit (32.768kHz) (N and D versions)
- On-chip multimaster I<sup>2</sup>C-bus
- On-chip clock-synchronous serial I/O with chip select
- Data flash area can be used in place of external EEPROM. (R8C/27 Group, R8C/29 Group)
- On-chip power-on reset function and voltage detection function eliminate need for separate reset IC.
- On-chip switchable sink- or source-type large-current drive ports. (N and D versions)
- 32pin Packages (R8C/26, R8C/27 Group)
- 20pin Packages (R8C/28, R8C/29 Group)

#### R8C/20-23 Block Diagram



#### R8C/24-25 Block Diagram



#### R8C/26-29 Block Diagram

R8C/Tiny	Low-Speed On-Chip Osc	Timer RA
Max 20MHz	High-Speed On-Chip Osc	Timer RB
Multiplier	Main-Clock Max 20MHz	Timer RC
Interrupt	Sub-Clock 32kHz	
Flash	Oscillation Stop Detection	Timer RE (RTC)
Data Flash 2KB	WDT	
RAM	A/D Converter	SIO/UART 2ch
POR/LVD		SIO/ Multi-master I <sup>2</sup> C
LED Drive Port		Hardware LIN
### R8C/2A-2D Group Features

- Support for low-voltage operation
   VCC = 2.2 to 5.0V (f(XIN) = 5MHz)
   VCC = 2.7 to 5.5V (f(XIN) = 10MHz)
   VCC = 3.0 to 5.5V (f(XIN) = 20MHz)
- High-precision, high-speed on-chip oscillator (40MHz)
- On-chip subclock oscillator circuit (32.768kHz)
- On-chip D/A converter
- Additional 16-bit timer channel (timer RF)
- Support for motor control by on-chip timer RD
- On-chip multimaster I<sup>2</sup>C-bus
- On-chip clock-synchronous serial I/O with chip select
- Data flash area can be used in place of external EEPROM. (R8C/2B Group, R8C/2D Group)
- On-chip power-on reset function and voltage detection function eliminate need for separate reset IC.
- On-chip switchable sink- or source-type large-current drive ports.
- 64pin Packages (R8C/2A, R8C/2B Group)
- 80pin Packages (R8C/2C, R8C/2D Group)

#### R8C/2E and R8C/2F Group Features

- High-precision, high-speed on-chip oscillator (40MHz)
- On-chip D/A converter
- On-chip comparator enabling comparison with external power supply
- Data flash area that can be used as substitute for external EEPROM (R8C/2F Group)
- No need for separate reset chip thanks to power-on reset function and voltage detection function
- On-chip switchable sink- or source-type large-current drive ports.
- Compatible with low-cost on-chip debugging emulator
- 32-pin package

# R8C/2A-2D Block Diagram

R8C/Tiny	Low-Speed On-Chip Osc	Timer RA
Max 20MHz	High-Speed On-Chip Osc	Timer RB
Multiplier	Main-Clock Max 20MHz	Timer RC
Interrupt	Sub-Clock 32kHz	Timer RD
Flash	Oscillation Stop Detection	Timer RE (RTC)
Data Flash 2KB	WDT	Timer RF
RAM	A/D Converter	SIO/UART 2ch
POR/LVD	D/A Converter	SIO/ Multi-master I <sup>2</sup> C
LED Drive Port		Hardware LIN

#### R8C/2F Block Diagram



Developmen

#### **R8C/2G Group Features**

- Low-voltage operation possible
   VCC = 2.2 to 5.5V (f(XIN) = 4MHz)
   VCC = 2.7 to 5.5V (f(XIN) = 8MHz)
- High-precision, high-speed on-chip oscillator (8MHz)
- On ship substant, fight-speed off-onip oscillator (own iz)
- On-chip subclock generator circuit (32.768kHz)
- 1-channel 16-bit timer (timer RF)
- On-chip voltage detection circuit (comparison with external power supply possible in comparator mode)
- Compatible with low-cost on-chip debugging emulator
- On-chip hardware LIN (using 1 timer channel)
- 32-pin package

#### R8C/2G Block Diagram



# **Product Lineup**

**R8C/Tiny Series** 

### R8C/2H Group Features

- Low-voltage operation possible
- VCC = 2.2 to 5.5V (f(XIN) = 4MHz) VCC = 2.7 to 5.5V (f(XIN) = 8MHz)
- High-precision, high-speed on-chip oscillator (8MHz)
- On-chip subclock generator circuit (32.768kHz)
- 1-channel 16-bit timer (timer RF)
- On-chip voltage detection circuit (comparison with external power supply possible in comparator mode)
- Compatible with low-cost on-chip debugging emulator
- On-chip hardware LIN (using 1 timer channel)
- 20-pin package



### R8C/2J Group Features

- Low-voltage operation possible
- VCC = 2.2 to 5.5V (f(XIN) = 4MHz) VCC = 2.7 to 5.5V (f(XIN) = 8MHz)
- High-precision, high-speed on-chip oscillator (8MHz)
- 1-channel 16-bit timer (timer RF)
- On-chip voltage detection circuit (comparison with external power supply possible in comparator mode)
- Compatible with low-cost on-chip debugging emulator
- On-chip hardware LIN (using 1 timer channel)
- 20-pin package (only 16 pins enabled)



### R8C/2K and R8C/2L Group Features

- Low-voltage operation possible VCC = 2.2 to 5.5V (f(XIN) = 5MHz) VCC = 2.7 to 5.5V (f(XIN) = 10MHz)
- VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)
- High-precision, high-speed on-chip oscillator (40MHz)
- Motor control possible using on-chip timer RD
- Data flash area that can be used as substitute for external EEPROM (R8C/2L Group)
- No need for separate reset chip thanks to power-on reset function and voltage detection function
- On-chip switchable sink- or source-type large-current drive ports.
- Compatible with low-cost on-chip debugging emulator
- 32-pin package

#### **R8C/2L Block Diagram**

R8C/Tiny	Low-Speed On-Chip Osc	Timer RA	
Max 20MHz	High-Speed On-Chip Osc	Timer RB	
Multiplier	Main-Clock Max 20MHz	Timer RC	
Interrupt		Timer RD	
Flash	Oscillation Stop Detection		
Data Flash 2KB	WDT		
RAM	A/D Converter	SIO/UART 2ch	
POR/LVD			
LED Drive Port		Hardware LIN	

# **Product Lineup**

On-Chip CAN



**ROM Max 1MB** 

Flash / Mask With Protect Intelligent I/O

Input Cap 8ch. Output Comp.16ch Communication Func. (H/W IE Bus)

 Pin compatible and peripheral function compatible with products such as the M16C/62P, while retaining features including low noise, low power consumption, and high ROM efficiency.

#### 40

# **Product Lineup**

**ROM Less Versions** 

### M16C ROM Less Versions



### M16C ROM Less Product Features

- External ROM products ranging from M16C core to M32C core
- Support for function (separate bus) facilitating connection of external memory if large memory capacity is required and function (multiplex bus) to reduce the number of pins used
- Products are available with enhanced bus interfaces supporting a variety of timing requirements.
- Support for simultaneous connection of two voltages, 3.3V for memory interface and 5V for peripheral functions
- Retains the features of the M16C Family (low power consumption, EMI/EMS characteristics, peripheral functions).
- In addition to a full emulator, a compact emulator is under development.

#### M32C/80 Block Diagram





# **Development Tools**

Renesas provides customers with comprehensive product development support in partnership with leading third-party vendors.



#### Integrated Development Environment Providing Powerful and Complete Support for Developing Embedded Systems

Renesas integrated development environment brings together the tools needed for developing applications, including a compiler and debugger (emulator software). All steps from coding to evaluation and verification can be performed using a single application.

# High-performance Embedded Workshop Integrated Development Environment

 Integrated and centralized control over all tools, Latest Software Tools Latest Documents from the editor to the debugger Flexible support for multiple build\*<sup>1</sup> configurations (support Support Information (FAQs, Tool News, Etc.) CASE Tools, Etc. for saving multiple optionally specified configurations, Products from Benesas Part support for addition of external build tools, etc.) Internet Per-project management of source files Easy-to-use GUI based on Microsoft Windows Code Editing Renesas Integrated Development Environ High-performance Embedded Workshop Generation of C startup code customized for individual MCUs Common User Interface Test support function (See page 46 for details.) Application (Framework) Project Manager Evaluation Always up to date tools and documents
 Auto-update utility (See page 42 for details.)
 Document updater (See page 42 for details.) Programs Debugging Builder Compiling Linking Editor ..... • Flexible customization functions Common Front End (Framework) Custom build phase TargetServer (extended COM functions) C/C++ Compiler/ Linker Simulator Edito Extended TCL/TK functions and scripting MISRA C Works with products from Renesas partner companies Middle Support Tools (Software) Che CASE<sup>\*2</sup> tools to support upstream process design. Version control tools Real-time OS \*1 Build: The sequence of operations involved in generating object code, including compiling, assembling and linking. \*2 CASE: Computer Aided Software Engineering Support Tools Emulator (Hardware) Target System CPU Boards Evaluation Board T-Engine B Integrated Conceptual Image of High-performance Embedded Workshop

### C Compiler Package

#### C Compiler

- Conforms to ANSI\*1 language standard.
- Optimization features and many #pragma extended functions for extracting top performance from the MCU
- Support for use of near/far designations with variables
- Function for calculating the stack size to be used
   Support for embedding of SQMIint MISRA C\*<sup>2</sup> rule checker
- ANSI: American National Standards Institute
- 2 MISRA Motor Industry Software Reliability Association. "MISRA" is a registered trademark of MISRA Ltd. held on behalf of the MISRA Consortium

#### Simulator debugger

- Support for target-less evaluation
- C language and assembly language source-level debugging
- Support for source file editing
- Trace function
- RAM monitor function Virtual port I/O and virtual interrupts functions
- GUI implementation of target I/O functions
- \* Each compiler package product includes a simulator debugger.

## Peripheral Driver Generator

This utility automatically generates I/O drivers for MCU on-chip peripheral functions and setting routines (functions) based on settings entered via a simple GUI

Download/

Document

View

- Shorter development times: Making settings is easy since there is no
- need to do manual coding of peripheral I/O functions Improved reliability: Avoid mistakes or omissions in peripheral I/O register settinas
- Effective utilization of resources: Smooth portability among different Renesas MCU models



## **Real-time OS**

Provides easy control of large-scale and complex applications in real time. Reduces program development time and improves reusability and maintainability

- Conforms to µITRON4.0 standard.
- Compact size suitable for ROM programming.
- Context selection function allows reduction of amount of RAM used.
- Excellent real-time functionality (interrupt response time, task switching time) • Simple initial setup of application programs for use with real-time OS
- Configurator provided.
- Wide array of operating system debugging functions when integrated debugging in High-performance Embedded Workshop.



Example GUI Configuration Window

See the "Development Tools List" listing for the individual MCU for details on available C compiler packages and real-time OS packages as well as information on the operating environment.



Note: See "Development Tools List" for a list of products composing each emulator system.

# PC7501 Emulator



Full-Spec Emulator with Support for Operating Frequencies over 20MHz and Many Debugging Functions

The PC7501 is a full-featured emulator that supports M16C Family MCUs with operating frequencies exceeding 20MHz. Switchable evaluation probes provide support for different MCU models in the M16C Family.

• Full-bus-trace emulator for M16C Family MCUs operating at 66MHz

- Compact design with functions packed into the case size of a conventional system emulation pod
- Further extends the many debugging functions of the PC4701U.
- Flexible support for new MCU products by changing the firmware
- Support for USB, LPT parallel, and LAN communication interfaces
- The MCU is positioned on the probe block directly above the user target for enhanced signal integrity.
- AC adapter complying with safety standards supplied.
- Support for power supply voltages of 100 to 240V, 50/60Hz

#### **Product Contents**

- Emulator unit
- Software CD-ROM (High-Performance Embedded Workshop integrated development environment)
- Power, parallel, and USB cables
- Emulation probe connector cable
- User's manual

#### Main Specifications

Main Specification	15					
Target MCUs	M32C/80 Series     M16C/60 Series     M16C/30 Series     M16C/Tiny Series     R8C/Tiny Series     See the following URL for details.     http://www.renesas.com/pc7501		Real-time trace	<ul> <li>256K cycles</li> <li>Trace content: Address, data, MCU status, external trigger, timestamp</li> <li>Trace modes: 5 (break, before, about, after, full)</li> <li>Writing can be turned on or off for specific events.</li> </ul>		
			Real-time RAM monitor	<ul> <li>4,096bytes (256bytes × 16 blocks)</li> <li>Data, end address attributes (read, write, non-access)</li> </ul>		
Max. operating frequency	66.7MHz (depending on product)	1		Execution time from program start to and		
Target MCU modes	Single-chip mode, memory expansion mode, microprocessor mode		Execution time	Maximum, minimum, and average execution time		
Emulation memory	4MB standard (depending on MCU specifications)		measurement	and traversal count for 4 specified segments		
Supported power supply voltage	2.2 to 5.5V (depending on product)			Count clock: MCU clock or 16MHz		
Power supply to MCU	From DC power supply of PC7501		C0 coverage	8,192KB (256KB × 32 blocks)		
Software breaks	64 points		External trigger inputs/event outputs	External trigger inputs × 8 or event outputs (break × 1, event ×		
Hardwara braaka	8 points (execution address, bus detect, interrupt, external trigger signal)		PC interface	LPT parallel, USB (USB 1.1, full-speed), LAN (10-BASE-		
Hardware breaks			Operating environment	Windows <sup>®</sup> XP, Windows <sup>®</sup> 2000		
Hardware break combinations	AND, OR, simultaneous AND, state transition     Bus count: 255 times		Overseas standards	Compliant (FCC standards, CE marking)		
Exception event detection	Access protect					

### **Debugging Functions of High-Performance Embedded Workshop Integrated Development Environment**

#### Easy-to-Use Emulator Debugger

- Enables debugging using High-Performance Embedded Workshop running under Microsoft Windows.
- Simple and direct GUI
- Easy drag-and-drop operations
- Refined basic debugging functions to facilitate development work
- Real-time RAM monitoring
- High-level debugging functions such as real-time trace, C0 coverage, and duration measurement
- Online help in HTML format
- The latest version of High-performance Embedded Workshop is available for download on the Renesas Web site: http://www.renesas.com/hew\_download.



Screen Capture of PC7501 Emulator/Debugger Window



Though small in size, these compact emulators provide the solid debugging functions of full-spec units. The product package includes software tools such as an integrated development environment, Emulator Debuggers, after purchasing it.

- All-in-one packages including all software required for development Compact design
- An emulation memory function and microprocessor mode can be added by connecting an optional emulation memory board.
- Low price
- Solid debugging functions
- Hardware break function
- Real-time RAM monitor function Real-time trace function
- USB interface support
- Product Contents

Emulator unit

- Software CD-ROM (High-Performance Embedded Workshop
- integrated development environment, compiler package evaluation
- version [free of charge]) • USB and power cables (separate 5V/2A power supply required
- for compact emulator)
- User's manual, etc.

#### Main Specifications

nam opcome	adono					
		Target MCUs	Compost omulator	Software breaks	64 points	
	Series	Group	Compact emulator		2 points (address match, bus match, max.	
		M32C/81, M32C/82, M32C/83	S30830T-CPE (developed by Sunny Giken Inc.) *5	Hardware breaks*6	255 times bus count setting supported)	
	M32C/80	M32C/80*3, M32C/84, M32C/85, M32C/8A*3	M30850T3-CPE*1 *2		function cannot be used at the same time.	
		M32C/87	M30870T2-CPE		<ul> <li>Recording 64K cycles of bus data</li> </ul>	
	M16C/80	M16C/80	M30800T-CPE*5		supported (address, data, MCU status)	
	MICCO	M16C/62A	M30620T-CPE*5	Real-time trace	<ul> <li>5 trace mode settings: break, before, about, after full</li> </ul>	
Product	IVI 16C/60	M16C/62P	MODEODTO ODE*2		Writing can be turned on or off for specific	
	M16C/30	M16C/30P	WI3002P13-CPE -		events.	
	M16C/Tiny	M16C/26A		Real-time RAM	<ul> <li>1,024 (256bytes × 4 blocks)</li> </ul>	
		M16C/28	M3028BT2-CPE*4	monitor	Data, access history	
		M16C/29		Execution time measureme	<ul> <li>Execution time from program start to end</li> </ul>	
		R8C/10 to 19, 1A to 1B			Count clock: 10MHz	
	R8C/Tiny	R8C/20 to 29	R0E521000CPE00	C0 coverage	Not implemented	
	-	R8C/2A to 2D, 2K**, 2L**		PC interface	USB (USB1.1, full speed)	
	Single-c	hip mode		Dimensions	60mm×85mm	
Target	Memory	expansion mode*2		Operating environment	Windows® XP, Windows® 2000	
VCU modes	• MPU mo	ode <sup>*2</sup>		Overseas standards	Compliant (CE marking)	
	(Supporte	ed MCU modes differ depending on the l	MCU product.)			
1. The M30850T3- 2. The emulator un 3. The M32C/80 ar 4. The M3028BT2- 5. The specificatior	CPE is the suc it supports sin ad M32C/8A at CPE is the suc as of these cor	ccessor to the M30850T2-CPE. gle-chip mode and memory expansion mode. re supported in the microprocessor mode only, ccessor to the M30290T2-CPE. mpact emulators differ from the main specifical	To use microprocessor mod , so a separate emulation m tions listed above. See the V	e it is necessary to purch emory board is required. Veb site of the specific p	nase a separate emulation memory board.	
The best the second second	a all from all and a	and the second state of th	and a second sec			

o. I ne nardware break function and trace point function cannot be used simultaneously
 \*\*: To be supported soon.

#### Enhanced Development Efficiency from Test Support Function of High-performance Embedded Worksho

Macro Generator Support Function

The macro generator support function can be used to record repeated operations such as project control, building, and debugging in a macro file (command script file). Macros can be conveniently recorded and played from a toolbar.

Test Support Function

Stores the contents of test result windows as test image files. The test image files can then be compared later on.

#### Extra Convenience by Combining Macro Generator Support Function and Test Support Function

For example, you could record the steps in the test procedure in a macro file and record the anticipated test values in a test image file. The results can then be compared easily each time the test is run, improving efficiency and quality.



# Compiler packages evaluation version (free of charge). Customers can begin development work on application programs right away





#### PC4701U Emulator Web http://www.renesas.com/pc4701u Full-spec Emulator for M16C MCUs operating up to 20MHz The PC4701U makes it possible to build an emulation system that supports a variety of MCUs by combining it with an emulation pod matching the target MCU. · Includes debugging functions such as advanced break and real-time trace • Includes evaluation functions such as C0 coverage and time measurement. Real-time RAM monitor function is standard. Support for MCUs with operating frequencies up to 20MHz Target MCUs M16C Family See the following URL for details. http://www.renesas.com/pc4701u **Emulation Pod Operating Environment** PC4701U Emulator Unit Microsoft Windows<sup>®</sup> XP, Windows<sup>®</sup> 2000 **Product Contents** Emulator unit • USB cable, etc. High-Performance Embedded Workshop integrated development environment (Latest version available for download on Web site.) E30A Emulator \* Under Development Web http://www.renesas.com/e30a Emulator with NSD interface allowing connection via a single pin The E30A emulator features a NSD (New Single-wire Debugger) interface and supports the R32C/100 Series. It makes it simple to perform software verification functions such as on-chip debugging and data tuning in the actual operating environment. • Connection to emulator via newly developed single-pin NSD interface. (A coaxial cable is the only additional item required to perform debugging.) OCD (On-Chip Debugger) functionality It is not necessary to probe the foot pattern of the target MCU, so there is no MCU signal deterioration. No need for custom evaluation chips or custom packages. (Debugging can be performed with the target MCU in place.) • Full range debugging functions Supports realtime emulation at the MCU's maximum operating frequency. Break and trace functionality are implemented in the MCU's on-chip circuitry.

Target MCU: R32C/100 Series

Operating Environment: Microsoft Windows<sup>®</sup> XP, Windows<sup>®</sup> 2000

Product Contents

- Emulator unit
- Oscillator circuit board
- AC Adaptor
- AC power cableUSB cable, etc.

• Software CD-ROM (High-Performance Embedded Workshop integrated development environment)



Web

Low-priced on-chip debugging emulator that can also be used to program flash memory on 8-bit to 32-bit Renesas MCUs.

- A single unit provides support for on-chip debugging and flash programming.
- Since the actual MCU is used, evaluation can be performed under conditions, very close to those of the actual system such as electrical characteristics.
- The emulator uses USB bus power from the PC and does not require a separate power supply to operate.
- A 3.5V or 5.0V power supply may be provided to the target system via the emulator.
- The connector to the system under development and the debugger user interface are compatible with the E8 (discontinued product), facilitating a smooth transition.
- The following software is bundled with the product, so you can start application development immediately after purchasing it.
- High-performance Embedded Workshop integrated development environment
- Compiler package (evaluation version [free of charge])
   Flash Development Toolkit (evaluation version [free of charge])
- The bundled software can also be downloaded free of charge from the E8a emulator Web site.
- Compact design measuring 92mm × 42mm × 15mm (40% the volume of the E8).
- Case made of environmentally friendly polylactide, which is derived from vegetable matter.

Iain Specifications						
	Series	Group				
	M32C/80	M32C/80 M32C/84, M32C/85, M32C/87, M32C/88				
	M16C/60	M16C/62P, M16C/6N4, M16C/6N5, M16C/6NK, M16C/6NL, M16C/6NM, M16C/6NN, M16C/6S, M16C/64**, M16C/65**				
Towned MOULE in	M16C/30	M16C/30P				
larget MCUs in	M16C/Tiny	M16C/26A, M16C/28, M16C/29				
the M16C Family	R8C/Tiny	R8C/10, R8C/11, R8C/12, R8C/13, R8C/14, R8C/15, R8C/16, R8C/17, R8C/18, R8C/19, R8C/1A, R8C/18, R8C/20, R8C/21, R8C/22, R8C/24, R8C/24, R8C/25, R8C/26, R8C/27, R8C/28, R8C/29, R8C/24, R8C/26, R8C/2C, R8C/20, R8C/22 ★*, R8C/2F ★*, R8C/2G ★*, R8C/2H ★*, R8C/2J ★*, R8C/2K ★*, R8C/2L ★*				
Max. operating frequency	Max. operating frequency of target MCU					
Target MCU modes	Single-chip mode,	memory expansion mode (supported MCU modes differ depending on the MCU product)				
Supported power supply voltage	2.7V to 5.5V (within guaranteed flash programming operation range of target MCU)					
Power supply to MCU	Supplied by emulator (3.3V or 5.0V, max. 300mA) or from Vcc on user board.					
Software breaks	255 points					
Hardware breaks	Number of bre 4 address brea Otherwise 2 a	ak points differs depending on the MCU product. <sup>11</sup> ak points on R8C/Tiny Series (excluding R8C/10 to R8C/13). ddress break points + 1 data condition break point.				
Special breaks	Forced break	pushing the STOP button of debugger.				
Trace	Number of jun Jump source F Series (exclud	nps differs depending on the MCU product.* <sup>1</sup> PC trace (jump source address for latest 4 jumps) on R8C/Tiny ing R8C/10 to R8C/13).				
PC interface	USB 1.1/2.0 ft	III speed				
Operating environment	Windows <sup>®</sup> XP,	Windows <sup>®</sup> 2000				
User interface	14-pin connector (product No. 7614-6002, Sumitomo 3M Limited) (Sold separately.) Note: Compatible with E8.					
Connection to developer's system	Connects using supplied user interface cable. (Connection signals differ depending on the target MCU product.)*1					
Use of developer's resources	On some MCU models, the emulator may require access to some port peripheral functions and ROM or RAM.*1					
Dimensions (mm)	92×42×15					
Overseas standards	Compliant (FC	C standards, CE marking)				

\*1 Be sure to read the E8a user's manual corresponding to the target MCU before using the E8a emulator. See the E8a emulator Web site for details of target MCUs: http://www.renesas.com/e8a.



E8 emulator (discontinued product)

Although the E8a has replaced to the E8, support for new MCU models will continue to be added to the E8 through July 2008. (This will consist mainly of adding support for versions of existing products with new ROM/RAM configurations.) However, there are no plans to provide support for MCU products (740 Family, M16C/65 Group, etc.) that would require major changes to the emulator software.

# Flash Development Toolkit Mtp://www.renesas.com/fdt

An On-Board Programming Tool from Renesas. (Flash Development Toolkit)



#### **On-Chip Flash MCU Programming Environments**

http://www.renesas.com/flash\_programming\_tools

Web

A Variety of Flash Programming Environments Provided by Renesas.



# **Initial Implementation Tools**

Low-priced and Support for Basic Functions

## Renesas Starter Kit

This is a user-friendly evaluation tool for Renesas MCUs. The included E8a emulator and High-Performance Embedded Workshop integrated development environment provide support for coding and debugging. In addition, it is possible to perform on-board programming of MCUs using Flash Development Toolkit.

Lineup

Т	arget MCUs	Product name	Part No
Group	Series	Troduct name	Tarrivo.
M32C/80	M32C/84, 85, 87, 88	Renesas Starter Kit for M32C/87	R0K330879S000BE
M16C/60 M16C/62P, 30P		Renesas Starter Kit for M16C/62P	R0K33062PS000BE
	M16C/6NK	Renesas Starter Kit for M16C/6NK	R0K3306NKS000BE
M16C/Tiny	M16C/28, 29	Renesas Starter Kit for M16C/29	R0K330290S000BE
	M16C/26A	Renesas Starter Kit for M16C/26A	R0K33026AS000BE
R8C/Tiny	R8C/1A,1B	Renesas Starter Kit for R8C/1B	R0K5211B4S000BE
-	R8C/20-23	Renesas Starter Kit for R8C/23	R0K521237S000BE
	R8C/24, 25	Renesas Starter Kit for R8C/25	R0K521256S000BE
	R8C/26, 27	Renesas Starter Kit for R8C/27	R0K521276S000BE
	R8C/2C, 2D	Renesas Starter Kit for R8C/2D	R0K5212D8S000BE

**Product Contents** 

- CPU board
- E8a on-chip debugging emulator unit\*1
- Software CD-ROM
- High-performance Embedded Workshop integrated development environment
   Compiler (evaluation version [free of charge])
- E8a emulator debugger\*1
- Flash Development Toolkit (evaluation version [free of charge]), etc.
- Connecting cable, etc.
- \*1: Older kits may include E8 instead.

### M3A-0806

The M3A-0806 is a flash writer that uses standard serial I/O mode 2 (UART mode). It rewrites programs using only four lines (TxD, RxD, GND, and Vcc). If the supplied cable is used, there is no need for an RS-232C driver for the target board. Note that the M3A-0806 does not support rewriting of the data area.

- Package includes flash reprogramming software and a custom serial cable.
- Very economically priced flash writer

#### Target MCUs

R8C/10 to R8C/1B, R8C/20 to R8C/29, M16C/26A, M16C/28, M16C/29, M16C/62A, M16C/62M, M16C/62P, M16C/6N, M16C/80, M16C/30P, M32C/83, M32C/84, M32C/85, M32C/87

#### Operating Environment

Microsoft Windows® XP, Windows® 2000

Note: The flash rewriting (Flashstarter) software used by the M3A-0806 is distributed free of charge. The EXE file and source code are available for download from the Renesas Web site. http://www.renesas.com/download



Starter Kit

Note: The target board is not included.

# **Sample Application Program Generator & Organizer**

Simply select the functions you want to implement with your MCU and this free utility will generate sample code.

- Simple Operation
- Generates MCU sample programs and requires no complex environment settings.
- Flexible Settings Allows developers freely to combine code for different applications, such as communication control or data flash control.
- Improved Efficiency Allows developers to combine program code they have written themselves with other program code.
- Training Materials
   Detailed software reference materials are
   built in, such as MCU peripheral circuit
   diagrams and timing charts. C language source
   code output files include extensive comments.
- Free Download from the Renesas Web Site http://www.renesas.com/sango





# **Development Tools List**

#### Development Tools for R32C/100 Series

MCU				
Series	RTOS	C compiler package *2	IDE	Emulator
R32C/100	M3T-MR100/4 *1 *6	R32C/100 Series C compiler package (MISRA C *3)	High-performance Embedded Workshop *4	E30A *5 ★★

\*1. M3T-MR100/4 is a general term referring to the real-time OS development kit (M3T-MR100K/4) and the mass production contract (M3T-MR100S/4)

C compiler package includes integrated development environment (High-performance Embedded Workshop), C compiler, assembler and simulator debugger.

\*3. MISRA C rule checking functionality may be added by installing the optional SQMIint MISRA C rule checker. \*4. High-performance Embedded Workshop is included with C compiler package and Emulator software.

\*5. E30A emulator bundles emulator software.

\*6. Please refer to the following URL for the target MCU group (http://www.renesas.com/r32c100)

★★ Under development or evaluation: product name may be changed.

#### Operating Environment for R32C/100 Series Software Tools

Product type	Product name	Host machine (OS) *6
RTOS	M3T-MR100/4 *1	IBM PC/AT compatibles (Windows <sup>®</sup> XP, 2000)
C compiler package	C compiler package for R32C/100 Series *2	IBM PC/AT compatibles (Windows® XP, 2000)
MISRA C rule checker	SQMIint *3	IBM PC/AT compatibles (Windows® XP, 2000)
IDE	High-performance Embedded Workshop *4	IBM PC/AT compatibles (Windows <sup>®</sup> XP, 2000)
Simulator debugger	Simulator Debugger for R32C *5	IBM PC/AT compatibles (Windows® XP, 2000)

\*1. M3T-MR100/4 is a general term referring to the real-time OS development kit (M3T-MR100K/4) and the mass production contract (M3T-MR100S/4). \*2. The C compiler package for R32C/100 Series includes an integrated development environment (High-Performance Embedded Workshop), C compiler, assembler and simulator debugger.

assertion and simulation debugger.
3. SQMInt MISRA C rule checker (Part No.: R0C00000SCW01R) is sold as the optional product of Renesas C compiler.
\*4. High-performance Embedded Workshop is included with C compiler package and Emulator debugger.

\*5. Simulator debugger is included with C compiler package.

\*6. Please refer to the following URL for Windows® Vista. http://www.renesas.com/tool\_env

#### Development Tools for M32C/80 Series 80

MCU		Introductory tools		Software tools			Emulator (included emula	tor debugger *	7)	Programming tool	
Series	Group	Starter kit	RTOS	C compiler package	IDE	Onchip debugging emulator	Compact emulator	Emulator	rcuit emulator Emulation probe	Flash programmer *10	IC socket board *13
	M32C/80					_	M30850T3-CPE *8		M30850T2-EPB	_	
	M32C/82	_					-		M30830T-EPB *9	_	_
M32C/80	M32C/84 (M32C/84, M32C/84T) M32C/85 (M32C/85, M32C/85T)	-					M30850T3-CPE *8		M30850T2-EPB	Flash Development Toolkit *11 (E8a emulator is necessary at programming)	R0K3100PSZ000BR (for PRQP0100JB-A [Previous code: 100P6S-A]) R0K3100PQZ000BR (for PLQP0100KB-A [Previous code: 100PSC-4])
	M32C/87 (M32C/87, M32C/87A, M32C/87B)	M32C/87 (Type No. : *2 R0K330879S000BE)	108/4 M3T-NC308WA High-p *3 (MISRA C *4)	High-performance Embedded Workshop *5	E8a *6	M30870T2-CPE	PC7501 M30870T-I	M30870T-EPB	M3A-0806 *12	[Previous code: 100F60-A] ) R0K3144PSZ000BR (for PLQP0144KA-A [Previous code: 144P6Q-A] )	
	M32C/88 (M32C/88T)						_		M30880T-EPB	Flash Development Toolkit *11 (E8a emulator is necessary at programming)	R0K3100POZ000BR (for PLQP0100KB-A [Previous code: 100P6Q-A]) R0K3144PSZ000BR (for PLQP0144KA-A [Previous code: 144P6Q-A])
	M32C/8A	_	1			-	M30850T3-CPE *8	1	M30850T2-EPB	_	_

\*2. \*3. \*4. \*5. \*6.

Each emulator includes an emulator debugger. Depending on the shipping date, the bundled emulator debugger may include products or versions that are not the most recent noos gravitable. The latest versions may be downloaded (the of charge) from the Renesas Technology in the Strephone State (thtp://www.renesas.com/download). The M3085012-CPE. The M3085013-CPE subsports allocation of emulation memory to an external area and microprocessor mode using the optional R0E330850MSRC0 emulation memory board. The M302612 Group can be used with the combination of an emulator debugger, the PC4701U emulation and the M3085017-PCE - emulation processor mode using the optional R0E330850MSRC0 emulation memory board. A variety of compatible programmer gate valiable. The latent states are the M3085012-CPE. The M3085013-CPE is the successor to the M3085012-CPE. The M3085013-CPE and the manufacture regarding programmer details, supported that is, supported tables, suppo \*7.

\*10. \*11.

\*12. \*13.

<b>80</b>	Accessories for M32C/80 Series
-----------	--------------------------------

	MCU	Accessories					
Series	Group	Package type	Package name	Previous code	Recommended accessories *1		
	M200/90	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)		
	M32C/80	100 pin 0.65mm pitch QFP	100 pin 0.65mm pitch QFP PRQP0100JB-A 100P6S-A		M3T-F160-100NRB (optional)		
	M32C/82	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)		
	M32C/84 (M32C/84, M32C/84T) M32C/85 (M32C/85, M32C/85T)	100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3T-F160-100NRB (optional)		
M32C/80 -	M32C/87 (M32C/87, M32C/87A, M32C/87B)	144 pin 0.5mm pitch LQFP	PLQP0144KA-A	144P6Q-A	M3T-FLX-144NSD (optional)		
	M22C/00 (M22C/00T)	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)		
	M32C/88 (M32C/88T)	144 pin 0.5mm pitch LQFP	PLQP0144KA-A	144P6Q-A	M3T-FLX-144NSD (optional)		
	M32C/8A	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)		

\*1. A variety of other accessories are available. Visit the Renesas Technology Web site (http://www.renesas.com/accessory) for details.

(optional): Not included with compact emulator or emulation probe. Purchase it separately.

#### BO Development Tools for M16C/80 Series

MCU		Software tools			Emulator (bundled Emulator debugger *5)			Programming tool	
Corioo	Crown	TROS	C compiler package	IDE	Compact emulator	In-circuit emulator		Electh programmer	IO acclust be and t7
Genes	Gioup					Emulator	Emulation pod or Probe	Flash programmer	IC SOCKET DOARD 7
M16C/80	M16C/80	M3T-MR308/4 *1	M3T-NC308WA *2 (MISRA C *3)	High-performance Embedded Workshop *4	M30800T-CPE (RAM 10K)	PC4701U	M30803T-RPD-E (RAM 24K) *6	M3A-0806	R0K3100PS2000BR (for PRQP0100JB-A [Previous code: 100P6S-A]) R0K3100PQ2000BR (for PLQP0100KB-A [Previous code: 100P6Q-A]) R0K3144PS2000BR (for PLQP0144KA-A [Previous code: 144P6Q-A])
*1 M3T-MR308/4 is a	M3T.MR308/4 is a general term referring to the real-time OS development kit (M3T.MR308K/4) and the mass production contract (M3T.MR308S/4)								

<sup>11</sup>. M3TMR30/4 is a general term referring to the real-time OS development ki (M3TMR308/4) and the mass production contract (M3T-MR308/4).
<sup>12</sup>. The M3TNc508W includes an integrated development environment (High-Performance Embedded Workshop), C complex, assembler and simulator debugger.
<sup>13</sup>. MISRA C rule checking functionality may be added by installing the optional SOMIint MISRA C rule checker (Part No.: R0C0000SCW01R).
<sup>14</sup>. High-performance Embedded Workshop is included with C complex pradate gate.
<sup>15</sup>. Each emulator includes an emulator debugger. Depending on the shipping date, the bundled emulator debugger may include products or versions that are not the most recent ones available.
<sup>16</sup>. The last event sions may be downloaded (free of large) from the Renessa Technology Web site (http://www.renessa.com/download).
<sup>16</sup>. Please contact us when you use this for the M16C/80T Group for automotive applications.
<sup>17</sup>. The IC Sockbard is and is support a specific programmer.

#### 80 Accessories for M16C/80 Series

M	CU	Accessories						
Series	Group	Package type	Package name	Previous code	Recommended accessories *1			
		100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)			
M16C/80	M16C/80	100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M30800T-PTC (included) + M3T-100LCC-DMS (optional) + M3T-FLX-100NRB (optional)			
	-	144 pin 0.5mm pitch LQFP	PLQP0144KA-A	144P6Q-A	M3T-FLX-144NSD (optional)			

\*1. A variety of other accessories are available. Visit the Renesas Technology Web site (http://www.renesas.com/accessory) for details. (optional): Not included with emulation pod or probe. Purchase it separately. (included): Included with emulation pod or probe.

# **Development Tools List**

#### 80 Operating Environment for M32C/80 and M16C/80 Series Software Tools

Product type Product name		Host machine (OS) *8
RTOS	M3T-MR308/4 *1	IBM PC/AT compatibles (Windows® XP, 2000)
C compiler package	M3T-NC308WA *2	IBM PC/AT compatibles (Windows® XP, 2000)
MISRA C rule checker	SQMIint *3	IBM PC/AT compatibles (Windows® XP, 2000)
IDE	High-performance Embedded Workshop *4	IBM PC/AT compatibles (Windows® XP, 2000)
Simulator debugger	Simulator Debugger for M32C *5	IBM PC/AT compatibles (Windows® XP, 2000)
Emulator debugger	PC7501 Emulator Debugger for M32C Series *6 PC4701 Emulator Debugger for M32C Series *6 Compact Emulator Debugger for M32C Series *6 FoUSB/UART Debugger for M32C Series *6 E8a Emulator Software *6	IBM PC/AT compatibles (Windows® XP, 2000)
Flash and PROM Programming	Flash Development Toolkit *7	IBM PC/AT compatibles (Windows® XP, 2000)

\*1. M3T-MR308/4 is a general term referring to the real-time OS development kit (M3T-MR308K/4) and the mass production contract (M3T-MR308S/4)

\*2. The M3T-NC308WA includes an integrated development environment (High-Performance Embedded Workshop), C compiler, assembler and simulator debugger. \*3. SQMIint MISRA C rule checker (Part No.: R0C00000SCW01R) is sold as the optional product of Renesas C compiler.

\*4. High-performance Embedded Workshop is included with C compiler package and Emulator debugger.

\*5. Simulator debugger is included with C compiler package.

\*6. Emulator debugger is bundled with emulators

\*7. Flash Development Toolkit (Part No.: R0C00000FDW04R) is available in a product version (with technical support) and an evaluation version (without technical support).

The E8a emulator (Part No.: R0E00008AKCE00) is necessary for programming. Visit the Renesas Technology Web site (http://www.renesas.com/fdt) to confirm support details for specific MCU product numbers.

\*8. Please refer to the following URL for Windows® Vista. http://www.renesas.com/tool\_env

### 60 30 20 10 Development tools for M16C/60, 30, 20, and 10 Series

	MCU Introductory tools Software tools Emulator (included Emulator debugger *7)		Programming tool																
Series	Group	MCU	Starter kit	RTOS	C compiler package	IDE	Onchip debugging emulator	Compact emulator	Ir Emulator	-circuit emulator Emulation probe or pod	Flash programmer *16	IC socket board *21							
	M16C/ M16C/	/64 <b>**</b> /65 <b>*</b> *	**				E8a *6 **	-	E100 **	*22 ★★	Flash Development Toolkit *19 ** (E8a emulator is necessary at programming)	_							
	M160	C/62A	Renesas Starter Kit for					M30620T-CPE		M30620T2-RPD-E									
	M16C	C/62M	M16C/62P (R0K33062PS000BE) *1				M3A-0665	_	PC4701U	M30620TL-RPD-E	M3A-0806 *17 *18	R0K3100PSZ000BR (for PRQP0100JB-A [Previous							
	M160	C/62N	-							M3062NT3-RPD-E	M3A-0806 *17	code: 100P6S-A])							
M16C/60	M160	M16C/62P Renesas Starter Kit for M16C/62P (R0K33062PS000BE) *1												E8a *6	M3062PT3-CPE *8	PC7501	M3062PT2-EPB *10	Flash Development Toolkit *19 (E8a emulator is necessary at programming) or M3A-0806 *17	(for PLQP0100KB-A [Previous code: 100P6Q-A])
	M16C/6V	M306V7				NC30WA *3 SRA C *4) High-performance Embeddied Workshop *5	-		PC4701U	M306V7T-RPD-E	M3A-0665 *20	_							
	M16C/6N	M306N4 M306N5 M306NK M306NL M306NM M306NN		M3T-MR30/4 *2	M3T-NC30WA *3 (MISRA C *4)		High-performance Embedded Workshop *5	E8a *6	_	PC7501	M306NKT-EPB *11	Flash Development Toolkit *19 (E8a emulator is necessary at programming) or M3A-0806 *17	R0K3100PSZ000BR (for PRQP0100JB-A [Previous code: 100P6S-A]) R0K3100PQZ000BR (for PLQP0100KB-A [Previous code: 100P6Q-A])						
	M16C/6H	M306H7					-	]	PC4701U	M306H7T3-RPD-E	_								
	M16C/6S	M306S0	_				E8a *6	M3062PT3-CPE + M306S0T-PRB *9	PC7501	M3062PT2-EPB *12 + M306S0T-PRB *9	Flash Development Toolkit *19 (E8a emulator is necessary at								
M16C/20	M16C/30P	M30302 M30304	Renesas Starter Kit for M16C/62P (R0K33062PS000BE) *1				E8a *6	M3062PT3-CPE *8	PC7501	M3062PT2-EPB *10	programming) or M3A-0806 *17	_							
	M16C/39P	M30392								M3062PT2-EPB *13 + M30396T-PRB *14	_								
M16C/20	M16C/24	M30245	-				-	-		M30245T3-RPD-E	*16								
M16C/10	M16C/1N	M301N2							PC4701U	M30100T3-RPD-E + M301N2T-PRB *15	M3A-0806 *17								

\*2. \*3. \*4. \*5. \*6.

 
 HisC/In
 MisOIN2
 MisOIN2+PRB 115
 MisOIN2+PRB 115

 CPU board, E5 on-chip debugging emulator, software (High-Performance Embedded Workshop integrated development environment, MST-NC30WA C compiler package evaluation version, E5 emulator software, Flash Development Tookit evaluation version, etc., are included.

 MSTMR204 is a general term referring to the real-time CS development Kill MST-MR30K(4) and the mass production contract (MST-MR30K).
 MSTMR20K/1
 MSTMR20K/1</td \*7.

\*8. \*9. \*11 \*12 \*13 \*14 \*15 \*16 \*17 \*18

\*19.

Note: Evaluation versions of software tools are free of charge.

Please refer to the following URL for details (http://www.renesas.com/tool\_evaluation).

	80 20 Set Package of Compact Emulators for M16C/62P and M16C/30P Group									
			Target MCU							
Series Group	Package type	Package name	Previous code	Product Type name	Components *1					
	80 pin 0.65mm pitch QFP	PRQP0080JA-A	80P6S-A	M3062PT3-CPE-1	Compact emulator M3062PT3-CPE *2 Converter board M3062PT-80FPB					
	M16C/60 M16C/6 M16C/30 M16C/3		100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3062PT3-CPE-2	Compact emulator M3062PT3-CPE *2 Converter board M30800T-PTC IC socket IC61-1004-051			
		M16C/62P M16C/30P				M3062PT3-CPE-5	Compact emulator M3062PT3-CPE *2 Converter board M3T-F160-100NRB			
		-	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3062PT3-CPE-3	Compact emulator M3062PT3-CPE *2 Converter board M3T-F160-100NSD			
			128 pin 0.5mm pitch LQFP PLQP0128KB-A		128P6Q-A	M3062PT3-CPE-4	Compact emulator M3062PT3-CPE *2 Converter board M3T-FLX-128NRD			

\*1. For debugging, the combination of a compact emulator and a conversion board supporting the target MCU are used to connect to the user's system. Compact emulators and conversion boards can be purchased individually.
 \*2. With the optional emulation memory board R0E33062PMSRC0, emulation memory allocation function and microprocessor mode are available.

### 60 30 20 10 Accessories for M16C/60, 30, 20, and 10 Series

MCU			Accessories						
Series	Group	MCU	Package type	Package name	Previous code	Recommended accessories *1	Emulator		
	M16C/	′64 ★★	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	**	E100 4 4		
	M16C/	65 ★★	100 pin 0.65mm pitch QFP	PRQP0100JD-B	100P6F-A	**			
	M160	2/62 4	80 pin 0.65mm pitch QFP	PRQP0080JA-A	80P6S-A	M3T-FLX-100LCC (included) + M3T-100LCC-80QSB (optional)			
	M16C/62M		M16C/62M 100		100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-FLX-100NSD (optional)	PC4701U
			100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3T-FLX-100NRB (optional)			
			80 pin 0.65mm pitch QFP	PRQP0080JA-A	80P6S-A	M3062PT-80FPB (optional)			
			100 pin 0.4mm pitch TQFP	PTQP0100LB-A	100PFB-A	M3T-F160-100NSE (optional)	DOATONI		
	IVITO	2/02IN	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)	PC47010		
			100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3T-F160-100NRB (optional)			
			80 pin 0.65mm pitch QFP	PRQP0080JA-A	80P6S-A	M3062PT-80FPB (optional)			
M16C/60	M16C/62P		100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)	PC7501		
			100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3T-F160-100NRB (optional)			
			128 pin 0.5mm pitch LQFP	PLQP0128KB-A	128P6Q-A	M3T-F160-128NRD (optional)			
	M16C/6V	M306V7	100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3T-F160-100NRB (optional)	PC4701U		
		M306N4	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)			
		M306N5	100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3T-F160-100NRB (optional)			
	M16C/6N	M306NK M306NL	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)	PC7501		
		M306NM M306NN	128 pin 0.5mm pitch LQFP	PLQP0128KB-A	128P6Q-A	M3T-F160-128NRD (optional)			
	M16C/6H	M306H7	100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M30800T-PTC (included) + LCC socket (included)	PC4701U		
	M16C/6S	M306S0	64 pin 0.5mm pitch LQFP	PLQP0064KB-A	64P6Q-A	*2	PC7501		
	M1CC/00D	M30302	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-F160-100NSD (optional)			
M16C/30	W160/30P	M30304	100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3T-F160-100NRB (optional)	PC7501		
	M16C/39P	M30392	100 pin 0.65mm pitch QFP	PRQP0100JB-A	100P6S-A	M3T-F160-100NRB (optional)			
M16C/20	M16C/24	M30245	100 pin 0.5mm pitch LQFP	PLQP0100KB-A	100P6Q-A	M3T-FLX-100NSD (included)	DC 4701U		
M16C/10	M16C/1N	M301N2	48 pin 0.5mm pitch LQFP	PLQP0048KB-A	48P6Q-A	M30102T-PTC (optional)	PC4/010		

\*1. A variety of other accessories are available. Visit the Renesas Technology Web site (http://www.renesas.com/accessory) for details.
\*2. Accessories are attached to signal conversion board M306S0T-PRB. (included): Included with compact emulator, emulation pod or probe. (optional): Not included with compact emulator, emulation pod or probe. Purchase it separately.
\*\* Under development

# **Development Tools List**

### 60 30 20 10 Operating Environment for M16C/60, 30, 20, and 10 Series Software Tools

Product type	Product name	Host machine (OS) *8
RTOS	M3T-MR30/4 *1	IBM PC/AT compatibles (Windows® XP, 2000)
C compiler package	M3T-NC30WA *2	IBM PC/AT compatibles (Windows® XP, 2000)
MISRA C rule checker	SQMIint *3	IBM PC/AT compatibles (Windows® XP, 2000)
IDE	High-performance Embedded Workshop *4	IBM PC/AT compatibles (Windows® XP, 2000)
Simulator debugger	Simulator Debugger for M16C and R8C/Tiny Series *5	IBM PC/AT compatibles (Windows® XP, 2000)
Emulator debugger	PC7501 Emulator Debugger for M16C and R8C/Tiny Series *6 PC4701 Emulator Debugger for M16C Series *6 Compact Emulator Debugger for M16C and R8C/Tiny Series *6 FoUSB/UART Debugger for M16C and R8C/Tiny Series *6 E8a Emulator Software *6	IBM PC/AT compatibles (Windows® XP, 2000)
Flash and PROM Programming	Flash Development Toolkit *7	IBM PC/AT compatibles (Windows® XP, 2000)

\*1. M3T-MR30/4 is a general term referring to the real-time OS development kit (M3T-MR30K/4) and the mass production contract (M3T-MR30S/4).

The M3T-NC30WA includes an integrated development environment (High-Performance Embedded Workshop), C compiler, assembler and simulator debugger.
 SQMIint MISRA C rule checker (Part No.: R0C00000SCW01R) is sold as the optional product of Renesas C compiler.
 High-performance Embedded Workshop is included with C compiler package and Emulator debugger.

\*5. Simulator debugger is included with C compiler package.

\*6. Emulator debugger is bundled with emulators

\*7. Flash Development Toolkit (Part No.: R0C00000FDW04R) is available in a product version (with technical support) and an evaluation version (without technical support).

The E8a emulator (Part No.: R0E00008AKCE00) is necessary for programming. Visit the Renesas Technology Web site (http://www.renesas.com/fdt) to confirm support details for specific MCU product numbers

\*8. Please refer to the following URL for Windows® Vista.

http://www.renesas.com/tool\_env

#### Development tools for M16C/Tiny Series

	MCU		Introductory tool		Software tool		Emulator (Emulator debugger is included. *6)			*6)	Programming tool	
					Compiler		Onchip	Compost	In-circuit emulator		Floop	IC analyst
Series Group	Group	up MCU	Starter kit	RTOS	package	IDE	debugging emulator	emulator	Emulator	Emulation probe	Programmer *12	board *13
	M16C/26A	M30260	Renesas Starter Kit for									R0K3048PQZ000BR
	(M16C/26A, M16C/26B, M16C/26T)	M30263	M16C/26A (R0K33026AS000BE) *1	E) *1							Flash Development Toolkit (R0C00000FDW04R) *10	(for PLQP0048KB-A [Previous code: 48P6Q-A])
M16C/Tiny	M16C/28	M30280	M3T-MR30/4 *2 Renesas Starter Kit for	M3T-NC30WA *3	Embedded Workshop	E8a	M3028BT2-CPE	PC7501	M3028BT-EPB	(E8a emulator is necessary at	R0K3064PQZ000BR	
	(M16C/28, M16C/28B)	M30281		(MISHA C	(WISHA C 4)	*5	(RUEUUUUSAKCEUU) 7	°		-9	or M3A-0806 *11	(tor PLQP100KB-A [Previous code: 64P6Q-A])
	M16C/20	M30290	(R0K330290S000BE) *1	(R0K330290S000BE) *1	0K330290S000BE) *1							R0K3080PQZ000BR (for PLOP0080KB-A [Previous code:
	W100/29	M30291										80P6Q-A])

\*2. \*3. \*4. \*5. \*6.

 Mode 
 M \*7 \*8.

\*9.

\*10

#### Set Package of Compact emulator for M16C/Tiny Series

Series	Group	MCU	Та	rget MCU		- Product name	Components *1	
	Group	IVICO	Package type	Package name	Previous code	Floduct hame		
M160 (M160 M160 M160	M16C/26A (M16C/26A,	M30263	42 pin 0.8mm pitch SSOP	PRSP0042GA-B	42P2R-E	M3028BT2-CPE-1	Compact emulator M3028BT2-CPE Converter board M30263T-42SSB	
	M16C/26B, M16C/26T)	M30260	48 pin 0.5mm pitch LQFP	PLQP0048KB-A	48P6Q-A	M3028BT2-CPE-2	Compact emulator M3028BT2-CPE Converter board M30260T-48FPD	
M16C/Tiny	M16C/28 (M16C/28, M16C/28B) M16C/29	M30281 M30291	64 pin 0.5mm pitch LQFP	PLQP0064KB-A	64P6Q-A	M3028BT2-CPE-3	Compact emulator M3028BT2-CPE Converter board M30291T-64FPD	
-		M30280 M30290	80 pin 0.5mm pitch LQFP	PLQP0080KB-A	80P6Q-A	M3028BT2-CPE-4	Compact emulator M3028BT2-CPE Converter board M30290T-80FPD	
	M16C/28 (M16C/28, M16C/28B)	M30280	85 pin 0.65mm pitch TFLGA	PTLG0085JB-A	85F0G	M3028BT2-CPE-5	Compact emulator M3028BT2-CPE Converter board M30280T-85LGF	

\*1. For debugging, the combination of a compact emulator and a conversion board supporting the target MCU are used to connect to the user's system. Compact emulators and conversion boards can be purchased individually

MACC	Ś	
MIOC	m	
<b>F</b> <sup>2</sup>	2	
ΠV		

#### Set Package of PC7501 Emulation probe for M16C/Tiny Series

Sorioo	Group	MCU	Tai	rget MCU		Broduct nome	Components *1	
Genes	Group	IVICO	Package type	Package name	Previous code	Froduct name		
M16C/Tiny	M16C/26A (M16C/26A,	M30263	42 pin 0.8mm pitch SSOP	PRSP0042GA-B	42P2R-E	M3028BT-EPB-1	Emulation probe M3028BT-EPB Converter board M30263T-42SSB	
	M16C/26B, M16C/26T)	M30260	48 pin 0.5mm pitch LQFP	PLQP0048KB-A	48P6Q-A	M3028BT-EPB-2	Emulation probe M3028BT-EPB Converter board M30260T-48FPD	
	M16C/28 (M16C/28, M16C/28B) M16C/29	M30281 M30291	64 pin 0.5mm pitch LQFP	PLQP0064KB-A	64P6Q-A	M3028BT-EPB-3	Emulation probe M3028BT-EPB Converter board M30291T-64FPD	
		M30280 M30290	80 pin 0.5mm pitch LQFP	PLQP0080KB-A	80P6Q-A	M3028BT-EPB-4	Emulation probe M3028BT-EPB Converter board M30290T-80FPD	
	M16C/28 (M16C/28, M16C/28B)	M30280	85 pin 0.65mm pitch TFLGA	PTLG0085JB-A	85F0G	M3028BT-EPB-5	Emulation probe M3028BT-EPB Converter board M30280T-85LGF	

\*1. For debugging, the combination of an emulation probe and a conversion board supporting the target MCU are used to connect to the user's system. Emulation probes and conversion boards can be purchased individually

#### Tiny Converter Board for M16C/Tiny Series \*1

Cariaa	Crown	MCU	Т		Broduct name		
Selles	Group	MCO	Package type	Package name	Previous code	Flouderhame	
M16C/Tiny	M16C/26A	M30263	42 pin 0.8mm pitch SSOP	PRSP0042GA-B	42P2R-E	M30263T-42SSB	
	(M16C/26A, M16C/26B, M16C/26T)	M30260	48 pin 0.5mm pitch LQFP	PLQP0048KB-A	48P6Q-A	M30260T-48FPD	
	M16C/28	M30281 M30291	64 pin 0.5mm pitch LQFP	PLQP0064KB-A	64P6Q-A	M30291T-64FPD	
	M16C/29	M30280 M30290	80 pin 0.5mm pitch LQFP	PLQP0080KB-A	80P6Q-A	M30290T-80FPD	
	M16C/28 (M16C/28, M16C/28B)	M30280	85 pin 0.65mm pitch TFLGA	PTLG0085JB-A	85F0G	M30280T-85LGF	

\*1. A variety of other accessories are available. Visit the Renesas Technology Web site (http://www.renesas.com/accessory) for details.

#### Tiny Operating Environment for M16C/Tiny Series Software Tools

Product type	Product name	Host machine (OS) *8
RTOS	M3T-MR30/4 *1	IBM PC/AT compatibles (Windows® XP, 2000)
C compiler package	M3T-NC30WA *2	IBM PC/AT compatibles (Windows® XP, 2000)
MISRA C rule checker	SQMlint *3	IBM PC/AT compatibles (Windows® XP, 2000)
IDE	High-performance Embedded Workshop *4	IBM PC/AT compatibles (Windows® XP, 2000)
Simulator debugger	Simulator Debugger for M16C and R8C/Tiny Series *5	IBM PC/AT compatibles (Windows® XP, 2000)
Emulator debugger	PC7501 Emulator Debugger for M16C and R8C/Tiny Series *6 Compact Emulator Debugger for M16C and R8C/Tiny Series *6 E8a Emulator Software *6	IBM PC/AT compatibles (Windows® XP, 2000)
Flash and PROM Programming	Flash Development Toolkit *7	IBM PC/AT compatibles (Windows® XP, 2000)

\*1. M3T-MR30/4 is a general term referring to the real-time OS development kit (M3T-MR30K/4) and the mass production contract (M3T-MR30S/4). \*2. The M3T-NC30WA includes an integrated development environment (High-Performance Embedded Workshop), C compiler, assembler and simulator debugger.

SQMInt MISRA C rule checker (Part No.: R0C00000SCW01R) is sold as the optional product of Renesas C compiler.
 High-performance Embedded Workshop is included with C compiler package and Emulator debugger.
 Simulator debugger is included with C compiler package.

\*6. Emulator debugger is bundled with emulators.
 \*7. Flash Development Toolkit (Part No.: R0C00000FDW04R) is available in a product version (with technical support) and an evaluation version (without technical support). The E8a emulator (Part No.: R0E00008AKCE00) is necessary for programming. Visit the Renesas Technology Web site (http://www.renesas.com/fdt)

to confirm support details for specific MCU product numbers.
\*8. Please refer to the following URL for Windows® Vista. http://www.renesas.com/tool\_env

Note: Evaluation versions of software tools are free of charge.

Please refer to the following URL for details (http://www.renesas.com/tool\_evaluation).

# **Development Tools List**

#### The Development tools for R8C/Tiny Series

N	ICU	Introductory tool		Software tool		En	ulator (Emulator debugg	ger is included	. *6)	Programming	tool
				0		Onchip		In-c	ircuit emulator		
Series	Group	Starter kit *1	RTOS	package *3	IDE	debugging emulator	Compact emulator	Emulator	Emulation probe	Flash Programmer *12	IC socket board *13
	R8C/18										
	R8C/19										M34-0114
	R8C/1A	Renesas Starter Kit for R8C/1B								Elash Development Toolkit	moreterie
	R8C/1B	(R0K5211B4S000BE)								(R0C00000FDW04R) *10	
	R8C/20									(E8a emulator is necessary at programming.)	
	R8C/21	Renesas Starter Kit for R8C/23								or	B0K521238Z000BB
	R8C/22	(R0K521237S000BE)								M16C Flash Starter M3A-0806 *11	
	R8C/23										
	R8C/24	Renesas Starter Kit for R8C/25		M3T-NC30WA *2		E8a (R0E00008AKCE00)	R0E521000CPE00	PC7501	R0E521000EPB00		R0K521258Z000BR
	R8C/25	(R0K521256S000BE)		(MISRA C *4)		*7	-8		-9		
	R8C/26	Renesas Starter Kit for R8C/27									R0K521276Z000BR
	R8C/27	(H0K521276S000BE)									
	R8C/28									Flash Development Toolkit	_
	R8C/29	_			High-performance					(R0C00000FDW04R) *10	
R8C/Tiny	R8C/2A		M3T-MR30/4 *14		Embedded					programming.)	**
	R8C/2B				Workshop '5						
	R8C/2C	Renesas Starter Kit for R8C/2D									R0K5212D8Z000BR
	R8C/2D	(10/321200300002)	-		-						
	H8C/2E										
	R8C/2F										
	**										
	R8C/2G						_	_	_	Elech Development Teallrit	
	Dec/ou			M3T-NC30WA *2		E8a (POE00008AKCE00)				(R0C00000FDW04R) *10	
	**	—		** (MISBA C *4)		*7				★★ (F8a emulator is necessary at	-
	R8C/2J **			(141101104 0 4)		**				programming.)	
	R8C/2K						DAEFOLOOODEOO		DOFFORMONEDDOO	1	
	**						*8	PC7501	*9		
	R8C/2L **						**		**		

\*2. \*3. \*4. \*5. \*6.

CPU back the bunched software may include products or versions that are not the most recent ones available. The latest versions may be downloaded (free of charge) from the Renessas Technology Web site (http://www.renessas.com/download). How MSTAR C rule checking functionary include products or versions that are not the most recent ones available. The latest versions may be downloaded (free of charge) from the Renessas Technology Web site (http://www.renessas.com/download). How MSTAR C rule checking functionary include products or versions that are not the most recent ones available. The latest versions may be downloaded (free of charge) from the Renessas Technology Web site (http://www.renessas.com/download). How MSTAR C rule checking functionary include products or versions that are not the most recent ones available. The latest versions may be downloaded (free of charge) from the Renessas Technology Web site (http://www.renessas.com/download). The Ease anulator (Path No: ROE0000BAKCE00) includes emulator software (High-Pedromance Embedded Workshop) integrated development environment. Ease emulator software, compiler evaluation version, Riash Development Toolkit evaluation version), Depending on the shipping date, the bundled emulator advares, comversion baard for the target connection is anothed emulator and the conversion baard are also available. For details, please refer to the lists of Set Package of Compact Emulator for RBCTing Series. The conversion board for the target connection is necessary for RBCSE 1000CPEB0. The set sales of the emulator and the conversion board are also available. For details, please refer to the lists of Set Package of Compact Emulator for RBCTing Series. The conversion board for the target connection is necessary for RBCSE 1000CPEB0. The set sales of the emulator and the conversion board are also available. For details, please refer to the lists of Set Package of CPC301 Emulation Probe for RBCTing Series. The conversion board for the target connection is necessary for RB \*7.

\*8. \*9. \*10

\*11. \*12. \*13. \*14.

Tiny Set	Pac	kage of Compact Emul	ator for R8C/Tiny	y Series	
		Target MCU	Product name	Comp (Compact emulator and converte	onents er board are also sold separately.)
Group		Package name		Compact emulator	Converter board *1
R8C/18 R8C/19		PLSP0020JB-A Previous code : 20P2F-A (20-pin 0.65mm-pitch LSSOP)	R0E521174CPE00		R0E521174CSJ00
R8C/1A R8C/1B	5	PRDP0020BA-A Previous code : 20P4B (20-pin 1.778mm-pitch SDIP)	R0E521174CPE10		R0E521174CDB00
R8C/20 R8C/21 R8C/22 R8C/23		PLQP0048KB-A Previous code : 48P6Q-A (48-pin 0.5mm-pitch LQFP)	R0E521237CPE00		R0E521237CFK00
R8C/24 R8C/25		PLQP0052JA-A Previous code : 52P6A-A (52-pin 0.65mm-pitch LQFP)	R0E521258CPE00		R0E521258CFJ00
R8C/26 R8C/27		PLQP0032GB-A Previous code : 32P6U-A (32-pin 0.8mm-pitch LQFP)	R0E521276CPE00	R0E521000CPE00	R0E521276CFG00
R8C/28 R8C/29		PLSP0020JB-A Previous code : 20P2F-A (20-pin 0.65mm-pitch LSSOP)	R0E521174CPE00		R0E521174CSJ00
R8C/2A		PLQP0064KB-A Previous code : 64P6Q-A (64-pin 0.5mm-pitch LQFP)	R0E5212BACPE10		R0E5212BACFK00
R8C/2B	5	PLQP0064GA-A Previous code : 64P6U-A (64-pin 0.8mm-pitch LQFP)	R0E5212BACPE00		R0E5212BACFG00
R8C/2C R8C/2D		PLQP0080KB-A Previous code : 80P6Q-A (80-pin 0.5mm-pitch LQFP)	R0E5212DACPE00		R0E5212DACFK00
R8C/2K	**	PLQP0032GB-A Previous code : 32P6LI-A	B0E5212L4CPE00		B0E5212L4CEG00
R8C/2L	**	(32-pin 0.8mm-pitch LQFP)			

\*1. Converter board, socket for user system connection and user's manual are included. ★★Under development

# **Development Tools List**

### Set Package of PC7501 Emulation probe for R8C/Tiny Series

	Target MCU	Product name	Comp (Compact emulator and converte	onents er board are also sold separately.)
Group	Package name		Compact emulator	Converter board *1
R8C/18 R8C/19	PLSP0020JB-A Previous code : 20P2F-A (20-pin 0.65mm-pitch LSSOP)	R0E521174EPB00		R0E521174CSJ00
R8C/1A R8C/1B	PRDP0020BA-A Previous code : 20P4B (20-pin 1.778mm-pitch SDIP)	R0E521174EPB10		R0E521174CDB00
R8C/20 R8C/21 R8C/22 R8C/23	PLQP0048KB-A Previous code : 48P6Q-A (48-pin 0.5mm-pitch LQFP)	R0E521237EPB00		R0E521237CFK00
R8C/24 R8C/25	PLQP0052JA-A Previous code : 52P6A-A (52-pin 0.65mm-pitch LQFP)	R0E521258EPB00	-	R0E521258CFJ00
R8C/26 R8C/27	PLQP0032GB-A Previous code : 32P6U-A (32-pin 0.8mm-pitch LQFP)	R0E521276EPB00	R0E521000EPB00	R0E521276CFG00
R8C/28 R8C/29	PLSP0020JB-A Previous code : 20P2F-A (20-pin 0.65mm-pitch LSSOP)	R0E521174EPB00		R0E521174CSJ00
R8C/2A	PLQP0064KB-A Previous code : 64P6Q-A (64-pin 0.5mm-pitch LQFP)	R0E5212BAEPB10		R0E5212BACFK00
R8C/2B	PLQP0064GA-A Previous code : 64P6U-A (64-pin 0.8mm-pitch LQFP)	R0E5212BAEPB00		R0E5212BACFG00
R8C/2C R8C/2D	(PLQP0080KB-A Previous code : 80P6Q-A (80-pin 0.5mm-pitch LQFP)	R0E5212DAEPB00		R0E5212DACFK00
R8C/2K 🔸	PLQP0032GB-A	R0E5212L4EPB00		R0E5212L4CFG00
R8C/2L 🖈	(32-pin 0.8mm-pitch LQFP)	**		**

\*1. Converter board, socket for user system connection and user's manual are included.  $\star\star$ Under development

R8C	ŝ	
linv		(

#### Operating Environment for R8C/Tiny Series Software Tools

Product type	Product name	Host machine (OS) *7
RTOS	M3T-MR30/4 *8	IBM PC/ATcompatibles (Windows® XP, 2000)
C compiler package	M3T-NC30WA *1	IBM PC/ATcompatibles (Windows <sup>®</sup> XP, 2000)
MISRA C rule checker	SQMIint *2	IBM PC/ATcompatibles (Windows® XP, 2000)
IDE	High-performance Embedded Workshop *3	IBM PC/ATcompatibles (Windows® XP, 2000)
Simulator debugger	Simulator Debugger for M16C and R8C/Tiny Series *4	IBM PC/ATcompatibles (Windows® XP, 2000)
Emulator debugger	PC7501 Emulator Debugger for M16C and R8C/Tiny Series *5 Compact Emulator Debugger for M16C and R8C/Tiny Series *5 E8a Emulator Software *5	IBM PC/ATcompatibles (Windows® XP, 2000)
Flash and PROM Programming	Flash Development Toolkit *6	IBM PC/ATcompatibles (Windows® XP, 2000)

\*1. The M3T-NC30WA includes an integrated development environment (High-Performance Embedded Workshop), C compiler, assembler and simulator debugger.
\*2. SQMlint MISRA C rule checker (Part No.: R0C0000SCW01R) is sold as the optional product of Renesas C compiler.
\*3. High-performance Embedded Workshop is included with C compiler package and Emulator debugger.
\*4. Simulator debugger is bundled with C compiler package.
\*5. Emulator debugger is bundled with emulators.
\*6. Flash Development Toolkit (Part No.: R0C0000FDW04R) is available in a product version (with technical support) and an evaluation version (without technical support). The E8a emulator (Part No.: R0C00006FDW04R) is necessary for programming. Visit the Renesas Technology Web site (http://www.renesas.com/fdt)to confirm support details for specific MCU product numbers.
\*7. Please refer to the following URL for Windows® Vista. http://www.renesas.com/tool\_env
\*8. M3T-MR30/4 is a general term referring to the real-time OS development kit (M3T-MR30K/4) and the mass production contract (M3T-MR30S/4).

# **Partners Tools**

Powerful alliances between Renesas and its partner companies support the product development work of our customers.

# **Coding Tools**



#### Middleware & Drivers



Visit our Web site for the latest information. http://www.renesas.com/partners





# **Partners Tools**

Powerful alliances between Renesas and its partner companies support the product development work of our customers.

# Flash & PROM Programming



NEC IN MISC IN REC IN THE CONTRACT OF THE CONTRACT.

MEMO	)
------	---



### M16C Middleware



### TCP/IP Protocol Stack

Two versions of the standard Internet protocol stack, slim and ultracompact, are available for the M16C family. Both designed to use a minimum of ROM and RAM. Flexible support for a variety of applications.

#### Features

- Slim version (target MCUs: M16C/62 Group\*1)
- Essential functions and a compact design (uses approx. 33 Kbytes of ROM).
- Enables protocol processing using the MCU's on-chip memory.
   Ultra-compact version (target MCUs: M16C/Tiny and R8C/Tiny Series) The ultra-compact version required no OS (uses approx. 8 Kbytes of ROM) and can be stored in the on-chip memory of the Tiny Series. Note: See the lineup of Software Libraries to Support Tiny MCUs on the next page for details.
- \*1. Compatible with M16C/62A, M16C/62M, M16C/62N, and M16C/62P

Applications

Internet cameras, remote monitoring/control systems, Internetcapable home appliances, etc.

Implementation model

User application													
HTTP server	FTP server	DHCP client	SMTP client										
TCP/IP													
PPP		LAN driver											
OS (not needed for ultra-compact version)													
	Hard	ware											

## FAT File System

The FAT file system library provides data compatibility with PCs for various types of memory cards and enables storage of large-volume resources on hard disks to support the increasing popularity of broadband connections.

#### Features

- Support for FAT12, FAT16, VFAT, and FAT32
- Support for multiple drives
- Support for long filenames and Japanese filenames
- Light version available with support for short filenames only (for M16C)
- Minimal memory usage, fast operation
- · Includes sample source code for compact flash card driver
- Applications

Digital cameras, digital camcorders, hard disk drive video recorders, hard disk drive audio recorders, other PC-compatible data storage devices

#### Total support from Renesas

Renesas provides developers with total support in the form of drivers for MCU and memory as well as middleware to enable efficient implementation of functions.



# **Software Libraries to Support Tiny MCUs**

http://www.renesas.com/tiny\_swlib

Renesas supplies software libraries for evaluation purposes to customers using Tiny Series MCUs. Designed to be compact enough for embedding on a single chip, these programs are compatible with all Tiny MCUs. The software libraries for Tiny MCUs enable developers to create applied solutions for embedded devices essential in today's ubiquitously networked society, for example devices supporting remote operation via a network.

The programs composing the software libraries implement simple functions and are easy to use, making them ideal for use in training and evaluation. They can be embedded in systems that are mass produced,\*1 thereby helping bring down the final market cost of the product. Feel free to try them out and see what they can do for you.



\*1. Since they are intended for evaluation, these software libraries come with no warranty or support.

\*2. MultiMediaCard and SD Memory Card drivers are sold separately. Development of systems using MultiMediaCard (MMC) or SD Memory Card technology requires purchase of a license. For information on licensing, contact the MultiMediaCard Association or SD Card Association.

### Ultra-Compact TCP/IP Protocol Stack

This communication protocol software library achieves very compact size by keeping the number of functions to a bare minimum.

- Small memory requirements: Approx. 8 Kbytes of ROM and 0.5 Kbytes of RAM (in case of R8C/Tiny) (Enables TCP/IP protocol handling using the on-chip memory of a Tiny MCU.)
- No OS necessary.
- Conforms to ITRON TCP/IP API standard. • Includes sample driver for LAN controller (RTL8019AS).
- Includes sample driver for PPP.
- Applications
  - · Remote device control/monitoring using mobile phone packet communication terminal (vehicle position data management, remote equipment malfunction diagnostics. etc.)
  - · Security services (communication of information on visitors/intruders to mobile phones, etc.)
  - · Centralized equipment management in office buildings and factories (management of climate control systems, lighting, sensors. etc.)
- Advanced version (under development)

An ultra-compact TCP/IP protocol stack with support for multiple communication terminals and higher data transfer speeds is currently under development.

### Sound Playback System

This software enables sound output on any system incorporating a Tiny MCU. It can be used to add true sound output functionality to devices that previously only provided visual indications or beeps.

- Sound compression and expansion using exclusive ADPCM format.
   Small memory requirements: Approx. 0.6 Kbytes of ROM and 30 bytes of RAM (in case of R8C/Tiny)
- Includes sound compression/expansion utility (PC application) for compressing recorded sound data (in WAV format) on a PC. (The compressed data can then be used by the MCU.)
- Includes sample driver for PWM output.



### Original File System

The original file system supports storage of measurement data or history data and the reprogramming of internal memory with data stored on memory cards.

- Small memory requirements: Approx. 9.8 Kbytes of ROM and 256 bytes of RAM (in case of R8C/Tiny)
- No OS necessary. File system uses original format.
- FAT file system conversion function provides compatibility with PC data. Applications
  - Data storage and data logging on devices of various kinds
  - Storage of personal user data on healthcare products, etc.
  - · Updating of programs and data on memory cards or devices that utilize data

[Application example combining network middleware and file system] Centralized equipment management in an office building or factory using a Web brows



A version of the original file system with extended functionality, such as support for directory and user-defined filenames, is currently under development.

### Data Flash Driver Software

This block device driver enables the storing of data in data flash on R8C/Tiny and M16C/Tiny MCUs. It simplifies the task of building a data management system using data flash.

- Small memory requirements: Approx. 3 Kbytes of ROM and 100 bytes of RAM (including stack)
- · Capable of handling different data sizes.
- Max. data update count: 1,000,000 times or more (depending on number and size of data units and the update count)
- Old data can be restored if system shutdown occurs during data update.
- Drive function interrupt/restart supported. This prevents the driver from monopolizing the CPU for an excessive length of time.

# CAN Communication Demo Set for Industrial Applications (M16C/29)



# Application of CAN MCUs in an Elevator (M16C)

#### Features

- Recreates an elevator system as an example of the use of CAN communication functionality.
- CAN communication is safe even from noise output from the motor.
- The M16C/29 can be used to implement both motor drive and CAN communication functions.





#### Audio Decompression/Audio Output Demo Set (M16C/26A)

#### Features

- Decompresses compressed audio data stored in the MCU's on-chip flash memory and produces PWM output for audio playback. The data compression format is ADPCM.
- The demo kit consists of an audio board (board with an amplifier, LPF, and compact speaker mounted on it) connected to the Renesas Starterkit for M16C/26A.



### LIN Communication Demo Set (M32C/87)

#### Features

- LIN communication is implemented using the M32C/87 as the master device.
- The R8C/23 is used as the slave device.



All trademarks and registered trademarks are the property of their respective owners. IEBus is a registered trademark of NEC Electronics Corporation. Windows is a trademark or registered trademark of Microsoft Corporation of the U.S.A. in the United States and other countries. MultiMediaCard is a trademark of Infineon Technologies AG of Germany and licensed by the MultiMediaCard Association (MMCA). Renesas Technology Corp. is an MMCA board member. TRON is an abbreviation of "The Real-time Operating System Nucleus." ITRON is an abbreviation of "Industrial TRON." µITRON is an abbreviation of "Micro Industrial TRON." The TRON Association holds the copyright on the µITRON specification. TRON ITRON and µITRON are the names of computer specifications and do not refer to any

TRON, ITRON, and  $\mu\text{ITRON}$  are the names of computer specifications and do not refer to any specific product or products.

# **Functions/Applications**

### Applications

		A)//Lloma Lloa															•	Ideal 😑 : Suitable
		A	V/Hoi	me Us	se		PC Re	elated		Automo	tive (App	licable P	roducts Av	vailable)			rity	
Series	Group	Audio	Video	Appliances	Amusement	PC	Storage	Imaging	Display	Engine	Driving Safety	Body/Chassis	Navigation/ Information	Car Audio	Mobile	Networking	Industrial/Secu	Notes
R32C/100	R32C/111**	•	•	•	٠	•		•	•							•	•	
M32C/80	M32C/88	•	٠	•	٠						٠	•		•		•	•	
	M32C/87	•		•							•			•				Large-capacity flash applications
	M32C/85	•	٠	•	٠			•			٠	•		•		•	•	
	M32C/84	•		•							•	•		•			•	
	M32C/83										•			•				
	M32C/82																	
	M32C/81			•								•		•		•		
	M32C/80	•			•										•		•	
M16C/80	M16C/80				•						•	•			•		•	
M16C/60	M16C/6S															•		
	M16C/6N										•	•		•		•	•	
	M16C/6V		•															
	M16C/6H		•															
	M16C/64**	•															•	
	M16C/65**	•															•	
	M16C/62P	•									•	•		•			•	
	M16C/62A	•	•	•	•	•	•	•	•				•	•		•	•	
	M16C/62N	•												•			•	
M16C/30	M16C/30P	•	•	•	•									•		•	•	
	M16C/39P	•																
M16C/20	M16C/2N										•	•				•		
	M16C/24					•	•											
M16C/Tiny	M16C/29	•		•							•	•	•	•		•	•	
	M16C/28			•							•	•					•	
	M16C/26A			•							•	•		•				
M16C/10	M16C/1N				•						•							
															**:	Jnder Development		

Ар	plication	S																
																	• :	Ideal 😑 : Suitable
		A	V/Hor	ne Us	se		PC Re	elated		Automo	tive (Appl	icable Pr	roducts Av	/ailable)			ity	
Series	Group	Audio	Video	Appliances	Amusement	PC	Storage	Imaging	Display	Engine	Driving Safety	Body/Chassis	Navigation/ Information	Car Audio	Mobile	Networking	Industrial/Secur	Notes
R8C/Tiny	R8C/10																	
	R8C/11																	
	R8C/12																	
	R8C/13																	
	R8C/14																	
	R8C/15																	
	R8C/16																	
	R8C/17																	
	R8C/18																	
	R8C/19																	
	R8C/1A																	
	R8C/1B																•	
	R8C/20																	
	R8C/21																	
	R8C/22																	
	R8C/23																	
	R8C/24																	
	R8C/25														•		•	
	R8C/26																	
	R8C/27														•			
	R8C/28																	
	R8C/29																	
	R8C/2A																	
	R8C/2B																	
	R8C/2C																	
	R8C/2D														•			
	R8C/2E**																	
	R8C/2F**														•			
	R8C/2G**	•		•													•	
	R8C/2H**														•			
	B8C/2J**																	
	R8C/2K**														•			
	R8C/2L**																	
		-		-		-											**'	Inder Development

# Package Photos



(Previous code: 52P6A-A) (0.5mm pitch)



PLQP0064KB-A

PRDP0020BA-A (Previous code: 20P4B) (20mil)



PTLG0064JA-A (Previous code: 64F0G) (6mm×6mm) (Previous code: 64P6Q-A) (0.5mm pitch)





PLQP0064GA-A (Previous code: 64P6U-A) (0.8mm pitch)



PLQ0032GB-A (Previous code: 32P6U-A) (0.8mm pitch) PLQP0048KB-A (Previous code: 48P6Q-A) (0.5mm pitch)



PLQP0080KB-A (Previous code: 80P6Q-A) (0.5mm pitch)





PTLG0085JB-A (Previous code: 85FOG) (7mm×7mm)



PLQP0128KB-A (Previous code: 128P6Q-A) (0.5mm pitch) PLQP0144KA-A (Previous code: 144P6Q-A) (0.5mm pitch)

69





PTQP100LB-A (Previous code: 100PFB) (0.4mm pitch)

70

# **Functions/Applications**

# Standard Functions

		;	2C/100				00,00	2C/80				6C/80					6C/60					00,00	00/30	6C/20		6C/Tiny		6C/10	
				8				1					M1					Ē						<u> </u>	M		B	6B	M1
		Group	,	R32C/111**	M32C/88	M32C/87	M32C/85	M32C/84	M32C/83	M32C/82	M32C/81	M32C/80	M16C/80	M16C/6S	M16C/6N	M16C/6V	M16C/6H	M16C/64**	M16C/65**	M16C/62P	M16C/62A	M16C/62N	M16C/30P	M16C/39P	M16C/24	M16C/29	M16C/28, 28	M16C/26A, 2	M16C/1N
	CPU	Multipli	er																										
		Multiply-a	occumulate instruction																										
		Barrol	chiftor										-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	_
~		EDII	Shinton		-	-				-	-																		
ũ	DIAA	TFU																											_
ij	DIVIA	DIMAC		•	-	•	•	-	-	•	-	-	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	
Ĕ		DTC/D	MAII																										
f	On-chip	RAM																											
ne	memory	Flash r	nemory																										
γ		Mask F	ROM																										
or		One-tir	ne PROM		-		-	-		-					-					-		-	-	-				-	_
E			1													-								_	-				_
Ĕ		DOM														_	_												_
Ľ,			655									-	-							-				-					
Ľ,		Data fla	asn	•	•									•	•	•		•	•	•	_		•	•		•	•	•	
0		Progra	m security																										
	External bus	Address	data separate buses																										
	extensions	Address	/data multiplex bus																										
		DRAM	controller																										
	Clocks	PLI																											
SUC	CIUCKS	Cubala	ok/PTC											-															
ctic		Subcio											-		-	-	-	-	-	-	-	-	-	-	-	-		-	
Į		On-chi	ooscillator											•	•			•	•	-						•	•		
ly 1		Oscillat	ion stop detection	•								•			•			•	•	•						•	•	•	
dd		Freque	ncy divider circuit																										
r s		Low-power	-consumption mechanism																										
We	Voltage	Low-vol	tage detection/LVD																										
bc	detection	Power-	on reset																										
ock	Operating	5V																											
ō	voltage	21/															-				-								-
	Voltage	0.64												-	-				-										
	A/D converters	8-DIt												•	-	•	•										-		-
		10-bit		•	•	•	•	•	•	•	•	•	•		•	_	_	•	•	•	•	•	•	•	•	•	•	•	-
		S & H																											
	D/A converter	8-bit																											
	Timers	Input c	apture																										
		Output	compare																										
		bit	16-bit																										
		bit	PWM output																						-				
			Real-time ports									_	_	-	-	-	-	-	-	-	-	-	-	-		-	-	-	_
		Functions	Fuent counter																										
		Functions	Event counter	-	-	-	-	-	-		-	-	•	•	-	•	-	-	-	-	-	-	•	-		-	-	-	
			2-phase encoder input												•														
			3-phase inverter output																										
	Real-time cl	lock																											
	Watchdog																												
SUC	Serial I/F	Clock no	n-synchronous serial																										
Stic		Clock s	vnchronous serial																										
Inc	Advanced	l <sup>2</sup> C buc	,																							•	•		
l fu	communication	IERuo	,											-		-	-												-
ra	communication	Cmart	aard/CIM															-	-						-	-	-	-	
he		Smart	card/SIIVI																			•	•	•					
rip		Synchronol	is serial communication unit	•	•	•	•	•	•	•	•	•	•		•	•	•	•	•	•	•					-			
Ре		CAN													•											•			
		LIN																											
		HDLC																											
		USB F	unction																										
		IrDA																											
	Display	OSD																											
		Data d	icer													-													
		Eluoroooo	nt dienlaw tubo controllor														-												
	Operation	CDC	n display lube controller																					-					
	operation	CHU													-		-	-	-	-	•	-	-	-	-	-	-	-	
	Tunctions	X/Y CO	iversion	•		•						•	-																
	I/O ports	Large-c	urrent drive ports																										
		N-chanr	el open-drain ports																										
		On-chip	pull-up resistors																										
	On-chip debugging	On-chi	o debugging														[							]					
	functions	On-boa	rd flash rewriting																										
																									++	· Und	or Do	velor	ment

<sup>\*</sup> Multimaster I<sup>2</sup>C

# Standard Functions

		Series	i																R8	C/Ti	iny														
		Group		R8C/10	R8C/11	R8C/12	R8C/13	R8C/14	R8C/15	R8C/16	R8C/17	R8C/18	R8C/19	R8C/1A	R8C/1B	R8C/20	R8C/21	R8C/22	R8C/23	R8C/24	R8C/25	R8C/26	R8C/27	H8C/28	BRC/20	R8C/2B	R8C/2C	R8C/2D	R8C/2E**	R8C/2F**	R8C/2G**	R8C/2H**	R8C/2J**	R8C/2K**	R8C/2L**
	CPU	Multipli	er																																
		Multiply-a	ccumulate instruction																																
		Barrel s	shifter																			_											_		
ns	DMA	DMAC																															_		
itio	0 1:	DIC/D	MAII																																
un o	On-chip	RAM																																	
s fu	memory	Flash n	nemory	•	•	•	•	•	•	•		•	•	•	•	•	•	•	•	-	•	•						-	•	•	•	•	•	•	-
ĥ		Mask F																										-							
Z		One-tin																				_	_		_								_		
Ĕ			//																									-							
шe		Data fl	55 vch																																
		Prograu	n security																																
E	External bus	Address/	data senarate huses	-		-		-	-		-	-				_	-	-	-	_	-	-										-	-	-	
	extensions	Address	/data multiplex bus																																
	extensions	DRAM	controller																																
	Clocks	PLI																																	
s	CIOCKS	Subclo	ck/RTC																			•	•		*										
tior		On-chi	oscillator																																
nnc		Oscillat	on stop detection																																
<u>S</u>		Freque	ncy divider circuit																																
dng		Low-power	consumption mechanism																																
er	Voltage	Low-volt	age detection/LVD																																
NOC	detection	Power	on reset																																
S	Operating	5V																																	
ဗီ	voltage	ЗV																																	
	A/D converters	8-bit																																	
		10-bit		lacksquare																															
		S & H																																	
	Comparator	•																																	
	D/A converter	8-bit																										•	•	•			_		
	Timers	Input ca	apture																			•											•		
		Output	compare			•																•			4								•	•	
		bit																																	
			Pww output	•	•	•	-	•	•	•	•	•	•	•	-	•	•	•	•	-	-	•						-	-	•	•	•	-	•	-
		Functions	Event counter																																
		Functions	2 phase aneodor input	•	-	-	-	-	-	•	-	-	-	•	-	-	-	•	•	-	-	•						-	-	-	-	-	-	-	-
			3-phase inverter output																																
	Real-time c	lock																																	
	Watchdog																																		
Suc	Serial I/F	Clock no	n-svnchronous serial																																
cti		Clock s	nchronous serial																																
fun	Advanced	I <sup>2</sup> C bus																																_	
<u>ש</u>	communication	IEBus																																	
hei		Smart of	card/SIM																																
rip		Synchronou	s serial communication unit																																
Ъ		CAN																																	
		LIN																																	
		HDLC																																	
		USB Fi	unction																																
		IrDA																																	
	Display	OSD																																	
		Data sl	icer																																
	-	Fluorescer	nt display tube controller																																
	Operation	CRC																																	
	tunctions	X/Y cor	nversion			_																					-							_	
	I/O ports	Large-c	urrent drive ports																			*	*		*										
		IN-Chann	ei open-arain ports	-																								-						-	
	On-chip debugging	On-chip	pull-up resistors			-											-															-			
	functions	On boo	rd flach rowriting			-			-			-		-			-	-			-	-										-	-	-	-
	Turiouorio	UII-DOa	ru nasi rewnung			-		-	-			-		-		-	-	-		-	-	-	-					1 🖤				-	-	-	

★★: Under Development \* Note: This function not implemented on J.K version.

# **Flash Memory Versions**

# Memory Options (ROM/RAM)

-															
								RAM size	e (bytes)					_	
		256	384	512	768	1K	1.5K	2K	2.5K	ЗK	4K	5K	6K	8K	10K
	01/	R8C/2J**													
	2K	R8C/2H**													
ľ			R8C/18												
	ΔК		B8C/1A												
	-11														
	4K+2K		H8C/19												
			R8C/1B												
			R8C/2H**	R8C/10		R8C/2K**									
				R8C/11											
				R8C/14											
				R8C/16											
	8K			R8C/18											
				B8C/1A											
				Dec/26											
				H8C/28											
				R8C/2E**											
				R8C/15		R8C/2L**									
				R8C/17											
				R8C/19											
	8K+2K			R8C/1B											
				R8C/27											
				B8C/29											
-				HOC/2F^^											
	8K+4K			R8C/12											
	-			<b>R8C/13</b>											
					R8C/10										
					R8C/11										
					R8C/14										
	12K				R8C/16										
_					R8C/18										
es															
Š															
e															
	12K+2K				R8C/17										
5					R8C/19										
วิ					R8C/1B										
r					R8C/12										
	12K+4K				R8C/13										
ľ				R8C/2G**		R8C/10	R8C/2K**								
						B8C/11									
						H8C/16									
	16K					R8C/18									
	-					R8C/1A									
						R8C/24									
						R8C/26									
						R8C/28									
						R8C/2E**									
						R8C/15	R8C/2L**								
						B8C/17									
						Dec/10									
						R00/19									
	16K+2K					H8C/1B									
						R8C/25									
						R8C/27									
						R8C/29									
						R8C/2F**									
Ī						R8C/12									
	16K+4K					R8C/13									
	24K					B8C/2G**	B8C/26	B8C/24							
-	2414 24					100/20	B8C/07	R8C/25							
	24N+2N							nou/25							
-	24K+4K					M16C/26A									
						(R8C/2G**)	R8C/26	R8C/20							
	32K							R8C/22							
								R8C/24							
							R8C/27	R8C/21							
	32K+2K							R8C/23							
								B8C/25							
		1	1	1	1	1	1		1	1	1	1	1	1	1

# Memory Options (ROM/RAM)

		RAM size (bytes)																		
		2K	2.5K	ЗK	4K	5K	6K	7K	7.5K	8K	10K	12K	16K	18K	20K	24K	31K	40K	48K	63K
			R8C/20																	
			R8C/22																	
	18K		B8C/24																	
	4010		D00/04																	
			ROC/ZA																	
			R8C/2C																	
			R8C/21																	
			R8C/23																	
	48K+2K		R8C/25																	
			R8C/2B																	
			R8C/2D																	
	48K+4K	M16C/26A			M16C/28	,														
				B8C/20						M16C/62N										
				Dec/22																
				nou/22	1															
	64K			R8C/24	2															
				R8C/2A	1															
				R8C/2C	, 															
				R8C/21																
				R8C/23	,															
	64K+2K			R8C/25	•															
				R8C/2B	,															
				R8C/2D																
		M16C/26A		M16C/1N	M16C/28															
	64K+4K	MIOUZUA			MIRC/POP															
					m100/02P	Dec./oc		Decint												
						R8C/20		H8C/2A												
(s	96K					R8C/22		R8C/2C												
yte						M16C/30P														
9	06K+2K					R8C/21		R8C/2B												
ize	301(+21(					R8C/23		R8C/2D												
م ا	0.014 414					M16C/30P				M16C/28										
õ	96K+4K									M16C/29										
Œ						M16C/30P	R8C/20		R8C/2A		M16C/62A									
	128K						B8C/22		B8C/2C		M16C/62N									
	12010						TIOO/LL		100/20		M16C/90									
							D00/01		Dag (op		W10C/80									
	128K+2K						H8C/21		HOC/2B											
							R8C/23		R8C/2D											
	128K+4K					M16C/6N					M16C/62P	M16C/28								
						M16C/30P						M16C/29	•							
	160K					M16C/30P						M16C/30P	,							
	192K						M16C/30P					M16C/30P								
	192K+4K						M16C/30P													
															M16C/62A					
	256K											M16C/30P			M16C/62N					
															M16C/80					
	256K+4K										MIGOIGN				MISCISOR					
											WIDC/DN		MICONT		WI 100/02P					
	256K+24K												M16C/64**	11000	M16C/65**	1102012				
	320K+4K													M32C/88		M32C/84				
																M32C/85				
														M32C/88		M32C/84	M16C/62P			
	384K+4K															M32C/85	M16C/6N			
																M32C/87				
	512K																M32C/83			
														M32C/88		M32C/84	M16C/62P			
	512K+4K															M32C/85	M16C/6N			
																M32C/87				
	512K±8K																	B32C/111**		B32C/111**
	E10K 04K																HICOMAN	1020/111-2		TUEUTIT
	J12K+24K																m10G/04**		11000100	
	/08K+4K																		M32C/87	
	IMB+4K																		M32C/87	

# **Flash Memory Versions**

# Memory Options (Pin count)

-										
						Pin count				
		20	32	42	48	52	64	80	85	100
	2K	B8C/2J**								
		<b>R8C/18</b>								
	4K	R8C/1A								
		<b>R8C/2H**</b>								
		R8C/2J**								
		Dec/10								
	4K+2K	NOC/19								
		R8C/1B								
		B8C/14	B8C/10							
	8К	100/14								
		<b>R8C/16</b>	<b>R8C/11</b>							
		B8C/18	B8C/26							
			<b>R8C/2E**</b>							
		<b>R8C/28</b>	R8C/2K**							
		R8C/2H**								
		R8C/15	R8C/27							
		D00/17	DOC/OF++							
		HOC/17	HOU/2F^^							
	8K+2K	R8C/19	R8C/2L**							
		B8C/1B								
		R8C/29								
Ī			<b>B8C/12</b>							
	8K+4K									
			<b>R8C/13</b>							
		R8C/14	R8C/10							
	12K	DOCHE	D00/11							
		H8C/16	HOC/II							
(c)		R8C/18								
j										
ð		NOC/TA								
Ð	12K+2K 12K+4K	<b>R8C/15</b>								
SI		<b>B8C/17</b>								
ROM										
		<b>R8C/19</b>								
		R8C/1B								
ł			Decide							
			H8C/12							
			R8C/13							
ł		Dec/14	Dec/10			Dec/24				
	16K	noc/14								
		<b>R8C/16</b>	<b>R8C/11</b>							
		B8C/18	B8C/26							
		R8C/1A	R8C/2E**							
		R8C/28	R8C/2G**>							
			DOC/OK++							
			HOC/2K**							
		R8C/15	R8C/27			R8C/25				
		B8C/17	B8C/2E**							
			1100/21							
	16K+2K	R8C/19	R8C/2L**							
		R8C/1B								
		R8C/29								
	1016 115		<b>R8C/12</b>							
	16K+4K		Dec/12							
			noc/13							
	0.414		R8C/26			R8C/24				
	∠4K		B8C/2G**							
			100/20							
	24K+2K		R8C/27			R8C/25				
	24K+4K			M16C/26A	M16C/26A					
			<b>D00/00</b>		D00/00	D00/04				
	32K		H8C/26		H8C/20	H8C/24				
			R8C/2G**		R8C/22					
	32K+2K		Dec/07		Dec/ot	Declor				
			HOC/2/		HOC/21	Hoc/25				
					R8C/23					
## Memory Options (Pin count)

						Pin count				
		42	48	52	64	80	85	100	128	144
	101/		R8C/20	R8C/24	R8C/2A	R8C/2C				
	48K		R8C/22							
			<b>B8C/21</b>	<b>B8C/25</b>	B8C/2B	R8C/2D				
	48K+2K		B8C/23							
	19K JK	M16C/26A	M16C/26A		M16C/28	M16C/28	M16C/28			
	401.441	WITOC/20A	Dec/20A	DOC/04		N/10C/20	W10C/20			
	64K		R8C/20	H8C/24	H8C/2A					
			R8C/22							
	64K+2K		R8C/21	<b>R8C/25</b>	R8C/2B	R8C/2D				
			<b>R8C/23</b>							
	64K JK	M16C/26A	M16C/26A		M16C/28	M16C/28	M16C/28			
	041(+41(		M16C/1N			M16C/62P				
			R8C/20		R8C/2A	R8C/2C		M16C/30P		
	96K		R8C/22							
			B8C/21		B8C/2B	B8C/2D				
	96K+2K		R8C/23		HOULD					
			100/23		M16C/09	M16C/09	M16C/09	M16C/20D		
	96K+4K				W10C/20	M10C/20	WI10C/20	WITC/JUP		
					M16C/29	M16C/29				
			R8C/20		R8C/2A			M16C/30P		M16C/80
	128K		<b>R8C/22</b>					M16C/62A		
	12010							M16C/62N		
								M16C/80		
			R8C/21		R8C/2B	R8C/2D				
	128K+2K		R8C/23							
					M16C/28	M16C/28		M16C/30P		
	1094 14				M16C/20	M16C/20		M16C/62P		
	12011+11				WITOC/25	MICO/COP		MICO/OZP		
(;						IVI 10C/02P				
rtes	160K							M16C/30P		
(d)	192K							M16C/30P		
Ze	192K+4K							M16C/30P		
1 si								M16C/62A		M16C/80
<b>O</b>	OFCK							M16C/30P		
œ	2500							M16C/62N		
								M16C/80		
								M16C/62P	M16C/62P	
	256K+4K							M16C/6N		
								M16C/64**	M16C/65**	
	256K+24K							M16C/65**	W100/03	
								M000/04		M000/04
								M32C/84		M32C/84
	320K+4K							M32C/85		M32C/85
								M32C/88		M32C/88
								M16C/62P	M16C/62P	M32C/84
								M16C/6N	M16C/6N	M32C/85
	20414 414							M32C/84		M32C/88
	384N+4N							M32C/85		M32C/87
								M32C/87		
								M32C/88		
	512K							M32C/82		M32C/82
								MIEC/EOD	MIECIEOD	M22C/03
								MICO/OZP	MICO/OZF	M00C/04
								MITOC/ON	WITOC/ON	WI32C/85
	512K+4K							M32C/84		M32C/88
								M32C/85		M32C/87
								M32C/87		
								M32C/88		
	512K+8K							R32C/111**		
	512K+24K							M16C/64**		
	768K+4K							M32C/87		M32C/87
	1MB+4K							M32C/87		M32C/87

★★: Under Development

## **Mask Versions**

## Memory Options (ROM/RAM)

							RAM	size (byte	es)						
		1K	2K	ЗK	4K	5K	6K	8K	10K	12K	16K	18K	20K	24K	31K
	ROM Less			M16C/62P			M16C/30P	M32C/80	M16C/80 M16C/62P M32C/84	M32C/8A			M16C/62P	M16C/80 M32C/8A**	M16C/62P
	24K	M16C/26A													
-	32K	M16C/1N		M16C/62A											
	48K		M16C/26A		M16C/62P										
	64K		M16C/26A	<u>M16C/1N</u>	M16C/28 M16C/29 M16C/62A M16C/62P				M16C/62A						
-	96K					M16C/30P M16C/62A M16C/62P		M16C/28 M16C/29	M16C/62A						
ze (bytes)	128K					M16C/30P M16C/39P M16C/62A M16C/6N			M16C/62A M16C/62N M16C/62P M16C/80 M32C/81 M32C/84	M16C/28 M16C/29 M16C/62N M32C/81					
M si:	160K						M16C/30P								
ВÖ	192K						M16C/30P M16C/39P			M16C/62P	M16C/6N				
-	256K								M16C/6N	M16C/62P			M16C/62A M16C/62N M16C/62P M16C/6N M16C/80 M32C/84 M32C/85		
	320K										M16C/62P			M16C/62P M32C/82 M32C/84 M32C/85	M16C/62P
	384K										M16C/62P			M16C/62P M32C/82 M32C/84 M32C/85 M32C/85	M16C/62P M32C/82
	512K														M32C/87

★★: Under Development

N /	0			
wemory	<sup>o</sup> Options	(PIN	count)	

				Pin c	count			
		42	48	64	80	100	128	144
	ROM Less					M16C/62P M16C/80 M32C/8A M32C/80 M32C/84		M16C/80 M32C/8A M32C/84
	24K	M16C/26A	M16C/26A					
	32K		M16C/1N		M16C/62N	M16C/62A		
	48K	M16C/26A	M16C/26A		M16C/62P	M16C/62P		
	64K	M16C/26A	M16C/26A M16C/1N	M16C/28 M16C/29	M16C/28 M16C/29 M16C/62A M16C/62P	M16C/62A M16C/62P		
	96K			M16C/28 M16C/29	M16C/28 M16C/29 M16C/62A M16C/62P	M16C/30P M16C/62A M16C/62P		
ROM size (bytes)	128K			M16C/28 M16C/29	M16C/28 M16C/29 M16C/62A M16C/62P	M16C/30P M16C/39P M16C/62A M16C/62N M16C/62P M16C/60N M16C/80 M32C/81 M32C/84		M32C/81 M32C/84
	160K					M16C/30P		
	192K					M16C/30P M16C/39P M16C/62P M16C/6N	M16C/62P M16C/6N	
	256K				M16C/62A M16C/62N	M16C/62A M16C/62N M16C/62P M16C/6N M16C/80	M16C/62P M16C/6N	M16C/80
	320K					M16C/62P M32C/82 M32C/84 M32C/85	M16C/62P	M32C/82 M32C/84 M32C/85
	384K					M16C/62P M32C/82 M32C/87	M16C/62P	M32C/82 M32C/87
	512K					M32C/87		M32C/87

#### • Specifications (M32C/80 Series)

Group	·	M32C/8A		M32	C/80				M32	C/81		
	ROM (Bytes)			-					12	8K		
	RAM (Bytes)	12K		8	K			10K			12K	
Memory	ROM Type*1			L					N	Λ		
	Data Flash											
	Program Security						-					
	CPU Regin Instructions						109 109					
	Minimum Instruction Execution Time (no)						108					
CPU	Multiplior						16 v 16-222					
	Multiply-Accumulate Instruction						10 × 10 + 48 - 48	1				
	Barrel Shifter						Yes	,				
	DMAC (Channels)						4					
DMA	DTC/DMACII					DMACII (Starts	ov all peripheral	interrupt factors	)			
	Address Space (Bytes)						16M					
External Bus Expansion	External Bus Interface	Support for insertion of 1 to 6 wait states, Outputs 4 chip-select signals, Page mode support	Sup	port for insertion Outputs 4 chip	of 1 to 6 wait st -select signals	ates,	Su	pport for insertic	on of 1 to 3 wait s	tates, Outputs 4	chip-select sign	als
	Bus Structure	S	electable from S	eparate bus, Mu	Itiplex bus, Data	Bus Width can b	e selected (8/16	-bit), The numbe	er of output addr	ess buses can b	e selected (16/20	0)
	DRAM Controller			-					Ye	es		
	Clock Generation Circuit				4 circi	uits (Main clock,	PLL, Sub-clock	and On-chip osc	illator)			
	PLL						Yes					
Clock	Subclock						Yes					
CIOCK	On-Chip Oscillator						Voc					
	Frequency Divider					1/n (n=1 4	2.3.4.6.8.10	2, 14, 16)				
	Power Save						Wait/Ston	, 1-, 10)				
Power Supply	Power-On Beset/POB						-					
Voltage Detection	Low Voltage Detection/LVD		,	Yes (Low voltage	)					_		
	Besolution × Channels			10-bit × 10	/		10-bi	× 26	10-bit × 34	10-bi	t × 26	10-bit × 34
A/D Converter	Sample and Hold						Yes					
	Multi-Channel Sample and Hold						-					
D/A Converter	Resolution × Channels						8-bit × 2					
	8-bit						-					
	16-bit					11	(Timer A, Timer	B)				
	Input Capture			-			5 (Intelli	gent I/O)	12 (Intelligent I/O)	5 (Intelli	gent I/O)	12 (Intelligent I/O)
	Output Compare			-			8 (Intellig	gent I/O)	20 (Intelligent I/O)	8 (Intelli	gent I/O)	20 (Intelligent I/O)
Timer	PWM Output			5 (Timer A)			13 (Timer A	ntelligent I/O)	25 (Timer A,	13 (Timer A	ntelligent I/O)	25 (Timer A,
				e (					Intelligent I/O)			Intelligent I/O)
	Real-Time Port			-			3 (Intellig	gent I/O)	8 (Intelligent I/O)	3 (Intelli	gent I/O)	8 (Intelligent I/O)
	Event Counter					11	(Timer A, Timer	B)				
	2-Phase Encoder Input			3 (Timer A)	1 (abavad			Times D0 Dee	3 (Timer A) + 2	(Intelligent I/O)		
Watabdag Timor	3-Phase Inverter Control				r (snared w	iun Timer A4, Tim	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	, Timer 62, Dea	d ume umer)			
watchuog Timer	Clock Sync / Clock Async			5 (LIADT)			1		7 (LIAPT Int	folligent I/O)		
Serial Interface	Clock Sync. Only	-		2 (Intellie	nent I/O)				1 (Intellio	rent I/O)		
	Clock Async, Only			- (	5		_		. (	5		
I <sup>2</sup> C-bus							5 (UART)					
IEBus				5 (UART)					6 (UART, Int	telligent I/O)		
Smart Card/SIM				. ,			5 (UART)					
Synchronous Serial	Communication Unit/Special Serial I/O						5 (UART)					
CAN	Channels			-					1			
CAN	Message Box (Numbers)			-					1	6		
IrDA												
CRC Calculation	Circuit					1 (CRC-0	CITT (X <sup>16</sup> + X <sup>12</sup>	+ X <sup>5</sup> + 1))				
X/Y Converter							Yes					
	Input Only (Numbers)						1	-	10.	-		101
10 0.1	CMOS I/O (Numbers)			45			8	5	121	8	5	121
I/O Ports	High Current Drive Port (Numbers)								-			
	Rull-Lip Resistor			45				5	121		5	121
External Interrup	te Pine			45			11	5	121	0	5	121
Debugging	On-Chip Debug						_					
Function	On-Board Flash Program						-					
Other	ROM Correction Function			_					Ye	es		
Functions	Others			3V, 5V Interface					_	_		
Operating Freque	ency/Supply Voltage		32MHz/4.2	to 5.5V, 24MHz/	'3.0 to 5.5V			32	MHz/4.2 to 5.5V,	20MHz/3.0 to 5	.5V	
Operating Ambie	nt Temperature (°C)					- 2	20 to 85, - 40 to	85				
		4-8		4-2		¥.	A-8	4-8	₹-	A-8	4-8	₹-
Package*2		OKE		B			100E	- KE	4K/	IN I	OKE	44/
гаскауе		100		010			010	100	114,	010	100	14
		2PC		10		L .	3PC	JPC	2PC	3P(	2PC	3PC
		-	· · · · ·	_	-	_	-	-		-	-	
				190		- 19		0	0	C	0	۹.
				SL <sup>k</sup>		ar a	XFF	XGF	19X	XFF	XGF	NG.
		*	<u>p</u>	-d.	L.	- 4	X	X	X	X	XX	X
Part No.		SGF	SAF	SAF	SAG	SAG	Ś.	Ş	0 V	Ş	ې د کې	ŴĊ
		AOS	3000	3000	3000	3000	11 ON	31 ON	312M	11 LV	31 LN	NI N
		305	306	306	305	305	305	305	305	305	305	305
		Ś	Σ	Σ	ŝ	Σ	Ś	Ś	Ś	Ś	Ś	Ś

<sup>1</sup> Built-in boot loader function ROM-less version <sup>\*1</sup> F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Q : QZROM version <sup>\*2</sup> Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M32C/80 Series)

Group						M32C/82						M32C/83	
	BOM (Bytes)		320K				38	4K				512K	
	RAM (Bytes)		OLOIN	24	1K				-	31	К	UTER	-
Memory	ROM Type*1					М						F	
	Data Flash						-	_					
	Program Security					-					Yes (ID Code Check	Function , ROM Co	de Protect Function)
	CPU						M32C/8	80 Core					
	Basic Instructions						10	08					
CPU	Minimum Instruction Execution Time (ns)					33.3 (@30MHz	:)	0.100			3	31.3 (@32MHz	)
	Multiplier						16×1	b→32					
	Barrel Shifter						10×10 <sup>-1</sup>	PS					
	DMAC (Channels)							4	-				
DMA	DTC/DMACII					DMACII (	Starts by all pe	ripheral interru	pt factors)				
	Address Space (Bytes)						16	6M					
External Bus	External Bus Interface				Supp	ort for insertior	of 1 to 3 wait s	states, Outputs	4 chip-select s	ignals			
Expansion	Bus Structure		Selectable fror	n Separate bus,	, Multiplex bus,	Data Bus Widt	h can be select	ted (8/16-bit), 7	he number of c	utput address	buses can be s	elected (16/20	)
	DRAM Controller					A size like (Masia	Ye	es	ahin anaillatan				
	DI I					4 circuits (iviain	CIOCK, PLL, SU	ib-clock and Or	1-crip oscillator	)			
	Subclock						Y	es					
Clock	On-Chip Oscillator						Ye	es					
	Oscillation Stop Detection			-			Ye	es	-				-
	Frequency Divider					1/n	(n=1, 2, 3, 4, 6	6, 8, 10, 12, 14,	16)				
	Power Save						Wait	/Stop					
Power Supply	Power-On Reset/POR						-	_					
voltage Detection	Low Voltage Detection/LVD	10 1		10 54 04	10 1-		-	- 10 5		10 53 04	10 1:1 00	(0 -:	10 10 01 (0
A/D Convertor	Sample and Hold	10-01	1×20	10-bit × 34	10-01	1×20	10-bit × 34	10-0	1×20	TU-DIL × 34	TU-DIL X 26	(2 circuits)	TU-DIL X 34 (2 dircuits)
A/D Conventer	Multi-Channel Sample and Hold					_						Yes	
D/A Converter	Resolution × Channels						8-bi	t×2					
	8-bit						-	_					
	16-bit						11 (Timer	A, Timer B)					
	Input Capture	5 (Intelli	gent I/O)	12 (Intelligent I/O)	5 (Intelli	gent I/O)	12 (Intelligent I/O)	5 (Intelli	gent I/O)	12 (Intelligent I/O)	5 (Intellig	gent I/O)	12 (Intelligent I/O)
-	Output Compare	8 (Intelli	gent I/O)	20 (Intelligent I/O)	8 (Intelli	gent I/O)	20 (Intelligent I/O)	8 (Intelli	gent I/O)	20 (Intelligent I/O)	10 (Intelli	gent I/O)	28 (Intelligent I/O)
limer	PWM Output	13 (Timer A,	Intelligent I/O)	25 (Timer A, Intelligent I/O)	13 (Timer A,	Intelligent I/O)	25 (Timer A, Intelligent I/O)	13 (Timer A,	Intelligent I/O)	25 (Timer A, Intelligent I/O)	15 (Timer A, I	ntelligent I/O)	33 (Timer A, Intelligent I/O)
	Event Counter	3 (Intelli	gent I/O)	8 (Intelligent I/O)	3 (Intelli	gent I/O)	11 (Timer	A Timer B)	gent I/O)	8 (Intelligent I/O)	4 (Intelliç	jeni i/O)	16 (Intelligent I/O)
	2-Phase Encoder Input						3 (Timer A) + 2	(Intelligent I/O	)				
	3-Phase Inverter Control				1 (sha	red with Timer	A4, Timer A1, T	Fimer A2, Time	r B2, Dead time	timer)			
Watchdog Timer								1					
	Clock Sync./ Clock Async.						7 (UART, In	telligent I/O)					
Serial Interface	Clock Sync. Only					(Intelligent I/C	))				2	(Intelligent I/C	))
l <sup>2</sup> C-bus	Clock Async. Only						5 (1)						
IEBus							6 (UART, In	telligent I/O)					
Smart Card/SIM							5 (U	ART)					
Synchronous Serial	Communication Unit/Special Serial I/O						5 (U	ART)					
CAN	Channels					_						1	
LDA	Message Box (Numbers)					_						16	
CBC Calculation	Circuit					1.(		X <sup>16</sup> + X <sup>12</sup> + X <sup>5</sup> +	1))				
X/Y Converter	Olicat						0110-00111 () Ye	es					
	Input Only (Numbers)							1					
	CMOS I/O (Numbers)	8	5	121	8	5	121	8	15	121	8	5	121
I/O Ports	N-Channel Open Drain Port (Numbers)							2					
	High Current Drive Port				-		-	-				_	
Extornal Interru	Pull-Up Hesistor	8	5	121	8	5	121	1 8	15	121	8	5	121
Dobugging	On-Chip Debug						1	1				Yes	
Function	On-Board Flash Program					_						Yes	
Other	ROM Correction Function					Yes						-	
Functions	Others						-						
Operating Frequ	ency/Supply Voltage			-	30MHz/4.2	to 5.5V, 20MHz	z/3.0 to 5.5V				32MHz/4.2	to 5.5V, 20MH	z/3.0 to 5.5V
Operating Ambie	ent Temperature (°C)			r			- 20 to 85,	, – 40 to 85					
		B-A	B_A	A-A	B-A	B-A	A-A	B-A	B-A	A-A	B-A	B-A	A-A
Package*2			Xo	4 X		Xo	4 X	FOO	Xo	44 X	roo	NOK NOK	* *
		0	010	017	0	010	012	201	010	012	201	010	017
		DE LO	ğ	- D	l de l	<sup>o</sup>	- No	<u>B</u>	b B	LQ.	Rai	Ъ,	ğ
		ā	ā	<u> </u>	ā	ā	<u> </u>	ā	ā	٩	٩	ē.	<u> </u>
			0	0									
		XFP	XGF	XGF	ХFР	KGP	KGP	KFP	KGP	KGP			
5		X	XX	XX	X	X	X	X	X	XX	۹.	<u>e</u> _	<u>e</u>
Part No.		Ň	MW.	Ŵ	Η̈́	Η̈́	Η×	ΗM	Η×	ΗM	ΞſΞ	٥Ľ	Ъ
		823	823	825	823	823	825	826	826	828	833	833	835
		430	M30	M30	M30	M30	M30	M30	M30	M30	M30	M30	M30
		C											

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M32C/80 Series)

Group											M32C/84	4								
	ROM (Bytes)		-			128K			320K		320K	+ 4K	38	4K		320K + 4ł	<	Ę	512K + 4ł	<
	RAM (Bytes)			1(	)K							_		24K				-		
Memory	ROM Type***		L			_		Л			Yes	- (4K)	-	-			Yes	- (4K)		
	Dura Hadri										Yes (ID Code C	Check Function,			X (ID 0			00110		<b>F</b>
	Program Security										ROM Code Pr	otect Function)			res (ID C	ode Crieci	k Function,	ROM CO	Je Protect	Function)
	CPU Desis lastrustians									M	32C/80 Co	ore								
	Minimum Instruction Execution Time (ns)									31	3 (@32M	Hz)								
CPU	Multiplier									1	6×16→3	12								
	Multiply-Accumulate Instruction									16>	< 16 + 48-	→48								
	Barrel Shifter										Yes									
DMA	DMAC (Channels)								MACIL (S	Starts by a	4 all nerinhe	ral interru	int factors							
	Address Space (Bytes)								(		16M			/						
External Bus Expansion	External Bus Interface	Support for inserti wait states, Outputs signals, Page mo	ion of 1 to 6 s 4 chip-select ode support					Su	upport for	insertion	of 1 to 6 v	wait states	s, Outputs	4 chip-se	elect sign	als				
	Bus Structure		Sele	ectable fro	m Separa	ate bus, N	lultiplex b	us, Data	Bus Width	n can be s	elected (8	3/16-bit), T	The numb	er of outp	out addres	s buses	can be se	ected (16	6/20)	
	DRAM Controller							4 circu	ite (Main	clock PL	- Sub-clo	ck and O	n-chin os	cillator)						
	PLL							4 0100	its (ivialit	CIUCK, I LI	Yes	ick and O	1-crip 030	matory						
	Subclock										Yes									
Clock	On-Chip Oscillator										Yes									
	Oscillation Stop Detection								1/2	(n-1.0.0	Yes	0 10 14	16)							
	Power Save								1/11	(11=1, 2, 3	, 4, 6, 8, 1 Wait/Stop	)	, 10)							
Power Supply	Power-On Reset/POR										-									
Voltage Detection	Low Voltage Detection/LVD									Yes	(Low volta	age)								
	Resolution × Channels	10-bit ×	< 10	10-bit × 18	10-bi	$t \times 26$	10-bit × 34	10-bi	$t \times 26$	10-bit ×34	10-bit × 26	10-bit × 34	10-bit × 26	10-bit × 34	10-bi	$t \times 26$	10-bit × 34	10-bi	$t \times 26$	10-bit × 34
A/D Converter	Sample and Hold										Yes									
	Multi-Channel Sample and Hold								-	-	-									
D/A Converter	Resolution × Channels										8-bit × 2									
	16-bit		11 (Timer A, Timer B)																	
	Input Capture									8 (I	ntelligent	I/O)								
	Output Compare									8 (I	ntelligent	I/O)								
Timer	PWM Output Real Time Part									13 (Time	r A, Intelli	igent I/O)								
	Event Counter									11 (T	imer . Tim	ner B)								
	2-Phase Encoder Input								3	B (Timer A	) + 1 (Inte	elligent I/C	))							
	3-Phase Inverter Control						1 (s	hared wit	th Timer A	A4, Timer	A1, Timer	A2, Time	r B2, Dea	ıd time tin	ner)					
Watchdog Timer	Clask Suna / Clask Asuna									6 (1145	1 T. Intollia	ant I/O)								
Serial Interface	Clock Sync. / Clock Async.									0 (UAF	ntelliaent	I/O)								
	Clock Async. Only										_									
I <sup>2</sup> C-bus											5 (UART)									
Smart Card/SIM											5 (UART) 5 (UART)									
Synchronous Serial	Communication Unit/Special Serial I/O										5 (UART)									
CAN	Channels										1									
IrDA	Message Box (Numbers)										16									
CRC Calculation	Circuit								1 (0	CRC-CCI	TT (X <sup>16</sup> +	$X^{12} + X^5 +$	- 1))							
X/Y Converter											Yes									
	Input Only (Numbers)	45		81	0	5	121	•	15	121	1	121	85	121	•	5	121	0	5	121
I/O Ports	N-Channel Open Drain Port (Numbers)	+5		01		0	121			121	2	121	00	121		5	121	0	0	121
	High Current Drive Port										_									
<b>F</b> 1000	Pull-Up Resistor	45		81	8	5	121	8	15	121	85	121	85	121	8	5	121	8	5	121
External Interrup	On-Chin Debug					_					11	26	-				Ve	20		
Function	On-Board Flash Program					-					Ye	es	-	_			Ye	es s		
Other	ROM Correction Function		-				Ye	es			-	-	Ye	es			-	-		
Functions	Others									3V,	5V Interfa	ace								
Operating Freque	ency/Supply Voltage								32M	Hz/4.2 to	5.5V, 24M	Hz/3.0 to	5.5V							
oportaing																				
		4	4	4	4	4	4	4	Ą	4	4-	4	4-	4-	4	4	4	4	4	Ą
Packago*2		5 B	ХB	¥	0 BB	R R	4 ¥ Y	00B	KB KB	4KA	KB	4KA	OKB	4KA	OB OB	R R	4KA	OB	R R	4KA
1 denage		010	010	014	010	010	014	010	010	014	010	014	010	014	010	010	014	010	010	014
		цъ Ц	<sup>o</sup>	P P	ц Б	- PO-	- PO-	ц.	-Q-	-QP	-OP	-Q-	-ΩP	-o-	L L	- PO-	-Q-	Ъ.	- PO-	- PP
		ā	2	Ē	ā	Ē	Ē	đ	4	đ	4	Ē	đ	<u> </u>	ā	Ē	ē.	ā	Ē	đ
					*	*	*	0	٩	٩			**	**						
					XFF	XGI	XGI	(XFI	XG	(XG			NGI	XGI						
Part No.		<u>a</u>	d.	d.	X	X	XX	(X-V	<x-v< td=""><td><x-v< td=""><td>/GP</td><td>/GP</td><td>XX+</td><td>XX+</td><td>L L</td><td>Ъ</td><td>GР</td><td>£</td><td>Ъ</td><td>GР</td></x-v<></td></x-v<>	<x-v< td=""><td>/GP</td><td>/GP</td><td>XX+</td><td>XX+</td><td>L L</td><td>Ъ</td><td>GР</td><td>£</td><td>Ъ</td><td>GР</td></x-v<>	/GP	/GP	XX+	XX+	L L	Ъ	GР	£	Ъ	GР
		OSF	080	256	OMO	OMO	2MG	3MV	3MV	5MV	3FM	5FM	3MF	5MF	3FH	3FH	5FH	3FJ	3FJ	5FJ.
		084	084	084	084	084	084	084	084	084	084	084	084	084	084	084	084	084	084	084
		W3	Β	Ξ	Β	Β	Ξ	Β	Ξ	Εŭ	Β	Β	M3	Β	Ξ	Ξ	Ψ	Β	Β	Εŭ

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M32C/80 Series)

Group								M32	C/85						
	ROM (Bytes)		320K			320K + 4K		38	4K		384K + 4K			512K + 4K	
	RAM (Bytes)				1			2	4K				-		
Memory	ROM Type**		M			F			N			)/a a			
	Program Security				Ves /ID Code Cher	Function BOM Cor	la Protect Function)			Vas	(ID Code Ch	eck Function	(4K) BOM Code	Protect Fund	
	CPU				103 (10 0000 01100			M32C/	80 Core	103		CORT UNCTON	, 110101 00000	THOROUT UNIC	
	Basic Instructions							1	08						
	Minimum Instruction Execution Time (ns)							31.3 (@	32MHz)						
CPU	Multiplier							16 × 1	6→32						
	Multiply-Accumulate Instruction							16  imes 16	+ 48→48						
	Barrel Shifter							Y	es						
DMA	DMAC (Channels)			1					4						
	DTC/DMACII						DMACII (St	arts by all pe	ripheral inter	rupt factors)					
External Rua	External Bus Interface					Support fo	or insertion o	f 1 to 6 wait	olvi states Outou	te 4 chin-sol	oct signals				
Expansion	Bus Structure		Selectable	from Separa	ate bus. Multir	olex bus. Data	a Bus Width	can be selec	ted (8/16-bit)	. The numbe	r of output ac	ldress buses	can be selec	ted (16/20)	
	DRAM Controller														
	Clock Generation Circuit					4 circ	cuits (Main c	ock, PLL, Su	b-clock and	On-chip oscil	lator)				
	PLL							Y	es						
	Subclock							Y	es						
Clock	On-Chip Oscillator							Y	es						
	Oscillation Stop Detection						1/- /-	Y	es	4.40)					
	Prequency Divider						1/11 (1	1=1, 2, 3, 4, 0 Wait	, 8, 10, 12, 1 /Ston	4, 16)					
Power Supply	Power-On Beset/POB								-						
Voltage Detection	Low Voltage Detection/LVD							Yes (Lov	voltage)						
	Posolution × Channela	10	+ ~ 26	10-bit	10 -	+ ~ 26	10-bit	10-bit	10-bit	10 -	+ ~ 26	10-bit	10	26	10-bit
A/D Converter	ricolution × oridiffiels	10-01		× 34	10-01		× 34	× 26	× 34			× 34	10-01		× 34
	Sample and Hold							Y	es						
D/A O	Multi-Channel Sample and Hold														
D/A Converter	Resolution × Channels							8-D	t×2						
	16-bit					-		11 (Timer	A Timer B)						
	Input Capture							8 (Intelli	aent I/O)						
	Output Compare							8 (Intelli	gent I/O)						
Timer	PWM Output							13 (Timer A,	Intelligent I/C	))					
	Real-Time Port								_						
	Event Counter							11 (Timer	A, Timer B)	(0)					
	2-Phase Encoder Input					1 (aborada	3 with Timor A	Timer A) + 1	(Intelligent I/	(U) por P2_Dood	time timer)				
Watchdog Timer	3-Fhase Inverter Control					I (Shareu v	WIT TIME A	, Timer AT,	1	iel DZ, Dedu	ume umer)				
	Clock Sync./ Clock Async.							6 (UART, In	telligent I/O)						
Serial Interface	Clock Sync. Only							1 (Intelli	gent I/O)						
	Clock Async. Only								_						
I'C-bus								5 (U	ART)						
Smart Card/SIM								5 (U	ART)						
Synchronous Serial	Communication Unit/Special Serial I/O							5 (U	ART)						
CAN	Channels								2						
CAN	Message Box (Numbers)							16	×2						
IrDA	<b>0</b> 1 1:								-						
CRC Calculation	i Circuit						1 (C	RC-CCITT (	$X^{10} + X^{12} + X^{0}$	' + 1))					
Ar Converter	Input Only (Numbers)							Y	1						
	CMOS I/O (Numbers)	я	5	121	R	15	121	85	121	۶ ا	5	121	8	5	121
I/O Ports	N-Channel Open Drain Port (Numbers)		-						2				-	-	
	High Current Drive Port														
	Pull-Up Resistor	8	15	121	8	35	121	85	121	8	5	121	8	5	121
External Interrup	ots Pins							1	1						
Debugging	On-Chip Debug		_			Yes			_			Y	es		
Other	POM Correction Eurotion		Voc			res		v	-			ř	es -		
Functions	Others		163					3V 5V	nterface						
Operating Frequ	ency/Supply Voltage						32MH	z/4.2 to 5.5V	24MHz/3.01	to 5.5V					
Operating Ambie	ent Temperature (°C)							- 20 to 85	– 40 to 85						
		<	4	4	4	4	Ą	4	4	4	<	4	4	4	<
P. 1		E E	Υ Ψ	¥. ¥.	Å Å	Ц Ц	Υ.Υ.Υ.	μ. Ψ.	Ϋ́Υ.	8	Ř	¥ Y	S B	Ř	Υ Υ Υ
Раскаде**		100	100	144	100	100	144	100	144	100	100	144	100	100	144
		a PC	DPO	DPO	D D D	DPO	DPO	DP0	0HC	D D D	DO	DP0	aPc	DO	DPO
		PRC	LL0	PLO	L H	PLO	PLO	LL0	PLO	L AR	PLO	LL0	PRC	PLO	PLO
			_		_	_	_	_	_	_					_
		<u>e</u> .	0	<u>с</u>				*4	** d						
		XX	XX	XX				CXG	6XG						
Part No.		X-V	X-N	X-N	VFP	VGF	VGF	×+	×+	E E	GP	GP	£	с С	G G
		M8	We	2 M	3FV	Э. Б	25	3MF	5MF	3FF	35	25	3FJ	3FJ	5FJ
		085	085	085	085	085	085:	085	085:	085	085	085	085	085	085:
		Ψ	Ψ	M3	W3	W3	M3	M3	W3	W3	W3	W3	W3	ЮЗ	W3

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M32C/80 Series)

Group			-				Ma	32C/87 (	M32C/8	87)								M32C/8	37 (M32	C/87A)		
	BOM (Bytes)	38	4K	384K	+ 4K		512K		512K	+ 4K	768K	+ 4K		1M + 4K		38	4K	384K	+ 4K		12K	
	RAM (Bytes)		24	K				31K					48K				24	4K			31K	
Memory	ROM Type*1	Ν	N	F			М					F				Ν	N	F	-		М	
,	Data Flash		-	Yes	(4K)		-					Yes (4K)				-	-	Yes	(4K)		-	
	Program Security	-	-	ROM Code C	neck Function, stect Function)		-			R	OM Cod	e Protect	k Functio	on, n)		-	-	ROM Code Pr	neck Function, otect Function)		-	
	CPU				,						M3	2C/80 C	ore						,			
	Basic Instructions											108										
CPU	Minimum Instruction Execution Time (ns)										31.3	3 (@32M	IHz)									
	Multiplier										16	$6 \times 16 \rightarrow 3$	32									
	Barrel Shifter										10 ×	Yes	740									
DMA	DMAC (Channels)										-	4										
DMA	DTC/DMACII								DM	IACII (St	arts by a	ll periphe	eral inter	rupt facto	ors)							
	Address Space (Bytes)							-			(1) 0	16M	0.1									
External Bus Expansion	External Bus Interface		Se		from Se	narate hu	is Multi	Suppi	Data Bu	s Width	1 1 10 6 W	valt state	s, Outpu 8/16-bit)	The nur	-select s	gnais utout ad	dross hi	isos can	ha salar	ted (16/20)		
	DRAM Controller					burato bu	io, maia	biox buo,	Dulu Du	o maar	0011 00 0	_	0, 10 010	, 1110 1101		aiparaa		000 0011	00 00.00	iou (10/20)		
	Clock Generation Circuit							4	1 circuits	(Main cl	lock, PLL	, Sub-clo	ock and	On-chip o	oscillator	)						
	PLL											Yes										
Clock	Subclock											Yes										
CIOCK	Oscillation Stop Detection											Yes										
	Frequency Divider									1/n (r	n=1, 2, 3,	4, 6, 8, 1	10, 12, 1	4, 16)								
	Power Save										1	Wait/Stop	0									
Power Supply Voltage Detection	Power-On Reset/POR										Voc	— (1. ow. volt	200)									
Vollago Dotobilon	Low voltage Detection/LvD	10-hit	10-bit	10-bit	10-hit	10-	hit	10-bit	10-bit	10-hit	10-hit	10-bit	age) 10	-bit	10-hit	10-bit	10-bit	10-hit	10-bit	10-bi	t I	10-bit
A/D Converter	Hesolution × Channels	×26	× 34	× 26	× 34	×2	26	× 34	× 26	× 34	× 26	× 34	×	26	× 34	× 26	× 34	× 26	× 34	×26		× 34
A/D Converter	Sample and Hold											Yes										
D/A Convertor	Multi-Channel Sample and Hold											- 0 hit v 0										
D/A Converter	8-bit																					
	16-bit										11 (Tir	mer A, Ti	mer B)									
	Input Capture										8 (Ir	ntelligent	I/O)									
	Output Compare	10 (Intelligent	16 (Intelligent	10 (Intelligent	16 (Intelligent	10 (Inte	elligent	16 (Intelligent	10 (Intelligent	16 (Intelligent	10 (Intelligent	16 (Intelligent	10 (Int	elligent	16 (Intelligent	10 (Intelligent	16 (Intelligent	10 (Intelligent	16 (Intelligent	10 (Intell	gent	16 (Intelligent
		15 (Timer A	21 (Timer A	15 (Timer A	21 (Timer A	15 (Tir	ner A	21 (Timer A	15 (Timer A	21 (Timer A	15 (Timer A	21 (Timer A	15 (Ti	mer A	21 (Timer A	15 (Timer A	21 (Timer A	15/Timer A	21 (Timer A	15 (Time	er A	21 (Timer A
Timer	PWM Output	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intellige	ent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intellig	ent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligen	t I/O)	Intelligent I/O)
	Real-Time Port	3 (Intelligent	8 (Intelligent	3 (Intelligent	8 (Intelligent	3 (Inte	lligent	8 (Intelligent	3 (Intelligent	8 (Intelligent	3 (Intelligent	8 (Intelligent	3 (Inte	elligent	8 (Intelligent	3 (Intelligent	8 (Intelligent	3 (Intelligent	8 (Intelligent	3 (Intelli	gent	8 (Intelligent
	Event Counter	10)	10)	10)	10)	I/C	)	10)	1/0)	10)	11 /Tir	10)	I/	0)	10)	10)	10)	10)	10)	1/0)		10)
	2-Phase Encoder Input									3 (	(Timer A)	) + 1 (Inte	elliaent l	(0)								
	3-Phase Inverter Control							1 (shar	ed with T	Timer A4	, Timer A	A1, Timer	A2, Tim	er B2, D	ead time	e timer)						
Watchdog Timer	1											1										
	Clock Sync./ Clock Async.	7 (UART, Intelligent I/O)	8 (UART, Intelligent I/O)	7 (UART, Intelligent I/O)	8 (UART, Intelligent I/O)	7 (UA	ART,	8 (UART, Intelligent I/O)	7 (UART, Intelligent I/O)	8 (UART, Intelligent I/O)	7 (UART, Intelligent I/O)	8 (UART, Intelligent I/O)	7 (U Intellia	ART,	8 (UART, Intelligent I/O)	7 (UART, Intelligent I/O)	8 (UART, Intelligent I/O)	7 (UART, Intelligent I/O)	8 (UART, Intelligent I/O)	7 (UAF	RT,	8 (UART, Intelligent I/O)
Serial Interface	Clock Sync, Only	manganceo	(intelligence et el	intengent iroj	incargone (roj	intellige	Jin (00)	incongent (roy	inteligent (O)	intergen (0)	2 (Ir	telligent	1/0)	cii( 1/0)	intengent (O)	intengent (O)	mongontiroj	interingent (ro)	intelligent ir Of	intelligen	1/0)	inteligent (0)
	Clock Async. Only											-										
I <sup>2</sup> C-bus												5 (UART)	)									
IEBus Smart Card/SIM											6 (UAH	I, Intellig	ent I/O)									
Synchronous Serial	Communication Unit/Special Serial I/O											5 (UART)	)									
CAN	Channels							2	2			- (- )							1			
CAN	Message Box (Numbers)							16	×2										16			
IrDA	Circuit									1.00	Y	es (UAR	T) V <sup>12</sup> · V <sup>5</sup>									
X/Y Converter	Circuit									1 (Ci		Yes	X + X	+ 1))								
	Input Only (Numbers)											1										
	CMOS I/O (Numbers)	85	121	85	121	8	5	121	85	121	85	121	8	15	121	85	121	85	121	85		121
I/O Ports	N-Channel Open Drain Port (Numbers)											2										
	Pull-Up Resistor	85	121	85	121	8	5	121	85	121	85	121	6	15	121	85	121	85	121	85		121
External Interrup	its Pins	11	14	11	14	1	1	14	11	14	11	14	1	1	14	11	14	11	14	11		14
Debugging	On-Chip Debug	-	_	Ye	es		-					Yes				-	-	Ye	es		-	
Function	On-Board Flash Program	-	-	Ye	es		-					Yes				-	-	Ye	es		-	
Other	Others	Ye	es				Yes				3V	5V Interf	ace			Ye	es	-	-		res	
Operating Freque	ency/Supply Voltage									32MH	z/4.2 to 5	5.5V, 24N	1Hz/3.0	to 5.5V								
Operating Ambie	ent Temperature (°C)										– 20 to	o 85, – 40	) to 85									
		۲.	۲.	¥-	۲-	₹.	A-	۲-	¥-	٩.	×.	-P	۲.	A-	Ą.	A-	٩.	×-	۲-	A-	Ā	Ą.
Package*2		- Ke	A4	OKE	4K <sup>p</sup>	DOLE	OKE	4K <sup>p</sup>	OKE	44 A	OKE	4K <sup>p</sup>	I I	- KE	4K <sup>p</sup>	OKE	4K <sup>b</sup>	N KE	4K <sup>p</sup>	JOUE	8	4Kp
		010	014	010	014	2010	010	014	010	014	010	014	010	010	014	010	014	010	014	2010	010	014
		La L	Lo_	Ъ	D D	1 2 2 2	D D	Ъ	LQP	La L	LQP	-QP	l d	Ъ	Ъ	LQ L	LQ L	LQ_	Гар	10H	P	LQ L
		Ē	Ē	đ	đ	ā	E.	Ē	đ	Ē	Ē	Ē	ā	립	đ	Ъ	Ē	Ē	đ	ā	Ē	ā
																d.	<u>L</u>			4	٩	۹.
		XGF	XGF			ЧЪ	(GP	(GP								XCO	DXX DXX			KXFI	SXG	XG
Port Nr.		×-	XX-	L C	<u>с</u>	X	XX	XX	d C	d.	6	<u>д</u>	<u>a</u>	L.	d.	A-X.	A-X.	AGP	AGP	X-A	X-A	4-X)
ran nu.		MH	MH	3FH(	SFH	-CMS	-CMS	-CMS	SFJG	FJG	JFK(	3F K	FLF	PLG	3FL(	MH	MH	JEH,	SFH,	ſſWS	ILMS	'FWS
		3873	3875	3873	3875	0876	3876	3876	3876	3876	3879	387E	3879	3879	387E	0873	3875	3873	3875	0876	0876	3878
		M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(	M3(

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code  $\star$ : New product  $\star\star$ : Under development

### • Specifications (M32C/80 Series)

Group				M32C/8	37 (M32	2C/87A)								M32C/8	(M32C	/87B)					
	ROM (Bytes)	512k	( + 4K	768K	+ 4K	1	M + 4K		38	4K	384K	+ 4K	5	12K	512	K + 4K	768k	( + 4K	11	l + 4K	
	RAM (Bytes)	3	1K			48K				24	ικ	_		311					48K		
Memory	ROM Type***				F Vos (4K)				- P	-	ł Vos	(4K)						F Vos (4K)			
	Dutu Hush		Ye	es (ID Co	de Chec	k Functior	٦,				Yes (ID Code C	heck Function,				Y	es (ID Co	de Chec	k Function,		
	Program Security		B	ION Cod	e Protec	t Function	)				ROM Code Pr	otect Function)				F	ROM Cod	le Protec	t Function)		
	CPU Desis lastrutions										M3	2C/80 C	ore								
	Minimum Instruction Execution Time (ns)										31.3	3 (@32M	Hz)								
CPU	Multiplier										16	3×16→3	12								
	Multiply-Accumulate Instruction										16×	16 + 48-	→48								
	Barrel Shifter											Yes									
DMA	DTC/DMACII								DN	IACII (St	arts by a	4 Il periphe	eral interrup	factors)							
	Address Space (Bytes)											16M		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,							
External Bus	External Bus Interface							Supp	ort for in	sertion of	f 1 to 6 w	ait state	s, Outputs 4	chip-selec	t signals						
Expansion	Bus Structure		Se	electable	from Se	parate bus	s, Multip	olex bus,	Data Bu	s Width (	can be s	elected (	8/16-bit), Th	e number (	f output a	iddress b	uses can	be selec	ted (16/20)		
	Clock Generation Circuit							4	1 circuits	(Main cl	ock, PLL	, Sub-clo	ck and On-	chip oscilla	or)						
	PLL											Yes			<i>.</i>						
	Subclock											Yes									
Clock	On-Chip Oscillator											Yes									
	Frequency Divider									1/n (n	=1, 2, 3,	4, 6, 8, 1	10, 12, 14, 1	6)							
	Power Save										1	Vait/Stop	)	,							
Power Supply	Power-On Reset/POR										N/	-									
Voltage Detection	Low voltage Detection/LvD	10-bit	10-bit	10-bit	10-bit	10-1	oit	10-bit	10-bit	10-bit	10-bit	LOW VOIL	age) 10-bit	10-1	it 10-bi	10-bit	10-bit	10-bit	10-bit		10-bit
	Resolution × Channels	×26	× 34	×26	× 34	×2	6	×34	×26	× 34	×26	×34	×26	×3	4 ×26	×34	×26	×34	×26		×34
A/D Converter	Sample and Hold											Yes									
D/A O	Multi-Channel Sample and Hold											-									
D/A Converter	Resolution × Channels 8-bit	303																			
	16-bit										11 (Tir	ner A, Ti	mer B)								
	Input Capture										8 (Ir	itelligent	I/O)				1	1			
	Output Company	16	10	16 //atallianat	10 //====	16	10	16	10	16	10 (latalling)		16								
	Output Compare	(inteiligent I/O)	(inteiligent I/O)	I/O)	(Intelligent	TO (Intellig	ent I/O)	(inteiligent I/O)	(inteiligent I/O)	(inteiligent I/O)	(Intelligent I/O)	(inteiligent I/O)	ro (intelligen	l/O) (intellig	inteilige	I/O)	l (inteiligent	(Intelligent I/O)	10 (Intellige	11 1/0)	(Intelligent I/O)
		Image: Non-State         Image: Non-State<														21 (Timer A.			21 (Timer A.		
Timer	PWM Output	Hold														Intelligent	15 (Time Intelligent	r A, I/O)	Intelligent		
																10)			10)		
	Real-Time Port															8 (Intelligent	3 (Intelliger	t I/O)	8 (Intelligent		
																` I/O)		,	1/0)		
	Event Counter										11 (Tir	ner A, Ti	mer B)								
	2-Phase Encoder Input 3-Phase Inverter Control							1 (shar	ed with "	3 ( Fimer A4	Timer A	+ 1 (Inte 1 Timer	A2 Timer I	32 Dead t	me timer						
Watchdog Timer								i (ontai	ou mar		, 1111017	1	, in the second se	, <u>Doud</u>							
		7 (UART,	8 (UART,	7 (UART,	8 (UART,	7 (1)4	BT	8 (UART,	7 (UART,	8 (UART,	7 (UART,	8 (UART,	7 (1148	8 (UA	T, 7 (UAR	r, 8 (UART,	7 (UART,	8 (UART,	7 (1)46	т	8 (UART,
Sorial Interface	Clock Sync./ Clock Async.	Intelligent I/O)	Intelligent I/O)	Intelligent	Intelligent	Intelliger	nt I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent I/O)	Intelligent	I/O)	ent Intelliger	nt   Intelligen I/O)	t Intelligent	Intelligent I/O)	Intelligent	i/O)	Intelligent I/O)
Senai interiace	Clock Sync. Only	,	,	,	,			,	,	,	2 (Ir	telligent	I/O)		,	,	,	,			,
	Clock Async. Only										,	-									
I <sup>2</sup> C-bus												5 (UART)									
IEBus Smart Card/SIM											6 (UAR	T, Intellig	ent I/O)								
Synchronous Serial	Communication Unit/Special Serial I/O											5 (UART)									
CAN	Channels				1										-						
1.54	Message Box (Numbers)				16							(114.00	Pr \		_						
CBC Calculation	Circuit									1 (CF		T (X <sup>16</sup> +	$\frac{1}{X^{12} + X^5 + 1}$	))							
X/Y Converter												Yes		,,,							
	Input Only (Numbers)											1									
I/O Porte	CMOS I/O (Numbers)	85	121	85	121	85		121	85	121	85	121	85	12	85	121	85	121	85		121
I/O FOILS	High Current Drive Port											_									
	Pull-Up Resistor	85	121	85	121	85		121	85	121	85	121	85	12	85	121	85	121	85		121
External Interrup	ots Pins	11	14	11	14	11		14	11	14	11	14	11	14	11	14	11	14	11		14
Debugging	On-Chip Debug				Yes				-	-	Ye	es S						Yes			
Other	ROM Correction Function				_				Ye	es	-	-	```	'es				_			
Functions	Others										3V,	5V Interf	ace								
Operating Frequ	ency/Supply Voltage									32MHz	z/4.2 to 5	.5V, 24N	1Hz/3.0 to 5	.5V							
Operating Amble	ent temperature ( C)										- 20 10	85, - 40	10 85	1		1					
						_	_				_	_	_			-		_		_	_
		-0	4-4>	-	4-42	-BL	4	4-A>	4	4-A>	9-1	4-A	7-8F		9-1	A-4	4	4-A>	-E	4	4-4>
Package*2		00	144	0	144	100	10	144	1001	144	100	144	100	10 14	100	44	001	144	100	0	144
		DAC	DAC	DAC	-O-dC	0 AC	-O-LC	DAC	-O-dC	DOLC	DOLC	.04č	2P0	Dec loc	-Odč	DAC	.04C	DOG	0 dc	DAC	DOLC
		PLC	PLG	PLC	PLC	РВ	PLC	PLC	PLG	PLC	PLC	PLC	РВС	PLG   PLC	PLC	PLG	PLG	PLG	A	PLC	PLC
									XGP	XGP			Υ <sup>E</sup> P	GP (GP							
		d.	<u>د</u>	6	Ъ	<u>A</u>	6	d U	XX-	XX-	GР	Ъ	XX-	X X	<u>L</u>	<u>C</u>	d C	GР	<u>e</u>	6	6
Part No.		JAG	JAG	KAC	-KA	:LAF	-LAC	-LA(	AHB	AHB	HB	HB	AJB.	AJB-	JBG	JBG	KBC	KB	LBF	LB	-LB(
		376F	378F	379F	37BF	379F	379F	37BF	373N	375N	373F	375F	876h	376h	376F	378F	379F	37BF	879F	379F	37BF
		1305	1305	1305	1306	M306	M306	1306	1306	1306	M306	M306	M30	1306	1306	1305	1305	1305	M30(	M30	1305
	DOM Incoming		C BOM v	arsion C	· One tir		version	07.0		arsion	_	-	_		-	-	+ · Now	product	++ · Linde	r dovo	lonment
*1 F : Flash memo	IV Version, L : RUIVI-less version	W . W	VIII			110 1 1 1 1 1 1 1			CI IV									DIOLIN			

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### Specifications (M16C/80 Series)

Group													M16	C/80											
αισαρ													WITO	0,00			01/						01/		
	HOM (Bytes)							-								12	вK			<u> </u>		25	6K		
	RAM (Bytes)			10	ЭK					24	4K					10	)K					20	)K		
	ROM Type*1						I	-							=	N 1	Л	F	М	1	=	N 1	Л	F	M
	Data Flash												-	-											
Memory														N. 11				Yes (ID		N 01				Yes (ID	
														Yes (II	O Code			Code Check		Yes (IE	Code			Code Check	
	Program Security						-	-						ROM	Code	-	-	PUNCION, BOM Code	-	ROM	Code	-	-	Punctori, BOM Code	-
														Protect I	Function)			Protect		Protect F	Function)			Protect	
															,			Function)			,			Function)	
	CPU												M16C/8	30 Core											
	Basic Instructions												10	06											
0.011	Minimum Instruction Execution Time (ns)												50 (@2	20MHz)											
CPU	Multiplier												16×1	6→32											
	Multiply-Accumulate Instruction											1	6×16·	+ 48→4	8										
	Barrel Shifter												-	-											
5144	DMAC (Channels)													4											
DIMA	DTC/DMACII												-	-											
	Address Space (Bytes)												16	6M											
External Bus	External Bus Interface								Supp	ort for in	nsertion	of 1 to	3 wait s	states, C	Dutputs	4 chip-	select s	ignals							
Expansion	Bus Structure			Selecta	ble fron	n Separ	ate bus	, Multip	lex bus,	Data b	us widt	n can be	e select	ed (8/16	6-bit), T	he num	ber of c	output ad	ddress I	buses c	an be s	elected	(16/20)	)	
	DRAM Controller												Y	es											
	Clock Generation Circuit										2	circuits	(Main	clock, S	ub-cloc	k)									
	PLL												-	-											
	Subclock												Y	es											
Clock	On-Chip Oscillator												-	-											
	Oscillation Stop Detection												-	-											
	Frequency Divider										1/n	(n=1, 2	, 3, 4, 6	6, 8, 10,	12, 14,	16)									
	Power Save												Wait	/Stop											
Power Supply	Power-On Reset/POR												-												
Voltage Detection	Low Voltage Detection/LVD												-	-											
	Resolution × Channels												10-bi	t × 10											
A/D Converter	Sample and Hold												Y	es											
	Multi-Channel Sample and Hold												-	_											
D/A Converter	Resolution × Channels												8-bi	t×2											
	8-bit												-	-											
	16-bit											11	(Timer .	A, Time	rB)										
	Input Capture												-	-											
	Output Compare												-	-											
Timer	PWM Output												5 (Tir	ner A)											
	Real-Time Port												-	-											
	Event Counter											11	(Timer	A, Time	r B)										
	2-Phase Encoder Input												3 (Tir	ner A)			-								
	3-Phase Inverter Control								1 (sha	red with	Timer	A4, Tim	er A1, 7	Timer A	2, Time	r B2, De	ead time	e timer)							
Watchdog Timer														1											
	Clock Sync./ Clock Async.												5 (U	ART)											
Serial Interface	Clock Sync. Only												-	-											
	Clock Async. Only			_									-												
I*C-bus				_					_		_		3 (U	ARI)						_				_	
IEBUS		——											3 (U	ART)											
Smart Card/SIM	0												3 (U	ART)											
Synchronous Serial	Communication Unit/Special Senai I/O												3 (0.	ART)											
CAN	Magaga Roy (Numbere)																								
IrDA	Message Box (Numbers)																								
CBC Coloulation	Circuit										1 /	CRC C		v16 , v1	2. 15.	1))									
V/V Convertor	Circuit										10		viii ()	<u>+ + </u>	+ ^ +	1))									
Arr Converter	Input Only (Numbers)												Ť.	1											
	CMOS I/O (Numbers)			5		0	1			5		ρ	1			5		11	21		0	5		11	21
I/O Porte	N-Channel Open Drain Port (Numbers)		4			0	•		4			0	•	2				1 14	- '		0	~		1 14	
	High Current Drive Port												-	_											
	Pull-Un Resistor		л	5		0	1			5		0	1		-	5		1	21		0	5		1/	21
External Interrup	ts Pins		4			0	·		4			0	. 1	1				1 14	- 1		0	~		1 14	_ 1
Debugging	On-Chip Debug							_					1		35	-	_	Yes	_	V	35	-	_	Yes	-
Function	On-Board Flash Program							_							35		_	Yes	_		35	-	_	Yes	-
Other	ROM Correction Function							-	_						-	Y/	es	-	Yes	-	-	Y/	es	-	Yes
Functions	Others												-	_											
Operating Freque	ency/Supply Voltage										20M	Hz/4.21	to 5.5V.	10MHz	/2.7 to	5.5V									
Operating Ambie	ent Temperature (°C)											- 2	0 to 85.	- 40 to	85										
			-		_		_		_		_				-				_				-		_
		A-A	5		4		ł		4-12		4		L C	B-A	B-A	B-A	B-A		ł	B-A	B-A	B-A	B-A		A-F
Package*2			3	2	Ś	Ì	4		3	2	Ś	K	É		No.		No.		2 1	N N	No.	l g	N N	Ì	44
		60	5				1	2	5		50	6	5	010	010	010	010		1	010	010	010	010		P14
		e e	ž		5		Ľ J	8	ž		5		3	٩ ۵	QP	٩ ۵	QP		J J	٩ ۵	QP	d d	QP		5
		l ä		2	Ľ L			8	I L	a	Ľ L	i	2	h H	PL	h H	PL		L L	P H	PL	H H	PL	2	Ľ L
			2		5		2		-		5		2			0	٩		٩			0	٩		٩
			Note		No.		Se la		Note		<sup>S</sup> N		<sup>S</sup>			XFF	XG		XG			H X	XG		XG
-			-BL		-BL		-BI		BL		-BI	0	-BI	٩.	<u>م</u>	X	X	L.	X	<u>a</u>	d C	X	X	<u>d</u>	X
Part No.		2FP	SFP	GF	GF	GF	GF	SFP	2FP	GF	GGF	SGF	GF	L L	<sup>0</sup>	40	-0	l O	<sup>2</sup>	GF	00-	-9V	-9V	99	NG-
		00	000	000	00	025	02	03	036	036	036	055	055	OOF	00	00	000	02F	02N	03F	03F	030	031	05F	050
		308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308	308
		ž	ž	Ξ	Ξ	ž	ž	Ξ	ž	Ξ	ž	ž	ž	Ξ	ž	Ξ	Ξ	Ξ	Ξ	Ξ	ž	ž	ž	Ξ	ž

<sup>1</sup> Built-in boot loader function ROM-less version <sup>\*1</sup> F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QZROM version <sup>\*2</sup> Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

 $\star$ : New product  $\star\star$ : Under development

#### • Specifications (M16C/60 Series)

<u> </u>	```		/										
Group					M16	C/64					M16	C/65	
	POM (Poter)		05.01/	. 0.41/			5101	. 0.41/			05.01/	0.416	
	DAM (Dutes)		2000	+ 24N			512K	+ 24K			2000	+ 24K	
Mamaa	POM Trace*1		10	n			3	-			20	JK	
Memory	ROM Type							-					
	Data Flash					Vee (ID Cede (	Tes	(BK)	ate at Eurotian)				
	Program Security					res (ID Code C	JNECK FUNCTION	, ROIVI Code PI	olect Function)				
	CPU						M16C/6	50 Core					
	Basic Instructions						9	1					
CPU	Minimum Instruction Execution Time (ns)				40.0 (@	25MHz)					31.3 (@	32MHz)	
0.0	Multiplier						16×1	6→32					
	Multiply-Accumulate Instruction						16×16 ·	+ 32→32					
	Barrel Shifter						-	_					
DMA	DMAC (Channels)						4	4					
DIVIA	DTC/DMACII						-	-					
	Address Space (Bytes)						1	М					
			Suppo	ort for insertion	of 0 to 3 wait s	tates, Outputs	4 chip-select si	anals.		Support for inser	tion of 0 to 5 wait s	tates. Outputs 4 ch	nip-select signals.
External Bus	External Bus Interface			Available to 4N	I bytes by addr	ess space exp	ansion function	5		Available to	o 4M bytes by addr	ess space expansi	on function
Expansion					Selectable fro	m Separate bu	s. Multiplex bus	. Data Bus Wid	ith can be seled	ted (8/16-bit).			
	Bus Structure				Th	ne number of or	utput address b	uses can be se	elected (12/16/2	20)			
	DBAM Controller						-	_					
	Clock Generation Circuit					4 circuits (Ma	in clock, PLL, S	Sub clock. On-c	hip oscillator)				
	PLI					- Chicano (inc	Y		nip oconiatory				
	Subclock						Vec (32	768kHz)					
	Boal Time clock				-	_	103 (02.	700((12)			V	20	
Clock	On-Chin Oscillator				Vec (Low c-	ood-1252-1-1	-			Voo /L!!-	th speed-4014	7   0w encode	125kH->\
	Oscillation Stor Detection				ies (LOW Sp	000.12JKHZ)	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	20			an apeeu.401VIF	z, Low speed:	12JKI 12)
	Frequency Divider						1/n /n_1 /	2 / 9 10)					
	Power Save						1/11 (11=1, 4	_, +, 0, 10) /Stop					
	Power Save						VVdit	Stop			X		
Power Supply	Fower-On Reset/POR					(volta ==)					Yes AL	dotoction O	
Voltage Detection	Low voltage Detection/LVD				Yes (Low	/ voitage)					Yes (Voltage	detection 3)	
	Resolution × Channels						10-bi	t×26					
A/D Converter	Sample and Hold						Ye	es					
	Multi-Channel Sample and Hold						-	-					
D/A Converter	Resolution × Channels						8-bit	t× 2					
	8-bit						-	-					
	16-bit						11 (Timer	A, Timer B)					
	Input Capture						-	-					
	Output Compare						-	_					
Timer	PWM Output				5 (Tin	ner A)					7 (Timer A, P	WM Function)	
	Real-Time Port						-	_					
	Event Counter						11 (Timer	A, Timer B)					
	2-Phase Encoder Input						3 (Tin	ner A)					
	3-Phase Inverter Control				1 (sha	red with Timer	A4, Timer A1, T	imer A2, Timer	r B2, Dead time	timer)			
Watchdog Timer								1					
	Clock Sync./ Clock Async.						6 (U	ART)					
Serial Interface	Clock Sync, Only						2 (S	5I/O)					
	Clock Async, Only						-	_					
I <sup>2</sup> C-bus					6 (U	ABT)					7 (Multi mast	er I <sup>2</sup> C, UART)	
IEBus						,	6 (U	ART)					
Smart Card/SIM							1 (U	ABT)					
Synchronous Serial	Communication Unit/Special Serial I/O						6 (U	ART)					
ojnomonodo oonar	Channels							-					
CAN	Message Box (Numbers)						-	_					
IrDA	Incodage Box (Hamberd)						-	_					
CBC Calculation	Circuit			1	(CBC-CCITT (	X <sup>16</sup> + X <sup>12</sup> + X <sup>5</sup> +	1))			1 (CBC-CCITT	$(X^{16} + X^{12} + X^5)$	1)/CBC-16 (Y10	$(3^{15} + \chi^{15} + \chi^{2} + 1))$
V/V Convertor	l'Oliculi			1		A TA TA T		_		1 (010-00111		1)/0110-10 (X	TA TA T I))
70 i Converter	Input Only (Numbers)							_					
	CMOS I/O (Numbers)							5					
I/O Porte	N-Channel Open Drain Port (Numbers)						8	3					
"O T OILS	High Curront Drive Port							_					
	Buill Us Desister							-					
Extornel later							8	0					
External interrup	lo ol: D.						I	3					
Debugging							Ye	35					
FUNCTION	On-Board Flash Program						Ye	es					
Other	ROM Correction Function							-					
Functions	Others				3V, 5V I	nterface				3V, 5	V Interface Par	tern Matching	Input
Operating Freque	ency/Supply Voltage				25MHz/2	.7 to 5.5V					32MHz/2	.7 to 5.5V	
Operating Ambie	ent lemperature (°C)	- 40	to 85	- 20	to 85	- 40	to 85	- 20	to 85	- 40	to 85	- 20	to 85
		m	Ą	ė	~	<b>≮</b>	ņ	Ą	ė	Ą		p	Ą
		ġ	<u> </u>	ġ	5		ġ	÷.	ġ	<u> </u>	4	5	<u> </u>
Package*2		00	00	100		8	100	00	100	00			00
		PO1	105	PO	3		PO1	-0c	PO1	-00 -		2	-01 -01
		ğ	ja,	ğ		2 Z	õ	a'	ğ	ğ	2	Ž	ja.
		Ľ.	1	14	ā	L	μ.	Ц	ä	Ц		Ē	L L
							Ì						
		*	*.	*	*	*	*.	*	\$	:	*	\$	*
		FA'	E L	FA'	Ш Ц	E	FA	8	FA	E E	FA'	FA'	E E
Part No.		00		ND	ND	QW	QW	2 M	N N N N N N N N N N N N N N N N N N N	Ð		Z	Z
		340	340	340	340	340	340	340	340	350	350	350	220
		F36	F36	F36	F36	F36	F36	F36	F36	F36	F36	F36	F36
		R5	R5	R5	R5	R5	R5	R5	R5	R5	R5	R5	R5

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/60 Series)

Group										N	116C/62	Р								
	ROM (Bytes)				-	-				48	зк		64K			64K + 4ł	<		96K	
	RAM (Bytes) ROM Type <sup>*1</sup>	10	)K	20	DK I	31 _	IK					4	K			F			5K M	
Memory	Data Flash							-								Yes (4K)	)		-	
	Program Security							-							Yes (ID Co ROM Coo	ode Checi le Protect	k Function, Function)		-	
	CPU Desis lastrusticas									M	6C/60 C	ore								
	Minimum Instruction Execution Time (ns)									41.	91 7 (@24M	Hz)								
CPU	Multiplier									1	6×16→3	32								
	Multiply-Accumulate Instruction Barrel Shifter									16>	(16 + 32-	→32								
DMA	DMAC (Channels)										2									
	Address Space (Bytes)						1	M						-	11	N	-	1N	1	-
External Bus	External Bus Interface			Suppor A	t for inser wailable to	tion of 1 t o 4M byte	o 3 wait s s by addr	tates, Ou ess space	tputs 4 ch e expansi	ip-select on functio	signals, n			_	Support fo of 1 to 3 w Outputs 4 o signals, Ava bytes by add expansion	r insertion ait states, chip-select ilable to 4M dress space in function		Support for of 1 to 3 wa Outputs 4 cl signals, Avail bytes by addu expansion	insertion it states, hip-select able to 4M ress space function	_
Expansion	Bus Structure		Select	table from The	Separate	e bus, Mul of output a	tiplex bus address b	, Data Bu uses can	is Width c be select	an be sel ed (12/16	ected (8/ 5/20)	16-bit),		-	Selectable fro bus, Multi Data Bus W selected (8/ number of ou buses can b (12/1)	om Separate plex bus, idth can be 16-bit), The tput address be selected 6/20)		Selectable from bus, Multip Data Bus Win selected (8/1 number of out buses can be (12/16	m Separate lex bus, dth can be 6-bit), The put address e selected /20)	_
	DRAM Controller							4 cire	uite (Mai	n clock P		lock On-	chin osci	llator)						
	PLL							4 010	Juits (Iviai	T CIOCK, T	Yes	100K, 011-	chip 030	nator)						
Clock	Subclock		Yes Yes Ves																	
CIOCK	Oscillation Stop Detection		Yes Yes 1/n (n=1, 2, 4, 8, 16)																	
	Frequency Divider		Yes 1/n (n=1, 2, 4, 8, 16) Wait/Stop																	
Power Supply	Power-On Reset/POR										-	,								
Voltage Detection	Low Voltage Detection/LVD Resolution × Channels									Yes	(Low volt	age) 6								
A/D Converter	Sample and Hold										Yes									
D/A Converter	Multi-Channel Sample and Hold Resolution × Channels										- 8-bit x 2									
DIA COnverter	8-bit										-									
	16-bit Input Capture									11 (Ti	mer A, Ti	mer B)								
	Output Compare										-			1						1
Timer	PWM Output Beal-Time Port						5 (Tin	ner A)			_			3 (Timer A)	5 (Tim	ner A)	3 (Timer A)	5 (Tim	er A)	3 (Timer A)
Timer	Event Counter									11 (Ti	mer A, Ti	mer B)								
	2-Phase Encoder Input						3 (Tin	ner A)						2 (Timer A)	3 (Tim	her A)	2 (Timer A)	3 (Tim	er A)	2 (Timer A)
	3-Phase Inverter Control			1 (share	d with Tin	ner A4, Ti	mer A1, T	imer A2,	Timer B2	Dead tin	ne timer)			-	Timer A1, Tim B2, Dead t	in Timer A4, her A2, Timer ime timer)	_	Timer A1, Time B2, Dead tir	er A2, Timer ne timer)	-
Watchdog Timer	Clock Sync / Clock Async						3 (1)	ART)			1			2 (LIART)	3 (1)4	ART)	2 (LIABT)	3 (LIA	BT)	2 (LIART)
Serial Interface	Clock Sync. Only						0 (0,	,			2 (SI/O)			12 (0/111)	0 (0/	,	12 (0/411)	0 (0/1	,	2 (0/111)
l <sup>2</sup> C-bus	Clock Async. Only						-	-			3 (LIART)			1 (UART)		-	1 (UART)	-		1 (UART)
IEBus											3 (UART)	)								
Smart Card/SIM	Communication Unit/Special Serial I/O										1 (UART) 3 (UART)	)								
CAN	Channels										-									
IrDA	Message Box (Numbers)																			
CRC Calculation	Circuit								1 (0	CRC-CCI	TT (X <sup>16</sup> +	X <sup>12</sup> + X <sup>5</sup> +	1))							
X/Y Converter	Input Only (Numbers)										- 1			-						
100	CMOS I/O (Numbers)				5	0					6	15		68	8	5	68	85	i	68
I/O Ports	N-Channel Open Drain Port (Numbers) High Current Drive Port										2									
External later	Pull-Up Resistor				5	i0		1			8	15		68	8	5	68	85	i	68
Debugging	On-Chip Debug						1							8	1	Yes	8	11	_	8
Function	On-Board Flash Program							-								Yes			-	
Functions	Others							163		3V,	5V interf	ace							163	
Operating Freque	ency/Supply Voltage	3V, 5V interface 24MHz/3.0 to 5.5V, 10MH2/2.7 to 20 to 55.4V, 10MH2/2.7 to								5.5V										
Operating Amble	ant temperature ( C)									- 20 1	0 85, - 40	10 65								
Package*2		PRQP0100JB-A	PLQP0100KB-A	PRQP0100JB-A	PLQP0100KB-A	PRQP0100JB-A	PLQP0100KB-A	PRQP0100JB-A	PLQP0100KB-A	PRQP0100JB-A	PLQP0100KB-A	PRQP0100JB-A	PLQP0100KB-A	PRQP0080JA-A	PRQP0100JB-A	PLQP0100KB-A	PRQP0080JA-A	PRQP0100JB-A	PLQP0100KB-A	PRQP0080JA-A
										(XFP	CXGP	(XFP	KGP	KGP				XXFP	XGP	KXGP
Part No.		0620SPFP	0620SPGP	0624SPFP	0624SPGP	0626SPFP	0626SPGP	0622SPFP	0622SPGP	0622M6P-XX	0622M6P-XX	0622M8P-XX	0622M8P-XX	0623M8P-XX	0622F8PFP	0622F8PGP	0623F8PGP	0622MAP-XX	0622MAP-XX	0623MAP-XX
		Β	Ξ	Ξ	EΨ	Ξ	Β	Β	Β	ΒM	Ξ	Β	M3	E E	В В	εW	Ψ	Β	θW	Ξ

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QZROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/60 Series : M16C/62P Group)

Group												Μ	116C/62	2P										
	BOM (Bytes)	1:	28K		1	28K + 4	ıĸ		192K				25	6K				2	56K + 4	к			320K	_
	RAM (Bytes)	12	2011	10	JK I	2010 + -	TIX .		1021	12	2K		20				20	)K	001(++				16K	
Mamaani	ROM Type*1		М			F						М							F				М	-
wemory	Data Flash		-		,	Yes (4K	)					-						`	Yes (4K	)			-	
	Program Security		_		Yes (ID C	ode Check	k Function,					_					Yes	(ID Cod	de Cheo	k Functi	ion,		_	
	CRU				HUM CO	ue Protect	Function)					M4	6C/60 C	ore			RU		Protec	Function	on)			
	Basic Instructions											IVI I	91	ore										
	Minimum Instruction Execution Time (ns)											41.7	7 (@24N	(Hz)										
CPU	Multiplier											16	6×16→	32										
	Multiply-Accumulate Instruction											16×	16 + 32	→32										
	Barrel Shifter												-											
DMA	DMAC (Channels)												2											
	DTC/DMACII												-											
	Address Space (Bytes)	1M		_	0	M	-									1M								
External Bus	External Bus Interface	of 1 to 3 wait si Outputs 4 chip- signals, Availal 4M bytes by ad space expans function	tates, select ble to Idress sion	-	of 1 to 3 w Outputs 4 signals, A 4M bytes t space ex func	vait states, chip-select vailable to by address kpansion ction	_				S	Support Av	for inse vailable t	rtion of to 4M by	1 to 3 w ytes by a	ait state: address	s, Outpu space e	its 4 chi xpansio	p-selec n functi	t signals	,			
Expansion	Bus Structure	Selectable fr Separate bu Multiplex bus, Bus Width can selected (8/16 The number of address buses of selected (12/11	om Js, Data n be i-bit), output can be 6/20)	-	Selectal Separa Multiplex Bus Widt selected The numbe address bu selected (	ble from ate bus, bus, Data th can be (8/16-bit), er of output ises can be (12/16/20)	-			S	ielectabl	e from The	Separat number	e bus, N of outpi	Aultiplex ut addre	bus, Da ss buses	ta Bus \ s can be	Width ca selecte	an be se ed (12/1	elected ( 6/20)	8/16-bit	),		
	DRAM Controller												-											
	Clock Generation Circuit								4	circuits	(Main c	lock, Pl	LL, Sub	clock, C	On-chip o	oscillator	)							
	PLL		Yes Yes																					
Clock	Subclock												Yes											
CIUCK	Oscillation Stop Detection												Vos											
	Frequency Divider											1/n (n	=1, 2, 4,	8, 16)										
	Power Save											1	Wait/Sto	p										
Power Supply	Power-On Reset/POR												-											
Voltage Detection	Low Voltage Detection/LVD											Yes	(Low vol	tage)										
	Resolution × Channels											1	0-bit × 2	6										
A/D Converter	Sample and Hold												Yes											
D/A Converter	Besolution × Channels												8-hit × 2	,										
DIA CONVERCE	8-bit												-											
	16-bit											11 (Tir	ner A, T	imer B)										
	Input Capture											1	-	,										-
	Output Compare												-											
	PWM Output	5 (Timer	A)	3 (Timer A)	5 (Tin	ner A)	3 (Timer A)								5	(Timer A	۹)							
Timer	Real-Time Port																							
	Event Counter	0.(7)	•	0.T. IV	0.(7)		0.77					11 (Tir	mer A, T	imer B)		( <b>T</b> )								
	2-Phase Encoder Input	3 (Timer	A)	2 (Timer A)	3(110	ner A)	2 (Timer A)								3	(Timer /	4)							
	3-Phase Inverter Control	1 (shared with 1 in Timer A1. Timer A2	1er A4, 2. Timer	_	1 (shared wi Timer A1. Tin	ith Limer A4, ner A2. Timer	_				1	(shared	d with Ti	mer A4.	Timer A	1. Time	r A2. Tir	ner B2.	Dead ti	me time	r)			
		B2, Dead time ti	imer)		B2, Dead	time timer)						(011010)			1111017	,	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		Doud i		• /			
Watchdog Timer													1											
	Clock Sync./ Clock Async.	3 (UAR	Τ)	2 (UART)	3 (U/	ART)	2 (UART)								3	B (UART	)							
Serial Interface	Clock Sync. Only												2 (SI/O)											
I <sup>2</sup> C bus	Clock Async. Only	-		1 (UART)	-		1 (UART)							)		-								
IFBus													3 (UART	)										
Smart Card/SIM													1 (UART	)										
Synchronous Serial	Communication Unit/Special Serial I/O											;	3 (UART	)										
CAN	Channels												_											
CAN	Message Box (Numbers)												-											
IrDA													-	10										
CRC Calculation	Circuit										1 (CR0	C-CCI	ГТ (Х <sup>10</sup> +	X'* + X	(* + 1))									
A r Converter	Input Only (Numbers)												1											
	CMOS I/O (Numbers)	85		68	8	5	68	8	5	111	8	5	111	8	15	111	8	5	111		8	15		111
I/O Ports	N-Channel Open Drain Port (Numbers)												2											
	High Current Drive Port												_											
<b>F</b> 1	Pull-Up Resistor	85		68	8	5	68	8	5	111	8	5	111	8	15	111	8	5	111		8	15		111
External Interrup	On Chin Dohug	11	_	8	1	I Vo-	8	<u> </u>				_							Vac					
Debugging	On-Onip Debug					Ves													Ves					
Other	ROM Correction Function	Y	/es			_						Yes							-				Yes	
Functions	Others											3V,	5V inter	face										
Operating Freque	ency/Supply Voltage										24MHz/	3.0 to 5	5.5V, 10	/Hz/2.7	to 5.5V									
Operating Ambie	ent Temperature (°C)											– 20 to	85, -4	0 to 85										
																								1
Deales as *2		A-BLA	80016-A 800										JKB-A	3KB-A										
aundye -		010	10	008	010	10(	008	010	10(	128	010	110(	128	010	310(	128	010	10(	128	010	010(	010	310(	128
		QP	A D	QPI	OP	a PC	OP(	- GP	aPc	В	QPI	аРс	D PC	OP(	aPc	L A C	QPI	Ч С С	aPc	QPI	aPc	Ö	aPc	aPc
		H H	PL	Ë	В. Н	PL(	ЪВ	PR	PLO	PLO	ЪВ	PLO	PLO	H H	PLC	PLC	PR	PLC	PLO	Ъ.	PLO	H H	PLC	PLO
							1					-	-		-	-						-	0	0
		Ϋ́FΡ	ĞР Ч	(GP				ЧЧ	(GP	(GP	КFР	KGP	KGP	KFP	KGP	KGP						XFP	XGF	XGF
		X	X	X	٩	L.	<u>د</u>	X	XX	XX	X	XX	×	X	X	X	٩	d.	٩.	٩	d.	X	X	X-
Part No.		CP.	Ч,	CP-	PPF	DPG	CPG	ЧЦ Ш	ËP	ËP	GP-	GP-	GP-	GP-	GP-	GP-	GPF	BPG	GPG	GPF	GPG	WP.	WP.	WP.
		WO	MON	N N	OFO	OFO	TF	M	M	3M	N N	ZM	3M	4M	4M	5M	4F(	4F(	SF(	LFC	LF	ZM	2M	3M
		062	3062	290	062	062	062	062	290	062	290	062	062	062	062	062	290	290	062	062	062	062	062	062
		E I	Σ	ШЗ	ВМ	M3	M3	M3	MЗ	ШЗ	Β	M3	Ξ 33	M3	MЗ	M3	ШЗ	ШЗ	M3	M3	ШЗ	M3	MЗ	M3
*1 E · Elash memo	ry version L · BOM-less version	M · Mask B	OMV	ersion	0 · 0ne	timo P	BOM	rsion 0	7 · O7P	OM yor	sion								A . I		duct 4	+ i l loc	lor dovo	lonmon

<sup>\*2</sup> Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/60 Series : M16C/62P Group)

Group													M160	C/62P											
	BOM (Butes)	<u> </u>		20	OK							38414					0	R4K + 4	ĸ		5124		F	12K + 4	ĸ
	BAM (Bytes)		2414	32		211/			164		r	204K					3	J+r∖ + 4	1\ 24	ĸ	JIZK		5	12N + 4	N
	POM Tupo*1	<u> </u>	∠4N		L	311			101		L	∠4N						F	31	r\	64		<u> </u>	F	
Memory	Data Elash	<u> </u>		-					1/1									r"			1/1	-	<u> </u>	F /oc / ///	
	Data Flash	<u> </u>															Vee /ID C	res (4r)	Eurotian				Vee (ID C	res (4rt)	Eurotion
	Program Security								-								ROM Co	de Protect	Function)		-		ROM Co	de Protect I	Function)
	CPU												M16C/	60 Core											
	Basic Instructions													1											
	Minimum Instruction Execution Time (ns)												11.7 (@	24MHz	)										
CPU	Multiplier												16 × 1	6→32	/										
	Multiply-Accumulate Instruction	<u> </u>										1	6 × 16	+ 32→3	2										
	Barrel Shifter						-		-				-	_											
	DMAC (Channels)													2											
DMA	DTC/DMACII													_											
-	Address Space (Bytes)												1	М											
External Bus	External Bus Interface				Suppo	ort for in	sertion	of 1 to	3 wait s	tates, C	Dutputs	4 chip-s	elect si	ignals, /	Available	e to 4M	bytes b	y addre	ss spac	e expai	nsion fu	nction			
Expansion	Bus Structure		S	electabl	e from \$	Separat	e bus, l	Multiple:	x bus, D	ata Bu	s Width	can be	selecte	d (8/16	-bit), Th	e numbe	er of ou	, tput add	iress bu	ises ca	n be se	lected (	12/16/2	0)	
	DRAM Controller							· ·						_				·						,	
	Clock Generation Circuit									4 circ	uits (Ma	in clock	, PLL, S	Sub clo	ck, On-c	hip osci	illator)								
	PLL												Y	es											
	Subclock												Y	es											
Clock	On-Chip Oscillator												Y	es											
	Oscillation Stop Detection												Y	es											
	Frequency Divider											1/r	n=1, 1	2, 4, 8.	16)										
	Power Save												Wait	/Stop											
Power Supply	Power-On Reset/POR												-												
Voltage Detection	Low Voltage Detection/LVD											Y	es (Lov	v voltag	e)										
	Resolution × Channels												10-bi	$t \times 26$											
A/D Converter	Sample and Hold												Y	es											
	Multi-Channel Sample and Hold												-												
D/A Converter	Resolution × Channels												8-bi	it×2											
	8-bit												-	-											
	16-bit											11	(Timer	A, Time	r B)										
	Input Capture												-	-											
	Output Compare												-	-											
Timer	PWM Output												5 (Tir	ner A)											
	Real-Time Port												-	_											
	Event Counter											11	(Timer	A, Time	rB)										
	2-Phase Encoder Input												3 (Tir	ner A)											
	3-Phase Inverter Control								1 (sha	red with	Timer	A4, Tim	er A1, 1	Fimer A	2, Timer	<sup>-</sup> B2, De	ad time	timer)							
Watchdog Timer														1											
	Clock Sync./ Clock Async.	<u> </u>											3 (U	ART)											
Serial Interface	Clock Sync. Only	<u> </u>											2 (5	SI/O)											
201	Clock Async. Only												-	_											
I C-bus													3 (U	ART)											
EBUS Emort Cord/EIM		——											3 (0.	ART)											
Smart Card/Silvi	Communication Unit/Crossial Corial I/O	——											2 (U												
Synchronous Senai	Chappele	——											3 (0	ANI) _											
CAN	Mossage Box (Numbers)																								
IrDA	Message Dox (Numbers)													_											
CBC Calculation	Circuit	<u> </u>									1 /	CRC-C		$X^{16} + X^{12}$	<sup>2</sup> + X <sup>5</sup> +	1))									
X/Y Converter	onom	<u> </u>									(	5110-0		-	тл †	•11									
san conventer	Input Only (Numbers)													1											
	CMOS I/O (Numbers)	R	5	111	R	5	111	<u>я</u>	5	111	\$	15	111	ء ا	15	111	R	5	111	R	15	111	R	5	111
I/O Ports	N-Channel Open Drain Port (Numbers)	⊢ °	-		. 0	-		. 0	-			-		2	-		0	-		0	-		. 0	-	
	High Current Drive Port													_											
	Pull-Up Resistor	8	5	111	8	5	111	8	5	111	6	15	111	6	15	111	8	5	111	8	15	111	8	5	111
External Interrup	ts Pins												1	1											
Debugging	On-Chip Debug								_									Yes			-			Yes	
Function	On-Board Flash Program								-									Yes			-			Yes	
Other	ROM Correction Function								Yes									-			Yes			-	
Functions	Others												3V, 5V i	interface	e										
Operating Freque	ency/Supply Voltage										24N	IHz/3.0	to 5.5V,	10MHz	z/2.7 to	5.5V									
Operating Ambie	ent Temperature (°C)											- 2	0 to 85,	, – 40 to	85										
		7			7											1		7	7				7	I T	
		∢	∢	∢	∢	∢	∢	⊲	∢	⊲	∢	⊲	∢	∢	∢	∢	∢	∢	∢	∢	∢	⊲	<	∢	∢
		ц	ų,	Ь Ф	ц	ų,	ų,	<u> </u>	ų,	μġ	ц Ц	μġ	ų,	l d	ų,	ų d	Ч	ų,	Ŕ	ц	ų R	ļ Ģ	ця,	ų,	Ą
Package*2		00	100	281	100	6	281	100	0	281	100	8	281	001	100	281	100	100	28	100	00	281	100	8	281
		P01	-01°	01	P01	010	-01°	P01	010	01	P01	01	-10c	P01	010	01	P01	-01	-01	P01	010	201	P01	01	-01
		ğ	, d	ğ	ğ	d d	Lo I	l ĝ	, a	b	1 2 2 2	b	LQ.	l ĝ	LQ.	ğ	ğ	ď	ğ	ğ	, a	ğ	ğ	ğ	LQ.
		Ē	립		Ē	립	Ē		Ē		ā		Ц	Ē	Ē	Ē	ā	Ц	d	ā	Ē		Ē	Ē	đ
		0	p.	0	0	p.	p.				6														
		XFF	XG	XG	XFF	XG	XG	ΎΕΡ	GF	GF	ΈΡ	GF	(GF	EP	(GF	GF				Ę	GP	GP			
		X	XX	X	XX	X	X	1 X	2	Ŷ	Ŷ	ĝ	Ŷ	ŝ	Ŷ	Ŷ	۵.	٩.	٩.	X	X	× ×	0	٩	۵.
Part No.		ΥP-	Å	۲P,	ΥP-	Ϋ́Ρ	Υb	<u> </u>	- Ļ	- 4		- Ļ	- F	<u> </u>	- đ	<u> </u>	ЪН	PG	PG	Ч- К-	A-	- H	PFF	PG	DG!
		TW	1 W	M	MS	MS	MV	MF	SMF	3MF	1 MF	1 MF	MF	MF	SMF	Ϋ́Υ	EH	HHS	H	ſWS	CMS	M	1FJI	1FJ	7FJI
		624	624	625	626	626	627	622	622	623	624	624	625	626	626	627	626	626	627	626	626	627	626	626	627
		130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130
		2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

opeen		0,00	, 36	163		00/	UZA	aru	up)											
Group										Ν	M16C/62	A								
	ROM (Bytes)		-	-			32K				64	1K					9	5K		
Momony	RAM (Bytes)	10	)K			3K				10K			4K			10K			5K	
wiemory	Data Flash			-							-		101							
	Program Security										-									
	CPU									М	16C/60 C	ore								
	Basic Instructions									60	91 5 (@16M	LI-7)								
CPU	Multiplier									1	.5 (@16ivi 6 × 16→3	12)								
	Multiply-Accumulate Instruction									16	× 16 + 32-	→32								
	Barrel Shifter										-									
DMA	DMAC (Channels)										2							-		
	DTC/DMACII Address Space (Bytes)			1	M			-	1	м		1	M		1	M	-	1	M	_
	Address opace (Dytes)								Support for	insertion of		Support for	insertion of		Sunnort for	insertion of	F	Support for	insertion of	
	External Bus Interface		Support	for inserti uts 4 chir	on of 1 wa	ait states, onals		-	1 wait state	es, Outputs	-	1 wait state	es, Outputs	-	1 wait stat	es, Outputs	-	1 wait state	es, Outputs	-
									4 chip-sel	ect signals		4 chip-sel	ect signals		4 chip-sel	ect signals		4 chip-sele	ect signals	
External Bus									Selecta Senarate b	ble from us Multiplex		Selecta Senarate hi	ble from us. Multinlex		Selecta Senarate b	ble from us Multinlex		Selectal Senarate hi	ble from us Multiplex	
Expansion		Select	able from	Separate	e bus, Mul	Itiplex bus	, Data		bus, Data B	us Width can		bus, Data Bi	us Width car		bus, Data B	us Width can	1	bus, Data Bu	us Width can	
	Bus Structure	Bus Wie	dth can b ut addres	e selecter ss buses r	d (8/16-bit an be sel	t), The nur lected (16	mber of /20)	-	be selecte	d (8/16-bit), er of output	-	be selected The number	d (8/16-bit), er of output	-	be selecte	d (8/16-bit), er of output	-	be selected The number	d (8/16-bit), er of outout	-
		outp		55 54303 (	211 00 30		(20)		address bu	ises can be		address bu	ises can be		address bu	uses can be		address bu	ises can be	
									selected	d (16/20)		selected	I (16/20)		selecte	d (16/20)		selected	1 (16/20)	
	DRAM Controller								2	oirquite (N	- Aain clock	Sub clor	(k)							
	PLL								2	circuito (r	-	., Oub clot	<i>xy</i>							
	Subclock										Yes									
Clock	On-Chip Oscillator										-									
	Oscillation Stop Detection									1/0 /	- 1 2 4	9 16)								
	Power Save									1/11 (1	Wait/Stor	o, 10)								
Power Supply	Power-On Reset/POR										-									
Voltage Detection	Low Voltage Detection/LVD										-									
	Resolution × Channels										10-bit × 10	0								
A/D Converter	Multi-Channel Sample and Hold	<u> </u>									res									
D/A Converter	Resolution × Channels										8-bit × 2									
	8-bit										-									
	16-bit									11 (T	imer A, Tii	mer B)				_				
	Output Capture																			
	PWM Output			5 (Tin	ner A)			3 (Timer A)	5 (Tir	ner A)	3 (Timer A)	5 (Tin	ner A)	3 (Timer A)	5 (Tir	ner A)	3 (Timer A)	5 (Tin	ner A)	3 (Timer A)
Timer	Real-Time Port										_									
	Event Counter	<u> </u>		0 (7				0.0T 1)	0.07	11 (T	imer A, Ti	mer B)		0.07	0.07	•	0 (T	0.77		0 (T
	2-Phase Encoder Input			3 (11	ner A)			2 (Timer A)	3 (11r	ner A)	2 (Timer A)	3 (Tin	her A)	2 (1 imer A)	3 (Tir	ith Timor M	2 (Timer A)	3 (Tin	ner A)	2 (Timer A)
	3-Phase Inverter Control	1 (s	hared wit	h Timer A	4, Timer /	A1, Timer	A2,	-	Timer A1, Tir	ner A2, Timer	_	Timer A1, Tir	ner A2, Time	·   _	Timer A1, Ti	mer A2, Timer	r —	Timer A1, Tin	ner A2, Timer	-
						mer)			B2, Dead	time timer)		B2, Dead	time timer)		B2, Dead	time timer)		B2, Dead	time timer)	
Watchdog Timer	Clask Supe / Clask Asupa			2 (11					2/11			2/11			2/11			2/11		
Serial Interface	Clock Sync. Only			3 (0)				12 (0AIII)	] 3(0	<u>(111)</u>	2 (SI/O)	3 (0/		[2 (0AIII)	3 (0	AIII)	[2 (0AIII)	3 (0/	<u>, , , , , , , , , , , , , , , , , , , </u>	2 (0/111)
	Clock Async. Only			-	-			1 (UART)	-	_	1 (UART)	-	-	1 (UART)	-	_	1 (UART)	-	_	1 (UART)
I <sup>2</sup> C-bus											1 (UART)									
IEBus											1 (UART)							-		
Synchronous Serial	Communication Unit/Special Serial I/O										- (UART)									
CAN	Channels										-									
CAN	Message Box (Numbers)										-									
IrDA CBC Coloulation	Circuit								1.0		- TT (V <sup>16</sup> .	V12 . V5 .	1))							
X/Y Converter	Olicuit								1 (0	0110-001	<u> </u>	<u> </u>	• • • • • •							
	Input Only (Numbers)										1									
	CMOS I/O (Numbers)		5	0		8	5	68	8	5	68	8	5	68	8	15	68	8	5	68
I/O Ports	N-Channel Open Drain Port (Numbers)										2									
	Pull-Up Resistor	<u> </u>	5	0		8	5	68	6	15	68	8	5	68	6	15	68	8	5	68
External Interrup	its Pins			- 1	1		-	8	1	1	8	1	1	8	1	1	8	1	1	8
Debugging	On-Chip Debug							<u></u>			_									
Function	On-Board Flash Program																			
Functions	Others										-									
Operating Freque	ency/Supply Voltage								16MHz/4	.2 to 5.5\	, 10MHz (	1 wait) /2	.7 to 5.5	/						
Operating Ambie	ent Temperature (°C)					,,				- 20 1	to 85, – 40	) to 85								
		8-A	8-A	8-A	8-A	8-A	8-A	Y-N	A-8	B-A	₹-	A-8	A-8	Y-	A-8	8-A	A-F	8-A	8-A	A-A
Package*2		DOJE	- No	DOJE	OKE	DOJE	OKE	108	DOJE	N N	108	DOJE	OKE	108	DOJE	- X	7CO8	DOJE	- No	7FOE
0		010	010	010	010	2010	010	000	010	010	000	010	010	000	2010	010	300	010	010	000
		RQF	ГĞ	ğ	Гаг	Вġ	Ľ	l ig	l ä	LG	R I	l ig	ğ	RGF	R I	ГĞ	1 2 2 1	BG	ГĞ	1 2 2 1
		_ ₽_		_ ₽_	₽.	_ ₽_	۵.	_ ₽	_ ₽_	_ ₽_	_ ₽_	_ ₽_	_ ₽_	_ ₽				₽.		
						٩	6	<u>L</u>	٩	L.	L.	e.	<u>ط</u>	L.	٩	d.	d.	<u>e</u>	6	<u>L</u>
						XXF	DXX	XXG	XXF	XXG	DXX	XXF	XXG	XXG	XXF	XX	XX	XXF	XX	XX
Part No.		£	Ъ	£	GР	A-X	A-X	A-X	A-X	A-X	A-X	A-X	A-X	A-X	X-A	A-X	A-X	A-X	A-X	X-A
		OSA	OSA	2SA	2SA	2M4	2M4	3M4	MO	OM8	1M8	2M8	2M8	3M8	-WO	OMP	1MP	2MP	2MP	3MP
		062	062	062	062	062	062	062	062	062	062	062	062	062	062	062	062	062	062	062
		ВМ	МЗ	M3	M3	ЩЗ	MЗ	μ M3	Ξ Ξ	M3	M3	Ш Ш	ШЗ	W3	M3	M3	Ξ M3	МЗ	β	Ψ

### • Specifications (M16C/60 Series : M16C/62A Group)

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/60 Series : M16C/62A Group)

Group	· · · · · ·							·	M16C/62A							
	BOM (Bytes)					128K							256	SK		
	RAM (Bytes)			10	K				5K				20	K		
	ROM Type*1	F	F	M		F		N	Λ		F		N		F	М
Memory	Data Flash						1		_							
	Program Security	Yes (IE Check F ROM Protect F	Code unction, Code unction)	-		Yes (ID Code Check Function, ROM Code Protect Function)		-	-		Yes (ID Check F ROM Protect F	Code unction, Code unction)	_		Yes (ID Code Check Function, ROM Code Protect Function)	_
	CPU							M	116C/60 Cor	e						
	Basic Instructions								91							
CPU	Minimum Instruction Execution Time (ns)							62	2.5 (@16MH	z)						
	Multiplier								16×16→32							
	Multiply-Accumulate Instruction							16	× 16 + 32→	32						
	DMAC (Channels)								2							
DMA	DTC/DMACII								_							
	Address Space (Bytes)		1	М		-	-	11	М	-		1	М		-	-
	External Bus Interface	Suppo Ot	ort for inserti utputs 4 chip	on of 1 wait s o-select signa	states, Ils	-	_	Support for 1 wait state 4 chip-sele	insertion of es, Outputs ect signals	-	Suppor Ou	t for insertitiputs 4 chip	on of 1 waits -select signa	states, Ils	-	-
External Bus Expansion	Bus Structure	Selectable Data Bus The numb	e from Sepa Width can er of output selected	rate bus, Mult be selected ( address bus d (16/20)	tiplex bus, 8/16-bit), es can be	-	_	Selectable from Multiplex bus, E can be select The number of buses can be s	n Separate bus, Data Bus Width ted (8/16-bit), output address elected (16/20)	_	Selectable Data Bus The numbe	from Separ Width can I er of output selected	rate bus, Multo be selected ( address bus i (16/20)	tiplex bus, 8/16-bit), es can be	_	-
	DRAM Controller								-							
	Clock Generation Circuit							2 circuits (	wain clock,	Sub clock)						
	Subclock								Yes							
Clock	On-Chip Oscillator															
	Oscillation Stop Detection								-							
	Frequency Divider							1/n (	n=1, 2, 4, 8	16)						
	Power Save		1/n (n=1, 2, 4, 8, 16) Wait/Stop													
Power Supply	Power-On Reset/POR								-							
vollage Delection	Low Voltage Detection/LVD								-							
A/D Converter	Sample and Hold															
D/A Converter	Resolution × Channels		Yes — 8-bit × 2													
	8-bit		8-bit × 2													
	16-bit							11 (T	imer A, Tim	er B)						
	Input Capture								-							
	Output Compare		- (31)													
Timer	PWM Output		5 (Tir	ner A)		3 (Tir	mer A)	5 (Tim	ner A)	3 (Timer A)		5 (Tin	ner A)		3 (Tim	ner A)
limer	Real-Time Port							11/7	-	or P)						
	2-Phase Encoder Input		3 (Tir	mer A)		2 (Tir	mer A)	3 (Tim	Inner A, Tim	2 (Timer A)		3 (Tin	ner A)		2 (Tim	ner A)
			0(11	10171		2 (		1 (shared wi	th Timer 44	2 (11110174)		0(11	10171)		2 (	101 7 19
	3-Phase Inverter Control	1 (shared )	with Timer A	4, Timer A1,	Timer A2,		_	Timer A1,	Timer A2,	-	1 (shared v	ith Timer A	4, Timer A1,	Timer A2,	-	-
			IIIEI DZ, DE	au ume ume	1)			Timer B2, Dea	ad time timer)			nei bz, De	au une une	1)		
Watchdog Timer									1							
Carial Interface	Clock Sync./ Clock Async.		3 (U	ART)		2 (U	ART)	3 (UA	ART)	2 (UART)		3 (U	ART)		2 (UA	ART)
Senai Interiace	Clock Sync. Only					1 (1)			2 (51/0)						1 (1)/	
I <sup>2</sup> C-bus	Clock Asyric. Only					1 (0	AIII)		1 (LIABT)	I (UAIII)					1 (07	NII)
IEBus									1 (UART)							
Smart Card/SIM									1 (UART)							
Synchronous Serial	Communication Unit/Special Serial I/O								-							
CAN	Channels								_							
	Message Box (Numbers)								_							
CBC Calculation	Circuit							1 (CPC		12 _ V <sup>5</sup> · · · · ·						
X/Y Converter	- on out							. 10110-00		- + A + I))						
	Input Only (Numbers)								1							
	CMOS I/O (Numbers)		8	35	_	6	68	8	5	68		8	5	_	6	8
I/O Ports	N-Channel Open Drain Port (Numbers)								2							
	High Current Drive Port					-	20	-	-				-		-	
External Interrup	ruii-up resistor			1		6	90 8	8	ວ 1	800		8	ວ 1		6	<u> </u>
Debugging	On-Chip Debua	Y	es	-		Yes	Ĭ	<u> </u>	-	5	Ye	s	–		Yes	
Function	On-Board Flash Program	Ye	es	- 1		Yes		_	_		Ye	s	-		Yes	-
Other	ROM Correction Function			Ye	s	_		Ye	es				Ye	s		Yes
Functions	Others															
Operating Freque	ency/Supply Voltage						16M	Hz/4.2 to 5.5	V, 10MHz (1	wait) /2.7 to	5.5V					
Operating Ambie	ent Temperature (°C)		1	, I		1		- 20	to 85, – 40	10 85						
		B-A	B-A	B-A	B-A		A-A	B-A	B-A	A-A	B-A	B-A	A-B	B-A	0-0	¢
Package*2		Foo	Noc Noc	Foo	NOK NOK		F08	Foo	NOK XOK	F08	Foo	NOK NOK	Foo	NOC XOC		
		0	010	-0-	010			01	010	00-	0	010	-01	010		5
		la la	LOP	l ag	LOP		ğ	RGF	LOP	BQF	ğ	LOP	l la	LQF		2
		Ē	<u> </u>	ă.	Ц	6	<u> </u>	L L	ц	ä	ä	Ц	ä	Ц	4	
				0	۹.		۵.	0	٩.	٩.			0	٩.		۹.
				XFF	XGI		XGF	XFF	XGF	XGF			XFF	XG		XG
		<u>0</u> .	<u>д</u>	XX-	XX-	<u>с</u>	X-	XX-	XX-	XX-	C.	<u>C</u>	XX-	XX-	<u>с</u>	XX-
Part No.		CAF	CAC	ICA	ICA	CAC	ICA	1CA	ICA.	ICA	GAI	GAC	IGA	IGA	GA	IGA
		20F	20F	20N	20N	21F	21N	22M	22N	23N	24F	24F	24N	24N	25F	25N
			60	9	90	90	00	90	90	90	90	90	90	90	90	90
		306	8	8	0	õ	0	l õ	ĕ	0	ē I	3	- m	ы Э	l m	ĕ

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/60 Series : M16C/62M Group)

Group	· · ·						M16C	C/62M					
	ROM (Bytes)			12	зк					25	6K		
	RAM (Bytes)			10	K					20	Ж		
	ROM Type*1	F		N	1	F	М	F	-	١	Λ	F	М
Memory	Data Flash						-						
moniory		Yes (ID	Code			Yes (ID Code		Yes (IE	O Code			Yes (ID Code	
	Program Security	Check Fu	inction,	-	-	Check Function,	_	Check F	unction,	-	_	Check Function,	_
		ROM C	Jode (notion)			HOM Code Protect		ROM Protect F	Code Function)			HOM Code Protect	
	0011	1101000110				T directority		11010011	unedony			T diffedority	
	CPU Regia Instructions						M16C/6	50 Core					
	Minimum Instruction Execution Time (no)						100 (@)	10141-					
CPU	Multiplior						16 \ 1	6					
	Multiply-Accumulate Instruction						16 × 16 ±	+ 32-32					
	Barrel Shifter							-					
	DMAC (Channels)						2	2					
DMA	DTC/DMACII						-	_					
	Address Space (Bytes)		1	M		-	-		1	М		-	_
	External Bus Interface	Support for inser	tion of 1 wait sta	ites, Outputs 4 chip	-select signals	-	-	Support for ins	ertion of 1 wait sta	tes, Outputs 4 chi	p-select signals	-	_
External Bus		Selectable	from Separate	e bus, Multiplex	bus, Data			Selectable	from Separate	bus, Multiplex	bus, Data		
Expansion	Bus Structure	Bus Width ca	an be selecte	d (8/16-bit), The	number of	-	-	Bus Width	can be selected	l (8/16-bit), The	e number of		-
		output ad	dress buses	can be selected	(16/20)			output a	ddress buses o	can be selected	1 (16/20)		
	DRAM Controller							-					
	Clock Generation Circuit					2	circuits (Main o	clock, Sub clocl	<)				
	PLL							-					
Clock	Op-Chip Oscillator						YE	-					
CIUCK	Oscillation Stop Detection							_					
	Frequency Divider	1/n (n=1, 2, 4, 8, 16)											
	Power Save	1/n (n=1, 2, 4, 8, 16) Wait/Stop											
Power Supply	Power-On Reset/POR												
Voltage Detection	Low Voltage Detection/LVD												
	Resolution × Channels						10-bit	t × 10					
A/D Converter	Sample and Hold						Ye	es					
	Multi-Channel Sample and Hold		Yes										
D/A Converter	Resolution × Channels						8-bit	t×2					
	8-bit							-					
	16-DIT						11 (Timer /	A, Timer B)					
	Output Compare												
	PWM Output		5 (Tir	ner A)		3 (Tin	ner A)		5 (Tin	ner A)		3 (Tin	ner A)
Timer	Beal-Time Port		0(11	10174		0(	-	_		10171		0(11	
	Event Counter						11 (Timer A	A, Timer B)					
	2-Phase Encoder Input		3 (Tir	ner A)		2 (Tin	ner A)		3 (Tin	ner A)		2 (Tin	ner A)
	2 Phase Inverter Central	1 (shared	d with Timer A	4, Timer A1, Tir	mer A2,		_	1 (share	ed with Timer A	4, Timer A1, Ti	mer A2,		_
	3-Filase inverter Control		Timer B2, De	ad time timer)				-	Timer B2, De	ad time timer)			
Watchdog Timer							1	1					
	Clock Sync./ Clock Async.		3 (U	ART)		2 (U/	ART)		3 (U/	ART)		2 (U	ART)
Serial Interface	Clock Sync. Only						2 (S	si/O)					
120 hun	CIOCK ASYNC. ONIY			_		1 (0/	ARI) 1 (11)					1 (0/	ARI)
I C-bus							1 (U/						
Smart Card/SIM							1 (U)	ART)					
Synchronous Serial	Communication Unit/Special Serial I/O						. (6,	_					
	Channels						_	_					
CAN	Message Box (Numbers)						-	_					
IrDA							_	_					
CRC Calculation	Circuit					1 (	CRC-CCITT (X	$X^{16} + X^{12} + X^5 +$	1))				
X/Y Converter	1							_					
	Input Only (Numbers)					-	1	1					-
	CMOS I/O (Numbers)		8	15		6	8			5		6	8
I/O Ports	N-Channel Open Drain Port (Numbers)						2	2					
	Righ Current Drive Port			5		6	•			5		6	0
External Interrun	Tuil-Op nesision		1	1		6	0		0	1		6	3
Dobugging	On-Chin Debug	Yes		-	-	Yes	_	Ye	200	-	_	Yes	_
Function	On-Board Flash Program	Yes	\$	-	-	Yes	-	Ye	25	-	_	Yes	-
Other	ROM Correction Function	-		Ye	s	-	Yes	-	-	Ye	es	-	Yes
Functions	Others						-	_					
Operating Freque	ency/Supply Voltage	10MHz/2.7 to 3.6V, 7MHz/2.4 to 3.6V, 7MHz (1 wait) /2.2 to 3.6V								6V			
Operating Ambie	ent Temperature (°C)	– 20 to 85, – 40 to 85									,		
		Ą	4	Ą.	4	<	¢	4	Ą.	Ą	Ą		۲.
<b>D</b>		BA I	Ř	SUB NB	Å			NB	Β. Ω	NB	Ê.		Ϋ́ΥΫ́Υ
Раскаде**		100	100	100	100		5	100	100	100	100		
		PAC 1	ЪО	Ъ	Ъ	0		Ъ	ЪО	Ъ	PO		
		PRG PRG					É	В	LC	В	5		Ĕ
		- u		<u>ш</u>	<u>u</u>		-	<u>ц</u>	<u></u>	ш.	<u>ц</u>		-
				<u>A</u>	<u>د</u>		<u>د</u>			<u>p</u>	<u>C</u>		<u>C</u>
				XX X	X		XXX			XXF	×		X
		4FP	4GP	X-1		1GP		L P	1G P	У-V	л- X.	1GP	1-X
Part No.		C N	NO.	ACN ACN	ACM	≥ O	ACN	N S S	ND:	NGN	AGN	N S S	AGN
		20F	20F	200	20M	21F	21k	24F	24F	24N	24N	25F	25N
		8	90	306	306	306	306	306	306	306	306	306	306
		e e	0										

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/60 Series : M16C/62N Group)

Group	· · · · ·										M160	C/62N									
	BOM (Bytes)	64	ĸ	1		_	128K									256K	-		-		
	RAM (Bytes)	8K	(				10K					12K				LOUIT	20	ЭK			
	ROM Type*1		I	F			М		F		Ν	1			F			М		F	М
Memory	Program Security	Yes (ID ROM C	) Code ( Code Pr	Check Fu otect Fur	nction, action)		_		Yes (ID Code Check Function, ROM Code Protect Function)			-		Ye Che Prot	s (ID Co ck Funct OM Cod ect Func	de tion, le tion)		_		Yes (ID Code Check Function, ROM Code Protect Function)	_
	CPU Basic Instructions	100 (@1	01411-)						· · · · · · · · · · · · · · · · · · ·		M16C/6 9	0 Core		I		· · · · · · · · · · · · · · · · · · ·				II	
CPU	Minimum Instruction Execution Time (ns) Multiplier	100 (@1	UMHZ)								16×1	62.5 (@ 6→32	16MHZ)								
	Multiply-Accumulate Instruction										16 × 16 -	+ 32→32									
	Barrel Shifter										-	-									
DMA	DTC/DMACII										-	-									
	Address Space (Bytes)				1M				-	-					1M						·
External Bus	External Bus Interface	Support for in 1 wait states 4 chip-selec	nsertion of s, Outputs ct signals	Support 4 chip- by a	for insert select sig ddress sp	tion of 1 w Inals, Avai pace expa	ait states, lable to 4N insion func	Outputs / bytes ction	-	-	Su	pport for Availab	insertion le to 4M	n of 1 wai bytes by a	t states, ( address :	Outputs 4 space ex	1 chip-sel pansion f	ect signation	ils,	-	
Expansion	Bus Structure	S The numb	Selectab Data Bu ber of or	le from S us Width utput add	eparate can be s lress bus	bus, Multi elected (8 ses can be	iplex bus, 8/16-bit), e selected	(16/20)	-	-		The num	Selectab Data Bu ober of o	le from S us Width o utput add	eparate t can be se ress buse	ous, Multi elected (8 es can be	iplex bus, 8/16-bit), e selecter	d (16/20)		-	
	Clock Generation Circuit									2 circui	ts (Main o	- clock, Sul	b clock)								
	PLL										-	-	,								
Clock	Subclock		Yes 																		
CIUCK	Oscillation Stop Detection		- - 1/n (n=1, 2, 4, 8, 16)																		
	Frequency Divider		– 1/n (n=1, 2, 4, 8, 16) Wait/Stop																		
D	Power Save		1/n (n=1, 2, 4, 8, 16) Wait/Stop —																		
Power Supply Voltage Detection	Low Voltage Detection/LVD		Wait/Stop — —																		
	Resolution × Channels	10-bit																			
A/D Converter	Sample and Hold										Ye	es									
D/A Converter	Multi-Channel Sample and Hold Resolution × Channels		10-bit × 10 10-bit × 18 Yes - 8-bit × 2																		
	8-bit										-	-									
	16-bit									1	1 (Timer )	A, Timer I	B)								
	Output Capture											-									
Timer	PWM Output			5	(Timer )	A)			3 (Tin	ner A)				5	(Timer A	A)				3 (Tim	er A)
	Real-Time Port										-	-	2)								
	2-Phase Encoder Input			3	(Timer	A)			2 (Tin	1 ner A)	1 (Timer )	A, Timer I	В)	3	(Timer A	A)				2 (Tim	er A)
	3-Phase Inverter Control	1 (shared	with Time	r A4, Timer	A1, Timer	A2, Timer B	32, Dead tim	ne timer)	-	- /	1 (sha	ared with	Timer A	4, Timer A	1, Timer	A2, Time	er B2, De	ead time	timer)	<u> </u>	·
Watchdog Timer	Clask Syna / Clask Asyna				2 /114 DT	7			2/14											2/11	
Serial Interface	Clock Sync. Only				3 (UANI	)			2 (0)	4ni)	2 (S	I/O)			S (UART)	)				2 (04	
	Clock Async. Only				-				1 (U/	ART)					-					1 (UA	NRT)
I <sup>2</sup> C-bus											1 (U)	ART)									
Smart Card/SIM											1 (U/	ART)									
Synchronous Serial	Communication Unit/Special Serial I/O										-	-									
CAN	Channels Message Box (Numbers)											-									
IrDA	moodage Box (Hamberd)										-	-									
CRC Calculation	Circuit									1 (CRC-	CCITT ()	$(^{16} + X^{12} + )$	- X <sup>5</sup> + 1))								
X/Y Converter	Input Only (Numbers)											-									
	CMOS I/O (Numbers)				85				6	8					85					68	3
I/O Ports	N-Channel Open Drain Port (Numbers)										2	2									
	Pull-Up Resistor				85				6	8	-				85					68	3
External Interrup	its Pins				11				8	3					11					8	
Debugging	On-Chip Debug		Y	es es			_		Yes			-			Yes					Yes Vac	
Other	ROM Correction Function		-	-		-	Yes		-		Ye	es			-			Yes		-	Yes
Functions	Others								/		-	-								· · · ·	
Operating Freque	ency/Supply Voltage	10Mi 2.7 to 3	Hz/ 3.6V	16M 3.0 to 7M	/IHz/ 0 3.6V, IHz/	16Mi 7MF	Hz/3.0 to 3	3.6V, .6V,	16MHz/ 3.0 to 3.6V, 7MHz/	78.01	16MHz/3. 7MHz/2.4	0 to 3.6V 4 to 3.6V,	, 2 6\/	16MF 7MH	Iz/3.0 to	3.6V, 3.6V	16MI 7MH	Hz/3.0 to	3.6V, 3.6V,	16MHz/ 3.0 to 3.6V, 7MHz/	16MHz/ 3.0 to 3.6V, 7MHz/ 2.4 to 3.6V, 7MLI-
		2.7 to 3.6V         7MHz/ 2.4 to 3.6V         7MHz/ 7MHz / 2.4 to 3.6V         7MHz/ 7MHz (1 wait)/2.2 to 3.6V         7MHz/ 2.4 to 3.6V         7MHz/ 7MHz (1 wait)/2.2 to 3.6V							, / C. C 10 0	v				/ IVIFIZ (1	wditj /2.	∠ i∪ J.0V	2.4 to 3.6V	(1 wait)/			
Operating Ambie	ent Temperature (°C)									_	20 to 85	– 40 to 8	35								∠.∠ 10 3.6V
Package*2		100JB-A	00KB-A	100JB-A	00KB-A	100JB-A	00KB-A	I00LB-A	V VI 081		100JB-A	00KB-A	I00LB-A	100JB-A	00KB-A	I00LB-A	100JB-A	00KB-A	IO0LB-A	BO IA-A	
		2P01	RaP01 RaP01 RaP01 LaP01 TaP01					2P01		5	2P01	2P01	2P01	2P01	2P01	2P01	2P01	2P01	2P01		5 F
		РВС	PLC	PRC	PLG	PRC	LC	PTC		É	PRC	PLC	PTC	РВС	PLC	PTC	PRC	PLC	PTC	L L L L L L L L L L L L L L L L L L L	
						۵.	<u>_</u>	<u>a</u> .		<u>e</u>	۹.	d.	Ē.				٩.	<u>م</u>	<u>م</u>		<u>C</u>
			۵.	۵.	<u>a</u>	XXXF	DXXX	ХХХН	۹.	XXXG	XXXF	DXXX	XXXH	۵.	<u>a</u> _	٩	XXXF	DXXX	XXXH	<u>م</u>	DXXX
Part No.		F8NF	FBNG	CNF	CNG	VCN-)	VCN-	ACN-	CNG	ACN-)	NGN	AGN	AGN	GNF	GNG	GNH	NGN	AGN-	AGN-	GNG	AGN-
		62GF	62GF	1620F	1620F	620N	620N	)620N	)621F	)621 N	622N	622N	1622 N	)624F	)624F	)624F	624N	1624N	1624N	)625F	625A
		M3C	M3C	M3C	M3C	M3C	M3C	M3C	МЗС	M3C	M3C	M3C	M3C	МЗС	M3C	M3C	M3C	M3C	M3C	M3C	M3C

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QZROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code  $\star$ : New product  $\star\star$ : Under development

opeen		0/00 001			oup)					
Group				M160	C/6N4				M16C/6N5	
	ROM (Bytes)	128K	128K	( + 4K	256K	256K	(+ 4K	128K	128K	+ 4K
	BAM (Bytes)		5K			10K			5K	
Memory	BOM Type*1	м		F	М		F	м		
	Data Elash	-	Yes	(4K)	-	Yes	(4K)	-	Yes	(4K)
	Program Security	-	Yes (ID Code Check Function	. ROM Code Protect Function)	-	Yes (ID Code Check Function	ROM Code Protect Function)	_	Yes (ID Code Check Function	ROM Code Protect Function)
	CPU			, nom ocus nelser runsleng		M16C/60 Core	, nom ooder release running			, nom odder releast runslash
	Basic Instructions					91				
	Minimum Instruction Execution Time (ns)					41.7 (@24MHz)				
CPU	Multiplier					16, 16, 2410112)				
	Multiply Assumulate Instruction					16 × 16 + 22 × 22				
	Rerrel Shifter					10 × 10 + 32-32				
	Barrel Shiller									
DMA	DMAC (Channels)					2				
	DTC/DMACII					-				
	Address Space (Bytes)			0		1M				
External Bus	External Bus Interface	0.1		Supp	ort for insertion of 1	to 3 wait states, Ou	tputs 4 chip-select s	ignais		(4.0.(0.0))
Expansion	Bus Structure	Select	table from Separate	bus, multiplex bus, L	Data Bus Width can	be selected (8/16-bi	t), The number of ou	tput address buses	can be selected (12	/16/20)
	DRAM Controller									
	Clock Generation Circuit				4 circuits (Main cl	ock, PLL, Sub clock,	On-chip oscillator)			
	PLL					Yes				
	Subclock					Yes				
Clock	On-Chip Oscillator					Yes				
	Oscillation Stop Detection					Yes				
	Frequency Divider					1/n (n=1, 2, 4, 8, 16	)			
	Power Save					Wait/Stop				
Power Supply	Power-On Reset/POR					-				
Voltage Detection	Low Voltage Detection/LVD					-				
	Resolution × Channels									
A/D Converter	Sample and Hold									
	Multi-Channel Sample and Hold									
D/A Converter	Resolution × Channels									
	8-bit									
	16-bit				3)					
	Input Capture					_	<i>'</i>			
	Output Compare					_				
Timor	BWM Output					E (Timor A)				
TITLET	P www.Output					5 (TIMELA)				
	Event Counter					11 /Timor A Timor F	2)			
	2 Phase Encoder Input					2 (Timor A)	2)			
	2-Phase Encoder Input			4 ( 1 -		3 (Timer A)		. P		
147-1-1-1	3-Phase Inverter Control			i (sna	red with Timer A4, I	imer AI, Timer AZ,	Imer 62, Dead um	e umer)		
watchdog Timei	r Let te te te					1				
	Clock Sync./ Clock Async.					3 (UART)				
Serial Interface	Clock Sync. Only					1 (SI/O)				
	Clock Async. Only					-				
I <sup>c</sup> C-bus						3 (UART)				
IEBus						3 (UART)				
Smart Card/SIM	1					1 (UART)				
Synchronous Seria	I Communication Unit/Special Serial I/O					3 (UART)				
CAN	Channels				2				1	
	Message Box (Numbers)			16	+ 16				16	
IrDA						-				
CRC Calculation	n Circuit				1 (CRC	-CCITT (X <sup>16</sup> + X <sup>12</sup> +	X <sup>5</sup> + 1))			
X/Y Converter						-				
	Input Only (Numbers)					1				
	CMOS I/O (Numbers)					85				
I/O Ports	N-Channel Open Drain Port (Numbers)					2				
	High Current Drive Port					-				
	Pull-Up Resistor					85				
External Interru	pts Pins					11				
Debugaina	On-Chip Debug	-	Y	es	-	Y	es	-	Ye	es
Function	On-Board Flash Program	-	Y	es	-	Y	es	-	Ye	es
Other	ROM Correction Function	Yes	1 .	_	Yes	-	_	Yes	-	_
Functions	Others					-				
Operating Frequ	ency/Supply Voltage					24MHz/3.0 to 5.5V				
Operating Ambi	ent Temperature (°C)					- 40 to 85				
oporating / initia				1		10 10 00				
		×-	A -		₹	₹		₹ 1	₹	₹
<b>D</b>		NB-1 JJB-1 JJB-1				9	2	I BC	뜆	
Раскаде**		0100					2	1 <u>5</u>	6	
		aP01 aP01 aP01				B			6	0 L
		PRO PRO PRO				Q.	Č	Z	Q.	Ē
							ū	L	<u> </u>	ā
		d o			E C			d C		
								X		
Part No						£	G D	8	£	GР
Fart NO.	N N N N N N N N N N N N N N N N N N N				5 5	Ğ	N N N	D L	Ŭ.	
A 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4				¥	¥	NS	NS	NS		
		306	306	306	306	306	306	306	306	306
							ž	ž	ž	ž

### • Specifications (M16C/60 Series : M16C/6N Group)

\*' F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/60 Series : M16C/6N Group)

Monte         Picture         Picture <th< th=""><th>0</th><th>(</th><th></th><th></th><th></th><th></th><th></th><th>Mile</th><th></th><th></th><th></th><th>hite</th><th></th><th></th><th></th><th>Mice</th><th></th><th></th></th<>	0	(						Mile				hite				Mice		
PROM           PROM         PR	Group			M160	5/6NK			M160	5/6NL			M160	5/6NM			M160	76NN	
Image:		ROM (Bytes)	192K	256K	384K + 4K	512K + 4K	192K	256K	384K + 4K	512K + 4K	192K	256K	384K + 4K	512K + 4K	192K	256K	384K + 4K	512K + 4K
Nervice         Tate Task         Image         Image <thimage< th="">         Image         Image</thimage<>		RAM (Bytes)		20K	31			201	3		105	20K	3		105	201	3	
Image         Part III Control Role Control         Part IIII Control Role Control         Part IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Memory	Data Elash	-	-	Yes	(4K)	-	-	Yes	(4K)		-	Yes	(4K)		-	Yes	(4K)
Product Politic State	moniory	Baarraon		-	Ves (ID Co	de Check			Ves (ID C	ode Check			Ves (ID C	nde Check			Ves (ID C	ode Check
Processor         Processor <t< td=""><td></td><td>Program Security</td><td>-</td><td>-</td><td>Function, F</td><td>ROM Code</td><td>-</td><td>-</td><td>Function,</td><td>ROM Code</td><td></td><td>_</td><td>Function, I</td><td>ROM Code</td><td></td><td>-</td><td>Function,</td><td>ROM Code</td></t<>		Program Security	-	-	Function, F	ROM Code	-	-	Function,	ROM Code		_	Function, I	ROM Code		-	Function,	ROM Code
Base headpoint         Image: Second Seco		CPU			11010011	unouony			1101000	M16C/6	50 Core		11010011	unotiony	I		11010011	
opp:         Main: Hands Route Ro		Basic Instructions								g	1							
Margine biologic mean         Margine (19, 16, 16-32)           DMA         Open Space Sp	CPU	Minimum Instruction Execution Time (ns)								41.7 (@	24MHz)							
Nome marked in the second is a		Multiplier								16×1	6→32							
OMAC (Channel) Addres Speec (Mel)         Image: Speec (Mel) <thimage: (mel)<="" speec="" th="">         Image: Speec (Mel)</thimage:>		Barrel Shifter								10 × 10 ·	+ 32→32 -							
Data         Processor         Pr	DMA	DMAC (Channels)									2							
Accord         Base of the set of sequel	DIVIA	DTC/DMACII								-	-			-				
Linking Difference         Difference <thdifference< th="">         Difference         <thd< td=""><td></td><td>Address Space (Bytes)</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td>M</td><td>auta di alala</td><td></td><td>-1-</td><td></td><td></td><td></td><td></td></thd<></thdifference<>		Address Space (Bytes)								1	M	auta di alala		-1-				
DRAW Control         Description of a product of a	External Bus Expansion	Bus Structure		Selectab	le from Sena	arate bus. N	Jultiplex bu	upport for i	s Width car	he selecte	d (8/16-bit)	The numb	er of output	t address b	uses can b	e selected (	12/16/20)	
Cock Generation Circuit         4 creater Man Book, PL, Sub Ock, On-the pacified in the set of the s	1	DRAM Controller		oolootab	io nom oopt	arato buo, r	nanapion be	o, Data Da	o main da	-	-	, 1110 114114	or or output	t dddrood b		00.00.00	12/10/20/	
PL     Image: Plane in the second seco		Clock Generation Circuit						4 circ	uits (Main c	lock, PLL, S	Sub clock, (	On-chip os	cillator)					
Subcivie         Subcivie         Non- training         Subcivie		PLL								Y	es							
Oxed as a bis of the constraint of the cons	Clask	Subclock								Y	es							
Procearby Prove Size         <	CIOCK	Oscillation Stop Detection		Yes														
Two websings in the series of		Frequency Divider		1/n (n=1, 2, 4, 8, 16)														
Processory Networks DescriptionProcessory Processory Processory Processory Processory Processory Processory Processory Processory Processory Processory Processory Processory Processory Processory Processory Processory Processory 		Power Save		Wait/Stop														
Withing Minding Marked Mode	Power Supply	Power-On Reset/POR		Wait/Stop														
AD Converter         Bissultant is backgrine         In URL 28           DiA Converter         Reportant is ball         840	Voltage Detection	Low Voltage Detection/LVD								10 1-	-							
Mile:Charges Sample and Hold	A/D Converter	Sample and Hold								10-DI	1 × 20							
DA Conventer         Readular Channels	TTD Contentor	Multi-Channel Sample and Hold		Yes														
Bolt	D/A Converter	Resolution × Channels																
If eldit         If (Imper A, Timer B)           Timer         If (Imper C, Timer A)		8-bit								-	_							
Implicit applicit         -           Timer         -           PMM Output         5 (Timer A)           Basil Time Pot 1         -           Event Control         3 (Timer A)           3 Phase Inverter Control         1 (Inmer A)           3 Phase Inverter Control         3 (Timer A)           3 Phase Inverter Control         3 (Timer A)           Seriel Interfect         3 (UART)           Clock Sync. Only         2 (SI/O)           Clock Sync. Only         -           Seriel Interfector         3 (UART)           EBus         3 (UART)           Seriel Commutation UnitSpecial Seriel I/O         -           CAN         Channels         2           CAN         Channels         1           CAN         Channels <td></td> <td>16-bit</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>11 (Timer</td> <td>A, Timer B) -</td> <td></td> <td></td> <td>-</td> <td></td> <td></td> <td>-</td> <td></td>		16-bit								11 (Timer	A, Timer B) -			-			-	
Time         PVML Output         5 (Timer A)           Real-Time Prot         -         -           Even Counter         3 (Timer A)         3 (Timer A)           3-Phase Encoder Input         3 (Timer A)         3 (Timer A)           3-Phase Encoder Input         3 (Timer A)         3 (Timer A)           3-Phase Encoder Input         3 (Timer A)         3 (Timer A)           3-Phase Encoder Input         3 (UART)         3 (UART)           Simant CaurdSout Input Special Small V         3 (UART)         3 (UART)           Else         3 (UART)         3 (UART)           Synet Cook Asyne: Only         2 (SI/O)         1 (UART)           Synet Cook Special Informacion UnitSpecial Small V         3 (UART)         3 (UART)           Synet Cook Special Informacion UnitSpecial Small V         3 (UART)         1 (UART)           Synet Cook Special V         3 (UART)         1 (UART)           Synet Cook Special Informacion UnitSpecial Small V         1 (UART)         1 (UART)           Synet Cook Special V         1 (UART)         1 (UART) <td></td> <td>Output Capture</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>-</td> <td>_</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>		Output Capture								-	_							
Real-Time Part	Timer	PWM Output								5 (Tir	ner A)							
Event Counter         11 (Timer A) Timer B)           2-Phase Encode riput         3-Phase Involve Control           3-Phase Involve Control         3-Phase Involve B2, Dead time timer)           Matchold Timer A)         Timer A)         Timer A)           Senal Interface         Clock Sync. Ohy         3 (UART)           Cook Sync. Ohy         2         3 (UART)           EBus         3 (UART)           Senar Card/SM         3 (UART)           Senar Card/SM         3 (UART)           Senar Card/SM         2         1         4 (SIO)           Fight Conspan="2">Cols Sync. Ohy         2         3 (UART)           Senar Card/SM         2         1         2           Genards         2         1           CAN         Message Box (Nimbers)         1         1           CAC         1         2           Ind CON (Nimbers)         2         1           CAC         1         2           Ind CON (Nimbers)         2		Real-Time Port								-	-							
2-Phase bencoder input         3 (1mer A)           Watching Timer         1 (shared with Timer A), Timer A2, Timer B2, Dead time timer)           Serial Internation         Clock Sync. Chiv         1           Serial Internation         Clock Sync. Chiv         2 (SUO)         4 (SUO)           Clock Sync. Chiv         2 (SUO)         4 (SUO)         4 (SUO)           To Cust         3 (UART)         5 (UART)         5 (UART)           Serial Internation         Signamic All All All All All All All All All Al		Event Counter								11 (Timer	A, Timer B)							
Valeholds Turner Dr. Rev miler Ar, miler Ar		2-Phase Encoder Input					1 /s	shared with	Timor 44	3 (ΠΓ Timer Δ1 T	imer Δ2 Ti	imer B2 D	ead time tin	ner)				
Clock Sync. Clock Async.         3 (UART)           Serial Interface         2 (SI/O)         4 (SI/O)           Clock Sync. Only         -         4 (SI/O)           Clock Sync. Only         -         3 (UART)           Clock Sync. Only         -         3 (UART)           Clock Sync. Only         -         3 (UART)           Smat Card/SIM         3 (UART)           Smat Card/SIM         -         1 (UART)           Synchrones Setal Communication UnitSpecial Setal I/O         -         1 (UART)           CAN         Chanels         2         1         2         1           IPDA         -         -         -         10         -           CRG Calculation Grout         1 (GR - CCITT (X <sup>i+</sup> X <sup>i+</sup> + 1))         -         -         -           V/ Converter         -         -         -         -         -           I/O Ports         Inglic Owner Dain Port (Numbers)         -         -         -         -           I/O Ports         Inglic Owner Dain Port (Numbers)         -         -         -         -         -           I/O Ports         Inglic Owner Dain Port (Numbers)         -         -         -         -         -         -	Watchdog Timer						. (	indica ma			1	inor be, b		101)				
Serial Interface         Clock Sync. Only		Clock Sync./ Clock Async.								3 (U	ART)							
Clock Kayne. Unity	Serial Interface	Clock Sync. Only				2 (S	I/O)							4 (S	SI/O)		-	
Inclusion         Operating Frequency/Supply Voltage         Operating Frequency/	I <sup>2</sup> C-bus	Clock Async. Unly								3 (1)								
Smart Card/SIM         1 (UART)           Synchronous Serial Communication Mit/Special Serial I/O         2         1         2         1           CAN         Channels         2         1         2         1           CAN         Channels         2         1         2         1           CAN         Channels         2         1         2         1           CAN         Message Box (Numbers)         16 + 16         16         16 + 16         16           I/DA	IEBus									3 (U	ART)							
Synchronus serial Communication Unit/Special Serial I/O           CAN         Channels         2         1         2         1           IrDA         -	Smart Card/SIM									1 (U.	ART)							
CAN         Channels         2         1         2         1           Message Box (Numbers)         16 + 16         16         16 + 16         16           IrDA         -         -         -         -         -           CRC Calculation Circuit         -         1 (CRC-CCITT (X <sup>16</sup> + X <sup>16</sup> + X <sup>16</sup> + 11))         X/X         -         -           V/ Converter         -         -         -         -         -         -           V/ Or Ports         MoS I/O (Numbers)         .         .         1         .	Synchronous Serial	Communication Unit/Special Serial I/O								3 (U	ART)		-					
InDA	CAN	Channels Message Box (Numbers)		16	+ 16				1			16	2			1	1	
CRC Calculation Circuit         1 (CRC-CCITT (X <sup>16</sup> + X <sup>12</sup> + X <sup>6</sup> + 1))           X/r Converter            Input Only (Numbers)            (VO Ports         Input Only (Numbers)         85         1           WC Converter          2           High Current Drive Port          2           High Current Drive Port          Yes           Pull-Up Resistor         85         111           Debugging         On-Chip Debug          Yes          Yes           Function         On-Chip Debug          Yes          Yes          Yes           Other         ROM Correction Function         Yes          Yes          Yes          Yes           Operating Ambient Temperature (°C)          Yes          Yes          Yes          Yes           Package <sup>8*</sup> PLOP0100KB-A         PLOP0128KB-A         PLOP0128KB-A         PLOP0128KB-A           Part No.         Agg	IrDA	Message box (Numbers)		10	+ 10					-	-	10	+ 10		1		0	
XY Converter	CRC Calculation	Circuit							1 (CR	C-CCITT ()	$X^{16} + X^{12} + X^{12}$	X <sup>5</sup> + 1))						
Induction         Induction <t< td=""><td>X/Y Converter</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>-</td><td>-</td><td></td><td></td><td>-</td><td></td><td></td><td>-</td><td></td></t<>	X/Y Converter									-	-			-			-	
VO Ports         Image: constraint of (Numbers)         Constraint of (Numbers)         Image: constraint of (Numbers)         Image: constraint of (Numbers)           External Interrupts         Pull-Up Resistor         85         111           External Interrupts         11         14           Debugging Function         On-Chip Debug         -         Yes         -         Yes         -         Yes           Chine ROM Correction Function         Yes         -         -         Yes         -         Yes         -         -		Input Only (Numbers)					5				1			1	11		-	
High Current Drive Port         -         -           Pull-Up Resistor         85         111           External Interrupts Pins         11         14           Debugging Function         On-Chip Debug         -         Yes         -         -         Yes         -         -         Yes         -         -         Yes         -	I/O Ports	N-Channel Open Drain Port (Numbers)				0	5				2							
Pull-Up Resistor         85         111           External Interrupt         Pins         11         14           Debugging         On-Chip Debug         -         Yes         -         Yes         -         Yes           Function         On-Board Flash Program         -         Yes         -         Yes         -         Yes         -         Yes           Other         ROM Correction Function         Yes         -         -		High Current Drive Port									-							
External Interrupts Pins     11     14       Debugging Function     On-Chip Debug     -     Yes     -     Yes     -     Yes       On-Board Flash Program     -     Yes     -     Yes     -     Yes     -     Yes       Other Functions     On-Board Flash Program     -     Yes     -     Yes     -     Yes       Other Functions     Others     -     Yes     -     Yes     -     Yes       Operating Frequency/Supply Voltage     -     -     24MHz/3.0 to 5.5V     -     -       Operating Ambient Temperature (*C)     -     -     -     -     -       Package**     PLOP0100KB-A     PLOP0128KB-A     -     -     -       Part No.     Ag		Pull-Up Resistor				8	5							1	11			
Debugging Function         On-Boal Flash Program         -         Yes         Yes         Yes         Yes         Yes         Yes         Yes         Yes         Y	External Interrup	ts Pins			N N	1	1							1	4			
Other Functions         ROM Correction Function Others         Yes         -         Yes         Yes <thyes< th=""> <th< td=""><td>Debugging</td><td>On-Chip Debug</td><td></td><td></td><td>Ye</td><td>es</td><td></td><td></td><td>Y</td><td>es</td><td></td><td></td><td>Ye Ve</td><td>es</td><td></td><td></td><td>Y</td><td>3S</td></th<></thyes<>	Debugging	On-Chip Debug			Ye	es			Y	es			Ye Ve	es			Y	3S
Functions         Others	Other	ROM Correction Function	Yes         -         Yes         -<									-	_					
Operating Frequency/Supply Voltage         24MHz/3.0.to 5.5V           Operating Ambient Temperature (°C)         - 40 to 85           Package <sup>9/2</sup> PLOP0100KB-A         PLOP0128KB-A           Parkage <sup>9/2</sup> PLOP0128KB-A         Colspan="2">Colspan="2"Colspa	Functions	Others								-	-							
Operating Ambient Temperature (°C)        40 to 85           Package*2         PLOP0100KB-A         PLOP0128KB-A           Part No.         d SX X + S + S + S + S + S + S + S + S +	Operating Freque	ency/Supply Voltage								24MHz/3	.0 to 5.5V				_			
Part No. 400 ML 1210 000 ML 12	Operating Ambie Packago*2	ent Temperature (°C)					OOKB-A		-	- 40	to 85				128KB-A			
Part No.         D06N KME-XXX3         D06N KME-XXX3         D06N KME-XXX3         D06N KME-XX3         D06N KME-Y         D06N KME-Y </td <td>Гаскауе</td> <td></td> <td></td> <td></td> <td></td> <td>FLQFU</td> <td>UUKD-A</td> <td></td> <td></td> <td>1</td> <td></td> <td></td> <td>1</td> <td>FLQFU</td> <td>ZOND-A</td> <td></td> <td></td> <td></td>	Гаскауе					FLQFU	UUKD-A			1			1	FLQFU	ZOND-A			
Author         006NLFHGP           006NLFHGP         006NLFHGP           006NLFHGP         006NLFHGP           006NLFHGP         006NLFHGP           006NLFHGP         006NLFHGP           006NLFHGP         006NLFHGP           006NLFHGP         006NLFHGP           006NNMG-XXX         006NNMG-XXX			L.	6			e.	L.			<u>с</u>	GP			d G	L.		
X-3         Y-3         Y-3 <thy-3< th=""> <thy-3< th=""> <thy-3< th=""></thy-3<></thy-3<></thy-3<>			X	XX			XX	XX	0		XX	XX	۵.	0	XX	XX	0	
906NNF	Part No.		ų. X	-9J	HGF	JGF	IE-X	X-9	HGF	JGP	VE->	AG-)	9H	JGF	1E-X	-9Į	HGI	JGF
			NK	NKN	NKF	NKF	NLN	NLN	NLF	NLF	WN	WN	NMF	NMF	NN	NZ ZZ	NNF	NNF
			1306	1306	/306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/30 Series)

Group							M160	C/30P					
	BOM (Bytes)	-	-			6K		96K	+ 4K		12	8K	
	RAM (Bytes)	6	К					5	К				
	ROM Type*1		_		F	N	Λ		F	:		N	N
Memory	Data Flash			-	_			Yes	(4K)		-	_	
	D			Yes (ID Code C	Check Function,				Yes (ID Code C	heck Function			
	Program Security	-	-	ROM Code Pr	otect Function)	-	-		ROM Code Pro	otect Function)		-	-
	CPU						M16C/6	60 Core					
	Basic Instructions						9	1					
CDU	Minimum Instruction Execution Time (ns)						62.5 (@	16MHz)					
CPU	Multiplier						16×1	6→32					
	Multiply-Accumulate Instruction						16×16 -	+ 32→32					
	Barrel Shifter						-	-					
DMA	DMAC (Channels)						2	2					
	DTC/DMACII												
	Address Space (Bytes)						1	M					
External Bus	External Bus Interface		0.1	0	Su	pport for inserti	on of 1 wait sta	tes, Outputs 4	chip-select sigr	als		1	
LAPANSION	DRAM Controllor		Selectable from	n Separate bus	, muniplex bus,	Data Bus Widt	n can be select	ed (8/16-bit), 1	ne number of c	utput address	buses can be s	elected (16/20)	)
	Clock Constantion Circuit						circuite (Main (	plack Sub-clas					
	PLI					2	circuits (Main C	-	N)				
	Subclock						Ye	25					
Clock	On-Chip Oscillator						-	-					
	Oscillation Stop Detection						-	_					
	Frequency Divider						1/n (n=1.2	2, 4, 8, 16)					
	Power Save						Wait	/Stop					
Power Supply	Power-On Reset/POR						-	-					
Voltage Detection	Low Voltage Detection/LVD												
	Resolution × Channels						10-bi	t × 18					
A/D Converter	Sample and Hold						Ye	es					
	Multi-Channel Sample and Hold						-	-					
D/A Converter	Resolution × Channels						-	-					
	8-bit							-					
	16-bit						6 (Timer A	, Timer B)					
	Input Capture							-					
<b>T</b>	Output Compare						-	-					
limer	PWM Output						3 (1 in	ner A)					
	Real-Time Port				-	-	6 (Timor A	- Timor P)			-		
	2-Phase Encoder Input						1 /Tip	(, Timer B)					
	3-Phase Inverter Control							-					
Watchdog Timer								1					
	Clock Sync./ Clock Async.						3 (U/	ART)					
Serial Interface	Clock Sync. Only						-	_					
	Clock Async. Only						-	_					
l <sup>2</sup> C-bus							3 (U/	ART)					
IEBus							1 (U/	ART)					
Smart Card/SIM							1 (U/	ART)					
Synchronous Serial	Communication Unit/Special Serial I/O						1 (0/	ARI)					
CAN	Mossage Box (Numbers)												
IrDA	Message Dox (Numbers)							_					
CRC Calculation	n Circuit					1 (	CRC-CCITT ()	$X^{16} + X^{12} + X^5 +$	1))				
X/Y Converter								-					
	Input Only (Numbers)							1					
	CMOS I/O (Numbers)						8	5		_			
I/O Ports	N-Channel Open Drain Port (Numbers)						2	2					
	High Current Drive Port		-		-	_	-	-			-	-	
	Pull-Up Resistor						8	5					
External Interrup	ots Pins						1	0					
Debugging	On-Chip Debug			-	-	1		Ye	es	V. (0 : 5	-	-	
Function	On-Board Flash Program			res (Unly Rewr	iting is possible)	-		Ye	es	res (Only Rewr	iting is possible)		
Other	Others			Y	es			-			Ye	es	
Operating Freese	oner/Supply Voltage					1014		10MUz/0 7 +-	5.51/				
Operating Ambie	ant Temperature (°C)					1010	- 20 to 85	- 40 to 85	5.5 V				
Operating Amble							2010003,	40 10 00					
					_	_					_		_
		₽́₽	B-A	B_A A	B-A	B-A	₽₽	₽,A	₽A	4	B-A	- A A	B-A
Package*2		R	Xo	20	Xo	Pog	Yo	No	Yo	20	Xo	20	Xo
-		010	010	010	010	010	010	010	010	010	010	010	010
		Å Å	D.	L L L	D.	D D D D D D	PO.	ğ	PO.	ğ	D.	ğ	D.
		4	1	4	Ц	4	Ъ	4	Ъ	PF.	1	4	1
				No te1	Note1	(FP	GP			5	56 1	Υ <sup>Ε</sup> Ρ	(GF
				*L	*L	â	â	0	٩	ž L	2 4 (5	Ŷ	2 X
				1 1	e e e e e e e e e e e e e e e e e e e	d.	d.	L.	ő	L L	Å	0	d.
Part No.		Ъ	GP	AP	AF	A	A	4	4	0	0	ö	
Part No.		12SPFP	12SPGP	12GAP	12GAF	12MA	IZMAI	12FAF	12 FAF	12 GC	12 GC	12 MCF	IZMO
Part No.		0302SPFP	0302SPGP	0302GAP	0302GAF	0302MAI	0302MAI	0302FAF	0302FAF	0302GC	0302GC	0302MCF	0302MC
Part No.		M30302SPFP	M30302SPGP	M30302GAP	M30302GAF	M30302MA	M30302MA	M30302FAF	M30302FAF	M30302 GC	M30302GC	M30302MCF	M30302MC

<sup>1</sup> Data can only be written once and cannot be erased. <sup>a</sup>' F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Q : QZROM version <sup>a</sup>' Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/30 Series)

Group										M160	C/30P								
	DOM (Bits)	1001	. 412	1		10	01/					10	01/			1001	. 41/	05	CK
	ROM (Bytes)	128K +	+ 4K		6	16 K	UK	1:	ĸ		F	19 K	2K	10	ok.	192K	+ 4K K	25	6K 2K
	BOM Type <sup>*1</sup>	514		F		1	A	12		F			Λ	12		U	=	1 12	
Memory	Data Flash	Yes (4	4K)							_						Yes	(4K)	-	_
	Brannen Canuity	Yes (ID	Code 0	Check Fun	ction,			Yes (	ID Code C	Check Fun	iction,		_		Yes (	ID Code C	heck Fun	ction,	
	Flogram Security	ROM	Code Pr	otect Fund	tion)			RON	I Code Pr	otect Fund	ction)				RON	I Code Pr	otect Fund	ction)	
	CPU									M16C/	60 Core								
	Basic Instructions									9	91								
CPU	Minimum Instruction Execution Time (ns)									62.5 (@	216MHZ)								
	Multiply-Accumulate Instruction									16 × 16	+ 32→32				-	-			-
	Barrel Shifter										-								
DMA	DMAC (Channels)										2								
DIMA	DTC/DMACII										-								
	Address Space (Bytes)									1	M								
External Bus	External Bus Interface		Colo	atabla from	Conorata	buo Mul	Sul Sulay buo	Doto Ruo	Sertion of	1 wait sta	ted (8/16)	uts 4 chip-	select sigr	nals	roop buog	a con ha a	alastad (1	6/20)	
Expansion	DRAM Controller		Sele	clable ITOIT	i Separate	bus, iviui	upiex bus,	Data Dus	Width Cal	T De Selec		Jil), The fi		Julpul auu	iess buse	s can be s	elected (	10/20)	
	Clock Generation Circuit								2 circu	uits (Main	clock, Sub	-clock)							
	PLL										-	,							
	Subclock									Y	'es								
Clock	On-Chip Oscillator										_								
	Oscillation Stop Detection										-								
	Frequency Divider									1/n (n=1, 1 Wait	2, 4, 8, 16	)							
Power Supply	Power-On Reset/POR																		
Voltage Detection	Low Voltage Detection/LVD										-								
	Resolution × Channels									10-bi	it $\times$ 18								
A/D Converter	Sample and Hold									Y	és								
B/1 0	Multi-Channel Sample and Hold										-								
D/A Converter	Resolution × Channels																		
	16-bit									6 (Timer A	A. Timer B	)							
	Input Capture										_	/							
	Output Compare										_								
Timer	PWM Output									3 (Tir	mer A)								
	Real-Time Port									-	-								
	Event Counter									6 (Timer A	A, Timer B	)							
	3-Phase Inverter Control										— —								
Watchdog Timer											1								
	Clock Sync./ Clock Async.									3 (U	ART)								
Serial Interface	Clock Sync. Only										_								
1 <sup>2</sup> 0 hus	Clock Async. Only									0./11									
IFBus										3 (U	ART)								
Smart Card/SIM										1 (U	ART)								
Synchronous Serial	Communication Unit/Special Serial I/O									1 (U	ART)								
CAN	Channels																		
L-DA	Message Box (Numbers)																		
CBC Calculation	Circuit								1 (CBC		X <sup>16</sup> + X <sup>12</sup> +	$X^{5} \pm 1))$							
X/Y Converter	Ondat								1 (0110	-00111 (2	_	X + 1))							
	Input Only (Numbers)										1								
	CMOS I/O (Numbers)									ε	35								
I/O Ports	N-Channel Open Drain Port (Numbers)										2								
	High Current Drive Port										-								
External Interrup	ts Pins									1	10								
Debugging	On-Chip Debug	Yes	S						-	-	-					Ye	es	-	-
Function	On-Board Flash Program	Yes	S	Yes (Only Rewri	ting is possible)	-	-	Yes (0	Only Rewr	iting is po	ssible)	-	-	Yes (Only Rewr	iting is possible)	Ye	es	Yes (Only Rewr	iting is possible)
Other	ROM Correction Function	-							Y	es						-	_	Ye	es
Functions	Others								10111-/0		-	7 +- 5 51/							
Operating Ambie	ency/Supply voltage								1010112/3	- 20 to 85	-40  to 8	.7 10 5.5 V 5							
												Ī							
		-	4	-	4	4	-	4	-	4	4	-	4	-	-	-	-	4	-
		ц.	ų	E E	ų,	ų.	ų,	l é	ų,	l d	ц.	ц.	ų.	ц.	ų.	ц.	ų,	ц.	ų,
Package*2		100	100	100	100	100	100	100	100	100	6	100	00	100	0	100	00	100	100
		6 C	ЪО	P P P	ро	PC C	PO	P P P	PO	P P C	Po	Po C	PO	6	PO	6	PO	D D D	PO
		Ъ Н Ц	PLO	L H	РГО	РВС	LL0	L R	L LO	L DH	PLO	L BR	PLO	PR(	PL0	PR(	LL0	PRC	L LO
				100	8	Ę	GP	100	- 1	5	1 pt c	L L	GP	fel	tet (			190	061
		e.	<u>C</u>	L N	<sup>N</sup> d	Ŷ	× ×	L N	2 (5	L P K	2 d.	X	- X	ž L	2 4 (5	۹.	<u>C</u>		4 G
Part No.		CPF	CPC	DPF	DP(	IDP.	IDP-	DPF	DP(	EPF	EPC	EP.	EP-	EPF	EPC	E H	EPG	GPI	GP(
		02F	02F	02G	02 G	02 M	02N	04G	04G	02G	02G	02N	02M	04G	04G	02F	02F	02G	02G
		303	303	303	303	303	303	303	303	303	303	303	303	303	303	303	303	303	303
		Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ

\*: New product \*\*: Under development

<sup>1</sup> Data can only be written once and cannot be erased. <sup>\*1</sup> F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Q : QZROM version <sup>\*2</sup> Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/1N Group)

Group		M16C/1N
	ROM (Bytes)	64K + 4K
	RAM (Bytes)	3К
Memory	ROM Type <sup>*1</sup>	F
	Data Flash	Yes (4K)
	Program Security	Yes (ID Code Check Function, ROM Code Protect Function)
	CPU	M16C/60 Core
	Basic Instructions	91
CPU	Minimum Instruction Execution Time (ns)	62.5 (@16MHz)
	Multiplier	16×16→32
	Demol Chiftee	10×10+32-32
	DMAC (Chappele)	
DMA	DTC/DMACI	_
	Addross Space (Butes)	_
Extornal Bus	External Bus Interface	_
Expansion	Bus Structure	_
	DBAM Controller	_
	Clock Generation Circuit	3 circuits (Main clock, Sub clock, On-chin oscillator)
	PLL	
	Subclock	Yes
Clock	On-Chip Oscillator	Yes
	Oscillation Stop Detection	Yes
	Frequency Divider	1/n (n=1, 2, 4, 8, 16)
	Power Save	Wait/Stop
Power Supply	Power-On Reset/POR	
Voltage Detection	Low Voltage Detection/LVD	_
	Resolution × Channels	10-bit × 14
A/D Converter	Sample and Hold	Yes
	Multi-Channel Sample and Hold	_
D/A Converter	Resolution × Channels	8-bit × 1
	8-bit	4 (Timer 1, Timer X, Timer Z)
	16-bit	1 (Timer C)
	Input Capture	1 (Timer C)
	Output Compare	-
Timer	PWM Output	2 (Timer Y, Timer Z)
	Real-Time Port	-
	Event Counter	1 (Timer X)
	2-Phase Encoder Input	-
	3-Phase Inverter Control	-
Watchdog Timer		
	Clock Sync./ Clock Async.	2 (UART)
Serial Interface	Clock Sync. Only	-
20.1	Clock Async. Only	-
I <sup>-</sup> C-bus		
IEBus		
Smart Card/SIM	0	
Synchronous Serial	Communication Unit/Special Serial I/O	
CAN	Magazana Day (Numbers)	
L-DA	Message Box (Numbers)	
IFDA	Circuit	
CRC Calculation	Circuit	
X/Y Converter	land Only (North and)	
	CMOS I/O (Numbers)	27
I/O Porto	N Channel Open Drain Port (Numbers)	
I/O FOILS	High Current Drive Port	
	Right Current Drive Fort	0
External Interrup	ts Pins	5/ 8
Dobugging	On-Chin Debug	0 Vac
Function	On-Board Elash Program	los Vas
Othor	BOM Correction Function	
Functions	Others	_
Operating Freque	ency/Supply Voltage	16MHz/4.2 to 5.5V
Operating Ambie	ent Temperature (°C)	-40 to 85
Package*2		PLOP0048KB-A
Part No.		M301N2F8FP

\*' F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/Tiny Series)

			<u> </u>												
Group						Ν	M16C/26A	(M16C/26A	.)					M160 (M160	C/26A C/26B)
	BOM (Bytes)	24	К	24K	+ 4K	45	3K	48K	+ 4K	6/	K I		64K	+ 4K	
	BAM (Bytes)		4	K 240				1010			<		0.11		
	POM Tupo*1		1		-		4	-	-	2	、 			:	
Memory	ROW Type	IV.	1		F	N	vi	F	-	N	1		r		
	Dala Flash		-	Yes	(4K)		_	Yes	(4K)	-	-		Yes	(4K)	
	Program Security	-	-	Yes (ID Code C	Check Function,		_	Yes (ID Code C	Check Function,		-	Ye	s (ID Code C	heck Functio	on,
				ROM Code Pr	otect Function)			HOM Code Pro	otect Function)			R	OM Code Pro	otect Functio	n)
	CPU							M16C/6	60 Core						
	Basic Instructions							9	1						
0.011	Minimum Instruction Execution Time (ns)						50 (@2	20MHz)						41.7 (@	24MHz)
CPU	Multiplier							16×1	6→32						
	Multiply-Accumulate Instruction							16×16+	+ 32→32						
	Barrel Shifter							_	_						
	DMAC (Channels)								2						
DMA	DTC/DMACI								_						
	Address Cases (Dutes)								_						
	Address Space (Bytes)								-						
External Bus	External Bus Interface							_	_						
Expansion	Bus Structure							-	-						
	DRAM Controller							_	_						
	Clock Generation Circuit					4 c	circuits (Main	clock, PLL, S	Sub clock, Or	n-chip oscillat	or)				
	PLL							Ye	es						
	Subclock							Ye	es						
Clock	On-Chin Oscillator							Ve	26						
21001	Oscillation Stop Detection							V							
	Froguopov Divider							1/n /n-1 /	2 / 9 16\						
	Dever Cause							1/11 (ff=1, 2	≤, 4, 0, 10)						
	Power Save							Wait/	Stop						
Power Supply	Power-On Reset/POR	ļ						-	-						
voltage Detection	Low Voltage Detection/LVD	ļ						Yes (Low	/ voltage)						
	Resolution × Channels	$10$ -bit $\times$ 12	10-bit  imes 10	$10$ -bit $\times$ 12	$10$ -bit $\times 10$	10-bit $ imes$ 12	$10$ -bit $\times 10$	10-bit $ imes$ 12	$10$ -bit $\times 10$	10-bit  imes 12	10-bit  imes 10	10-bit  imes 12	10-bit  imes 10	10-bit  imes 12	10-bit $ imes$ 10
A/D Converter	Sample and Hold							Ye	es						
	Multi-Channel Sample and Hold							Ye	es						
D/A Converter	Resolution × Channels							-	-						
	8-bit							_	_						
	16-bit							8 (Timer A	Timer B)						
	Input Capture								_						
	Output Capitale														
-	Output Compare							- /	-						
Timer	PWM Output							5 ( I in	ner A)						
	Real-Time Port							-	_						
	Event Counter							8 (Timer A	A, Timer B)						
	2-Phase Encoder Input							3 (Tim	ner A)						
	3-Phase Inverter Control					1 (shared v	with Timer A4	1, Timer A1, T	Timer A2, Tim	ner B2, Dead	time timer)				
Watchdog Timer								1	1						
	Clock Sync./ Clock Async.	3 (UART)	2 (UART)	3 (UART)	2 (UART)	3 (UART)	2 (UART)	3 (UART)	2 (UART)	3 (UART)	2 (UART)	3 (UART)	2 (UART)	3 (UART)	2 (UART)
Serial Interface	Clock Sync. Only		. /	/	/	/	/			/	. ,		. /	. /	,
	Clock Async Only							_	_						
l <sup>2</sup> C-bus	e.e.ski koynor offiy							1 /11/	ART)						
IFBus								1 (U/	4RT)						
Smart Card/SIM								1 /11/	4RT)						
Synchronous Corist	Communication Unit/Coasial Carial I/O							1/1/	4RT)						
Synchronous Serial	Chappele							1 (UA	- III)						
CAN	Crianneis							-							
1.5.1	Message Box (Numbers)							-	-						
IrDA		L						-	_						
CRC Calculation	Circuit					1 (CRC	C-CCITT (X1	$^{\circ} + X^{12} + X^{5} +$	1) /CRC-16	$(X^{16} + X^{15} + X^{15})$	(* + 1))				
X/Y Converter								-							
	Input Only (Numbers)						-	-	-				-		
	CMOS I/O (Numbers)	39	33	39	33	39	33	39	33	39	33	39	33	39	33
I/O Ports	N-Channel Open Drain Port (Numbers)		-						_				-		· · · · · ·
	High Current Drive Port							_	_						
	Pull-Up Besistor	39	33	39	33	39	33	39	33	39	33	39	33	39	33
External Interrur	ts Pins		50					1	1			55	50		
Dobugging	On-Chin Debug	-	-	v	96	-	_	V.		-	. 1		v		
Eunction	On Roard Floot Descrete		_	Ye Ye			_	Ye			_		Ye		
- unotion	DOM-Board Flash Program	Vec (6.11)	a matel - C	Y	85	N== (A 111		Ye	5	No. (A 11)	and the		Ye	:5	
Other	HOW Correction Function	res (Addres	s rhatch × 2)	-	_	res (Addres	s match $\times 2$ )	-		res (Addres	s match × 2)			-	
Functions	Others	L						-	-						
														24MHz/4.	.2 to 5.5V,
Operating Frequ	ency/Supply Voltage					20MHz	z/3.0 to 5.5V,	10MHz/2.7 t	o 5.5V					20MHz/3.	.0 to 5.5V,
														10MHz/2	.7 to 5.5V
Operating Ambie	ent Temperature (°C)						- 20 to 85	- 40 to 85						-40 to 85	-20 to 85
		4	<u>Р</u> -	A-	-8-	A-	-9-	×-	-9-	A-1	е-	<u>۲-</u>	-P	₹-	- <u>-</u>
Dealers *2		Т Щ Ц	jū.	E E	jā	Ř	j d	Ř	j d	Ř	ğ	ЖЕ	ja:	ž	j j
Package*2		948	342	748	742	348	742	948	342	348	342	348	342	348	542
		D C C	POC	502	POC	Poc	POC	202	POC	POC	POC	POC	POC	POC	POC
		ġ	S	ō	1 SE	ō	13S	à	- ISE	ō	ISL	ō	ŝ	ō	L SE
		<b> </b>	ii.	님	L I	님	1 1	L 1	1 1	님	ä	Ц	Ĕ.	Ы	l E
		<u>L</u>	<u>0</u>			<u>C</u>	<u>e</u> .			L.	<u>0</u>				
		X	XF			X	X			X	Υ.				
			×	0	0	Ó				- A	Č.	0_	0	ñ	ř.
		×	×	6	1	~	×	L.	L 15	×	× I	75	L L	6	
Part No.		3A-XX	3A-X	AGI	3AFI	6A-X	6A-X	SAGF	SAFF	8A-X	8A-X	3AGI	3AFF	BGI	BF
Part No.		хх-ремс	3M3A-X	DF3AGI	3F3AFI	M6A-X	3M6A-X	DF6AGF	3F6AFF	X-M8A-X	3M8A-X	JF8AG	3F8AFF	DF8BGI	3F8BF
Part No.		260M3A-XX	263M3A-X	260F3AGF	263F3AFI	260M6A-X	263M6A-X	260F6AGF	263F6AFF	260M8A-X	263M8A-X	260F8AG	263F8AFF	260F8BGI	263F8BF
Part No.		130260M3A-XX	130263M3A-X	130260F3AGF	/30263F3AFF	130260M6A-X	//30263M6A-X	130260F6AGF	130263F6AFF	130260M8A-X	130263M8A-X	130260F8AG	130263F8AFF	/30260F8BGI	/30263F8BF

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (M16C/Tiny Series)

			, .		,															
Group									I	M16C/28	3								M16 (M160	C/28 C/28B)
	POM (Puters)		101 1		6			GAK I AK		06					10	91/	-	1001		,
	ROW (Bytes)	-	40N + 4N		04	ŧr.		04N + 4N		90	Л	01/	90K + 4K		12	on		1201	+ 41	
	RAM (Bytes)				4	ĸ						8K					12	2K		
Memory	ROM Type*1		F		N	Л		F		N N	Л		F		N	Λ			-	
,	Data Flash		Yes (4K)		-	-		Yes (4K)		-	-		Yes (4K)			-		Yes	(4K)	
	Brown Consults	Yes (ID Co	de Check	Function,			Yes (ID C	ode Check	Function,		_	Yes (ID C	ode Check	Function,	_	_	Yes (I	D Code C	heck Fun	ction,
	Program Security	ROM Coc	le Protect	Function)	-	-	ROM Co	de Protect	Function)	-	-	ROM Co	de Protect	Function)	-	-	ROM	Code Pr	otect Fund	ction)
	CPU									M1	6C/60 C	nre								
	Regis Instructions										01	0.0								
	Dasic Instructions									(0.0014)	31								44 7 (0	
CPU	Minimum Instruction Execution Time (ns)								50	(@20MF	1Z)								41.7 (@	24MHZ)
	Multiplier									1	6×16→3	32								
	Multiply-Accumulate Instruction									16>	< 16 + 32-	→32								
	Barrel Shifter										-									
	DMAC (Channels)	1									2									-
DMA	DTC/DMACII										-									
	Address Space (Bytes)										_									
Esternal Due	Extornal Bus Interface										_									
External Bus	Due Obrusture																			
Expansion	Bus Structure			_	_															
	DRAM Controller										-									
	Clock Generation Circuit							4 circ	cuits (Mai	n clock, P	LL, Sub c	clock, On-	chip oscill	ator)						
	PLL										Yes									
	Subclock										Yes									
Clock	On-Chip Oscillator										Vas									
Olocit	On one Oscillation	-									Vee									
	Oscillation Stop Detection									41.1	tes	0.40)								
	Frequency Divider					-				1/n (r	1=1, 2, 4,	8, 16)						-		
	Power Save										Wait/Stop	)								
Power Supply	Power-On Reset/POR										-									
Voltage Detection	Low Voltage Detection/LVD									Yes	(Low volt	age)								
	Resolution × Channels	10-bit	1 × 24	10-bit x 13	10-bit x 24	10-bit x 13	10-bi	t×24	10-bit x 13	10-bit x 24	10-bit x 13	10-bi	t × 24	10-bit x 13	10-bit x 24	10-bit x 13	10-bit x 24	10-bit x 13	10-bit x 24	10-bit x 13
A/D Converter	Sample and Hold										Yes									
100 0000000	Multi-Channel Sample and Hold	<u> </u>									Voc									
D/A Convertor	Resolution v Channels										-									
D/A Converter	Resolution × Ghannels																			
	8-bit	L									-									
	16-bit									8 (Tir	ner A, Tin	ner B)								
	Input Capture									6	8 (Timer S	6)								
	Output Compare									8	(Timer S	6)								
Timer	PWM Output									13 (Ti	mer A. Tir	mer S)								-
	Beal-Time Port					-					_									
	Event Counter									Q (Tir	nor A Tin	oor B)								
	O Dhase Essential lagest	———								0 (Time										
	2-Phase Encoder Input									3 (11me	er A)+1 (1	Imer S)								
	3-Phase Inverter Control						1 (s	shared wit	h Timer A	4, Timer	A1, Timer	r A2, Time	er B2, Dea	d time tin	ner)					
Watchdog Timer											1									
	Clock Sync./ Clock Async.										3 (UART)	1								
Serial Interface	Clock Sync. Only	2 (S	I/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)	2 (S	GI/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)	2 (5	i/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)
	Clock Async, Only																			
I <sup>2</sup> C-bus										2 (Multin	master I <sup>2</sup> (									-
IERus										2 (1910101		<i>b</i> , <i>b</i> /(11)								
Case and Canad/OIM		——																		
Smart Card/Silvi											T (UART)									
Synchronous Serial	Communication Unit/Special Serial I/O										1 (UART)									
CAN	Channels										-									
OAN	Message Box (Numbers)										-									
IrDA											-									
CRC Calculation	Circuit	1									-									
X/Y Converter											-									
701 001101101	Input Only (Numbors)	<u> </u>									_									
	Input Only (Numbers)	-			74		_			74		-			74		74			
	CMOS I/O (Numbers)		1	55	/1	55	/	1	55	/1	55	/	1	55	/1	55	/1	55	/1	55
I/O Ports	N-Channel Open Drain Port (Numbers)										-									
	High Current Drive Port										-									
	Pull-Up Resistor	7	1	55	71	55	7	'1	55	71	55	7	1	55	71	55	71	55	71	55
External Interrup	ots Pins										11									
Debugging	On-Chip Debug		Yes		-	_		Yes		-	_		Yes		-	-		Ye	es	
Function	On-Board Flash Program		Yes		-	_		Yes		-	_		Yes		_	_		Y	25	
Other	POM Correction Eulection	<u> </u>			Voc (Addroc	c match v 2)				Voc (Addroc	c match v 9)				Voc (Addroc	c match v 2)			_	
Eurotions	Others				103 (Addica	5 mator × 2)				103 (Addica	5 matori × 2)				103 (Additos	5 matori × 2j				
T UTICUOTIS	Others																			
																			24MHz/4.	2 to 5.5V,
Operating Frequ	ency/Supply Voltage							20MF	Iz/3.0 to	5.5V, 10M	IHz/2.7 to	5.5V							20MHz/3.	0 to 5.5V,
																			10MHz/2.	7 to 5.5V
		- 20 to 85,	- 20		00.1.05	40.1.0	-	- 20		001.05	40.1.0	-	- 20			05 44			40	
Operating Amble	ent lemperature (C)	- 40 to 85	to 85	-	- 20 to 85,	- 40 to 8	5	to 85	-	-20 to 85,	- 40 to 8	15	to 85		- 20 to	0 85, - 40	J to 85		- 40	10 85
					1															
		4	<	4	4	4	4	<.	4	4	4	4	<	4	4	Ą	ج.	4	4	4
		8	ģ	8	8	8	8	ģ	8	9	8	9	<u> </u>	E E	8	<b>9</b>	8	8	8	<u><u> </u></u>
Package*2		8	85	64	80	64	80	82	64	80	641	80	8	64	80	64	80	64	80	64
		8	ö	8	8	ē	Ö	Õ	8	8	8	8	8	0	ÖÖ	8	Ö	ē	Ö	8
		6	Ó	L L	L L	L L L	L L	Ŭ	L L L	6	L L	L L	Ŭ	L L L	L L	L L	L d	P L	L G	L L
		1 2 1	ΠL	JLC	5	5	5	F	5	5	5	۲		Ľ	5	۲,	5	L L	1 7 1	2
			4	-	-						4			<u><u> </u></u>	<u><u></u></u>		-	<u> </u>	<u> </u>	
										우	우				₽	무				
					Ŧ	Ť				×	×				×	×				0
			g	۵.	×	X	۵.	g	۵.	X	X	۵.	Q	۵.	×	×		<u>_</u>	Ξ	Ξ
Part No.		H9	9	H9	-9	8	H8	8	H8	-FI	-Al	AH	¥.	AH	ģ	ģ	5 5	Ъ.	CB	CB
		LO LO	10F	E E	N0 V0	2	UL L	LOF	E E	No.	2	E OF	E OF	E E	00	2	10F	E E	LOF	E E
		028	)28	)28	)28	)28	128	)28	)28	128	128	128	)28	)28	)28	128	)28	028	128	)28
		130	//30	130	130	130	A3C	130	A3C	130	A3C	130	130	130	130	130	130	A3C	130	/30
			<	<	<	<	<	<	<	<	<	<	<	<	<	<	<	<	<	<

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/Tiny Series)

Group						M16	C/29				
	ROM (Bytes)	64	ιK	96	6K	96K	+ 4K	12	вК	128K	+ 4K
	RAM (Bytes)	4	ĸ		8	к			12	2K	
Memory	ROM Type*1		N	Λ		F	-	N	1	F	
	Data Flash		-			Yes	(4K)	-		Yes (ID Code C	(4K)
	Program Security		-	-		ROM Code Pr	otect Function)	-	-	ROM Code Pr	otect Function)
	CPU					M16C/6	50 Core			1	,
	Basic Instructions					9	1				
CPU	Minimum Instruction Execution Time (ns)					50 (@2	20MHz)				
	Multiplier					16×1	6→32				
	Barrel Shifter					16 × 16 -	+ 32→32 -				
	DMAC (Channels)						2	-			
DMA	DTC/DMACII					-	_				
	Address Space (Bytes)					-	-				
External Bus	External Bus Interface						-				
Expansion	DBAM Controller										
	Clock Generation Circuit				4 circuits (	Main clock, PLL, S	Sub clock, On-chip	oscillator)			
	PLL					Ye	es				
	Subclock					Ye	es				
Clock	On-Chip Oscillator					Ye	es				
	Oscillation Stop Detection					Ye	95 2 4 9 16)				
	Power Save					Wait	2, 4, 8, 16) /Stop				
Power Supply	Power-On Reset/POR						-				
Voltage Detection	Low Voltage Detection/LVD					Yes (Low	voltage)			-	
	Resolution × Channels	10-bit × 27	10-bit × 16	10-bit × 27	10-bit × 16	10-bit × 27	10-bit × 16	10-bit × 27	10-bit × 16	10-bit × 27	10-bit × 16
A/D Converter	Sample and Hold					Ye	85				
D/A Converter	Resolution × Channels					-	-				
	8-bit					-	-				
	16-bit					8 (Timer A	, Timer B)				
	Input Capture					8 (Tin	ner S)				
Timor	Output Compare					8 (Tin	ner S)				
Timer	Real-Time Port					13 (1111181 /					
	Event Counter					8 (Timer A	, Timer B)				
	2-Phase Encoder Input					3 (Timer A)-	⊦1 (Timer S)				
144 - 1 - 1 <b>T</b>	3-Phase Inverter Control			1	1 (shared with Tim	ner A4, Timer A1, T	Timer A2, Timer B	2, Dead time timer	)		
vvatchdog Timer	Clock Sync / Clock Async					3 (1)					
Serial Interface	Clock Sync. Only	2 (SI/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)	2 (SI/O)	1 (SI/O)
	Clock Async. Only					-	-				
I <sup>2</sup> C-bus						2 (Multi mast	er I <sup>2</sup> C, UART)				
IEBus Smort Cord/SIM						1 (U/	ART)				
Synchronous Serial	Communication Unit/Special Serial I/O					1 (U	ART)				
0,000	Channels					. (0	1				
CAN	Message Box (Numbers)					1	6				
IrDA	<b>0</b>					-	-	x15 x2			
CRC Calculation	Circuit				1 (CRC-CCII	1 (X <sup>10</sup> + X <sup>12</sup> + X <sup>0</sup> +	1) /CRC-16 (X <sup>10</sup>	$+ X^{13} + X^{2} + 1))$			
	Input Only (Numbers)					-	-				
	CMOS I/O (Numbers)	71	55	71	55	71	55	71	55	71	55
I/O Ports	N-Channel Open Drain Port (Numbers)					-	-				
	High Current Drive Port	71		71	55	-	-	71		71	
External Interrun	ts Pins	/1	55	71	55	1 1	1	71	55	71	55
Debugging	On-Chip Debug		-	-		Ye	98	-	-	Ye	s
Function	On-Board Flash Program		-	_		Ye	es	-	-	Ye	s
Other	ROM Correction Function		Yes (Addres	s match × 2)		-	-	Yes (Addres	s match × 2)	-	-
Functions	Others						- 10MH=/2 7 to 5 5	V			
Operating Ambie	ency/Supply voltage				2	- 20 to 85	- 40 to 85	v			
g.											
		đ	4	đ	4	đ	đ	4	4	đ	4
		Ą	Ą	ц.	Ч. Ч.	ц.	θ	ų.	Ą	ц.	Ą
Package*2		080	064	080	064	080	064	080	064	080	064
		DPO	DO	DO	DO	DO	Ōd	DO	DO	Dod	DO
		PLO	PLO	PLO	PLC	PLO	PLO	PLO	PLO	L PLO	PLO
		<u> </u>	무	무	우			웃	<u>₽</u>		
		1××	1XX	1XXX	1XX		C	XX	XX	0	0
Part No.		18-X	18-X	1A-X	IA-X	AHF	AHF	<u>j</u>	Ç-Ç	E.	GH
		M06	91 N	M06	91M	90E	915	M06	91 N	90F	91F
		302:	302	302:	302:	302	302	302	302	302:	302
		Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ	Σ

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/6H Group)

Group			M16C/6H	
	ROM (Bytes)	128K	25	6K
	RAM (Bytes)	5K	8	K
	ROM Type*1	1	Ň	F
Memory	Data Flash		_	
	Program Security	-	-	Yes (ID code check function, ROM code protect function)
	CPU		M16C/60 Core	
	Basic Instructions		91	
CPU	Minimum Instruction Execution Time (ns)		62.5 (@16MHz)	
	Multiplier		16×16→32	
	Multiply-Accumulate Instruction		16×16 + 32→32	
DMA	DMAC (Channels)		2	
	Clock Generation Circuit		2 circuits (Main clock, Sub-clock)	
	PLL		-	
	Subclock		Yes	
Clock	Real Time clock		Yes	
	On-Chip Oscillator		-	
	Frequency Divider		1/n (n = 1, 2, 4, 8, 16)	
	Power Save	Normal operation	(High-speed, Medium-speed, Low-speed, Low-power consu	Imption)/Wait/Stop
A/D Converter	Resolution × Channels		8-bit × (8 + 2)	
D/A Converter	Resolution × Channels		-	
Timer	16-bit		11 (Timer A, Timer B)	
Watchdog Timer			1	
	Clock Sync./ Clock Async.		3 (UART0 to UART2)	
Serial Interface	Clock Sync. Only		2 (SI/O3, SI/O4)	
	Clock Async. Only		-	
I <sup>2</sup> C-bus			4 (UART0 to UART2 + Multi master I <sup>2</sup> C)	
IEBus			1 (UART2)	
Smart Card/SIM			1 (UART2)	
Synchronous Serial	Communication Unit/Special Serial I/O		-	
CAN	Channels		-	
OAN	Message Box (Numbers)		-	
CRC Calculation	Circuit		1 (CRC–CCITT (X <sup>16</sup> + X <sup>12</sup> + X <sup>5</sup> + 1))	
	Input Only (Numbers)		1	
I/O Ports	CMOS Output Only (Numbers)			1
1/01/01/03	CMOS I/O (Numbers)		79	
	N-Channel Open Drain Port (Numbers)		4	
External Interrup	ts Pins		8	
Debugging Function	On-Board Flash Program		-	Yes
Other	ROM Correction Function	Yes (Adress	s match × 4)	-
Functions	Others		VBI Data slicer (PDC, VPS, WSS, EPG-J, CCD, CC2X, ID-1	
Operating Freque	ency/Supply Voltage		16MHz/4.5 to 5.5V	
Operating Ambie	nt Temperature (°C)		– 20 to 70	
Package*2			PRQP0100JB-A	
Part No.		M306H7MC-XXXFP	M306H7MG-XXXFP	M306H7FGFP

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/6S Group)

Group		M16C/6S
	ROM (Bytes)	96K
	RAM (Bytes)	24К
Memory	ROM Type*1	F
	Data Flash	-
	Program Security	Yes (ID code check function, ROM code protect function)
	CPU	M16C/60 Core
	Basic Instructions	91
CPU	Minimum Instruction Execution Time (ns)	65.1 (@15.36MHz)
010	Multiplier	16×16→32
	Multiply-Accumulate Instruction	16×16+32→32
	Barrel Shifter	-
DMA	DMAC (Channels)	2
DIVIA	DTC/DMACII	-
	Address Space (Bytes)	-
External Bus	External Bus Interface	-
Expansion	Bus Structure	-
	DRAM Controller	-
	Clock Generation Circuit	2 circuits (Main clock, On-chip oscillator)
	PLL	_
	Subclock	-
<b>.</b>	Real Time clock	_
Clock	On-Chip Oscillator	Yes
	Oscillation Stop Detection	
	Frequency Divider	1/n (n=1, 2, 4, 8, 16)
	Power Save	Normal operation (High-speed, Medium-speed)/Wait/Stop
Power Supply	Power-On Beset/POB	
Voltage Detection	Low Voltage Detection/LVD	_
	Besolution × Channels	_
A/D Converter	Sample and Hold	_
A/D Conventer	Multi-Channel Sample and Hold	_
D/A Convertor	Resolution v Channels	_
D/A Converter	A bit	_
	o-bit	E (Times A)
	Insut Casture	S (Time A)
-	Output Compare	
Timer	Pww Output Deal Time Deat	
	Real-Time Port	
	Event Counter	
	2-Phase Encoder Input	
147	3-Phase Inverter Control	
Watchdog Timer		
	Clock Sync./ Clock Async.	2 (UAR10, UAR11)
Serial Interface	Clock Sync. Only	2 (SI/04 is internally connected to 11800)
.2	Clock Async. Only	1 (UART2)
I <sup>-</sup> C-bus		3 (UART0 to UART2)
IEBus		-
Smart Card/SIM		-
Synchronous Serial	Communication Unit/Special Serial I/O	
CAN	Channels	-
	Message Box (Numbers)	-
IrDA		-
CRC Calculation	Circuit	-
X/Y Converter		-
	Input Only (Numbers)	1
	CMOS I/O (Numbers)	20
I/O Ports	N-Channel Open Drain Port (Numbers)	1 (P7_0)
	High Current Drive Port	-
	Pull-Up Resistor	20 (Pull-up resistor can be set every four ports)
External Interrup	ts Pins	3 (INT1-INT3)
Debugging	On-Chip Debug	Yes
Function	On-Board Flash Program	Yes
Other	ROM Correction Function	-
Functions	Others	Power line communication function
Operating Freque	ency/Supply Voltage	15.36MHz/3.0 to 3.6V
Operating Ambie	nt Temperature (°C)	- 20 to 85, - 40 to 85
Package*2		PLQP0064KB-A
-		
Part No.		M306S0FAGP

\*\* F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/39P Group)

Group		M160	C/39P						
	ROM (Bytes)	128K	192K						
	RAM (Bytes)	5K	6K						
Memory	ROM Type*1	N	M						
	Data Flash	-	-						
	Program Security	-	_						
	CPU	M16C/6	60 Core						
	Basic Instructions	9	1						
CPU	Minimum Instruction Execution Time (ns)	62.5 (@	16MHz)						
	Multiplier	16×1	6→32						
	Multiply-Accumulate Instruction	16×16	+ 32→32						
DMA	DMAC (Channels)		2						
	Clock Generation Circuit	2 circuits (Main (	clock. Sub clock)						
	PLI		-						
	Image: Second								
Clock	On-Chin Oscillator	103 (02.	-						
	Erequency Divider	1/n (n-1 5	2 4 8 16)						
	Power Save	Normal operation (High-speed Medium-speed	Low-speed Low-nower consumption)/Wait/Ston						
A/D Convertor	Posolution × Channels	Normal operation (ringh speed, mediam speed,							
D/A Converter	MIEC/39P           RAM (bytes)         128K         192K           RAM (bytes)         5K         0K           Data Flash         -         -           Opgan Security         -         -           Opgan Security         -         -           OPGU         MIEC/30P         -           Bala Instructions         91         -           Mitroin Instruction Security         -         -           Multipler         04/5 (15 Mitro)         -           Multipler         62.5 (16 Mitr)         -           Multipler         -         -           OlAC (Channels)         2         -           Clock Generation Circuit         2 cloculs Min clock, Sub clock)         -           PLL         -         -           Frequency Divider         Normal operation (High-speed, Low power consumption)/WallStop         -           Frequency Divider         Normal operation (High-speed, Low power consumption)/WallStop         -           Frequency Divider         Normal operation (High-speed, Low power consumption)/WallStop         -           Frequency Divider         Normal operation (High-speed, Low power consumption)/WallStop         -           Frequency Divider         Normal operation (Hig								
D/A Converter	16 bit	6 (Timer I	Timer P)						
	DW/M Output	S (Intel A	(, Timer B)						
Timer	NIBC/39P           RAM (Bytes)         128K         192K           RAM (Bytes)         0K         0K           ROM Type*         0K         0K           ROM Type*         0K         0K           ROM Type*         0K         0K           Data Flash         -         -           Program Security         -         -           CPU         MICC600 Core         -           Basic Instructions         91         -         -           Multiply-Accumulate Instructions         91         -         -           Multiply-Accumulate Instructions         16 to 14 ac-32         -         -           Multiply-Accumulate Instructions         2         -         -         -           Code Generation Concut         2 circuits (Main code, Stock)         -         -         -           PL         -         -         -         -         -         -           Processave         Normal operation (High-speed, Medium-speed, Low speed,								
	Event Counter	Imer A, Timer B)							
	2-Phase Encoder Input	1 (shared wi	th Timer A2)						
Watchdog Timer									
Serial Interface	Clock Sync./ Clock Async.	2 (UARI 1	I, UART2)						
-0	Clock Sync. Only	1 (used in UARIC	), VFD Controller)						
I <sup>2</sup> C-bus		2 (shared with U	JART1, UART2)						
IEBus		1 (shared w	vith UART2)						
Smart Card/SIM		1 (shared w	vith UART2)						
Synchronous Serial	Communication Unit/Special Serial I/O	1 (UART2 : Sp	pecial mode 2)						
VFD		High Current Drive Port 34 (Segment (N	lumbers) ≤ 32, 2 ≤ Digit (Numbers) ≤ 16)						
CRC Calculation	Circuit	1 (CRC-CCITT ()	$X^{16} + X^{12} + X^5 + 1))$						
	Input Only (Numbers)		1						
	CMOS I/O (Numbers)	5	1						
I/O Ports	High Current Drive Port	3	34						
	N-Channel Open Drain Port (Numbers)	2 (P7_0	0, P7_1)						
	Pull-Up Resistor	51 (Pull-up resistor can	be set every four ports)						
External Interrup	its Pins		7						
Other	Basic Instructions         Difference           Multiplier         0         0.01								
Functions	Others	-	-						
Operating Frequ	ency/Supply Voltage	When using VFD:16MHz/4.5 When not using VFD:16MHz/4	5 to 5.5V, 10MHz/3.0 to 3.6V, 4.2 to 5.5V, 10MHz/2.7 to 5.5V						
Operating Ambie	ent Temperature (°C)	- 20	to 75						
Package*2		PRQP0	100JB-A						
Part No.		Mk (Bytes)         128K           Mk (Bytes)         5K           Mk Type"         5K           Mk Type"         -           tap Flash         -           opgam Security         -           U         MtGreb Occore           sic Instruction Exection Time (ns)         62.3 (et MuHz)           tighty Accumulate Instruction         62.4 (et MuHz)           tighty Accumulate Instruction         16 x 16 -32           AGC (Channels)         2           ack Generation Circuit         -           AGC (Channels)         -           bild         -           bild operation (High-speed, Medium-speed, Low-power consumption)/           solution x Channels         10-bit x 18           solution x Channels         -           -bit         G (Finer AT Timer B)           Yikase Encoder Input         1 (shared with Timer A)           ent Counter         1 (shared with Timer A)           right Cancer         1 (shared with UART2)           tight Cancer         1 (shared with UART2)           tight Accurrent Drive Port 34 (segment (humbers) < 12, 22, 22 S Digit (Numbers) < 15							

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (R8C/Tiny Series)

Group								F	R8C/1	8													R	8C/1	9						
	ROM (Bytes)	İ —	4K			8	к			12	2K			1	6K		4	1K + 2I	ĸ		8K -	2K			12K	+ 2K			16K	+ 2K	
	RAM (Bytes)		384			51	12			76	68			1	K			384			51	2			7	68			1	K	
Memory	ROM Type*1																F														
	Data Flash								-														Y	es (2k	<)						
	Program Security											Yes	(ID co	ode ch	eck fur	nction	, RON	1 code	protec	ct funct	tion)										
	CPU															R8C	Core														
	Basic Instructions	<u> </u>														3	39														
CPU	Minimum Instruction Execution 1 line (ns)														5	10 (@2	20MH	z)													
	Multiple														16	V 16	1 22-	222													
	Clock Generation Circuit												2	circuit	ro Mai	n cloc	+ 32- k On	chin o	scillat	or)											
	PLI												2	circuit	5 (10101		_	criip o	Somat	01)											
	Subclock															-	_														
Clash	Real Time clock															-	_														-
CIOCK	On-Chip Oscillator										١	/es (H	igh pr	recisio	n, High	spee	d : 8N	1Hz, Lo	ow spe	eed : 12	25kHz	)									
	Oscillation Stop Detection															Y	es														
	Frequency Divider														1/n	(n=1,	2, 4, 8	, 16)													
	Power Save														_	Wait	/Stop														
Power Supply	Power-On Reset/POR															Y	es														
Voltage Detection	Low Voltage Detection/LVD	-													Yes (V	oitage		ction 2	)												
A/D Converter	Sample and Hold																_														
D/A Converter	Besolution × Channels															-	_														
Birtoontoitoi	8-bit														2 (T	imer )	K. Tim	er Z)													
	16-bit				-											1 (Tir	ner C	)													
	Input Capture	1													1 (sh	aed w	ith Tir	ner C)													-
	Output Compare														1 (sh	aed w	ith Tin	ner C)													
Timer	PWM Output														1 (sh	aed w	ith Tir	ner Z)													
	Real-Time Port		1 (shaed with Timer Z)																												
	Event Counter			1 (shaed with Timer Z) – 1 (shaed with Timer X) –																											
	2-Phase Encoder Input			1 (shaed with Timer X) — —																											
Martin I The second	3-Phase Inverter Control																														
Watchdog Timer	Clack Syna / Clack Asyna										1 (Wit	n auto	omatio	starti	ng tuno		AND CIO	DCK SOL	Irce p	rotectio	on tun	ction)									
Sorial Interface	Clock Sync./ Clock Async.															1 (0/	- -														
Senai internace	Clock Async Only															1 (1)															
I <sup>2</sup> C-bus																. (0/	_														
Synchronous Serial	Communication Unit/Special Serial I/O																_														
	Channels																-														
CAN	Message Box (Numbers)															-	-														
	Input Only (Numbers)																3														
	CMOS I/O (Numbers)															1	3														
I/O Ports	N-Channel Open Drain Port (Numbers)																-														
	High Current Drive Port																4														
Eutomal Internet	Pull-Up Resistor															1	3														
External Interrup	On-Chin Dobug																/														
Function	On-Board Elash Program																es														
Other	ROM Correction Function																_														
Functions	Others															comp	arato	r													
Operating Freque	ency/Supply Voltage												:	20MHz	z/3.0 to	5.5V	10MI	Hz/2.7	to 5.5	V											
Operating Ambie	unt Temperature (°C)	20	to 95	40	to 95			20	to 95			- 40	20	) to 95	- 40		20 to	05	- 40		00 to 9	E	40	to 95		20	to 95		- 40	20	to 95
Operating Amble	ant temperature ( C)	- 20	10 65	- 40	10 85			- 20	10 85			to 85	- 20	10 85	to 85	_	2010	65	to 85	- 2	20 10 2	5	- 40	10 85		- 20	10 85		to 85	- 20	10 85
		4		ج.		4-1	A-B	Ą	4-J	A-B	.	4	¥-	A-B	<	ŗ	₹.		Ā		A-B	4-V	<	¢	A-B	Y-	4	A-1		¢	A-B
Packago*2		0B/		ŃB		0B/	X8	Я	OBA	28K	1	Ŕ	B	- Xa	9		OBA		ЛB		X8	0B/	<u>a</u>		8	BA	Ŕ	OBA	ġ	Ś	1 X
1 ackage		02		020		00	00	020	00	00		2020	00	00		NZ0	02		020		00	00		Į.	00	00	050	002		ž	00
		PP		PO		DP(	NO N	PO	DPD	NO N		D	PP0	N N			DP		SPO		NO N	DPC		5	N N	DPD	PO	DPO	G	5	N S
		ЧЧ		PL,		БЧ	Ъ	PL,	H	Ъ		Ľ	H H	L ≥	Ē	Ľ	РВ		PL,		Ρ	РВ	ā	Ĺ	≥	H H	L L	РВ	ā	ذ -	≧
				R8F2118155         F8F2118105           R8F21181055         PLSP0020UB-A           R8F21182057         State of the control of th																											
																							0	0							
Part No.		8	BP	DSF	DSF	Q	Ę	P	0	Ę	P	DSF	0	Ę	DSF	ЪР	8	SP	DSF	SP	P	DC	DSF	DSF	P	0	PP P	0	DSF	P	Ę
		181	181	181	182	182	182	182	183	183	183	183	84	184	184	184	191	191	191	192	192	192	192	193	193	193	193	194	194	194	194
		21.	21.	211	211	21.	21.	21	21.	21.	21	211	211	211	211	21.	211	21.	21.	21.	21.	21.	:21	21.	21.	21	211	21.	21.	51.	21
		R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F	R5F

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

	(1100		•••								_					_	_						_	_	_						
Group								R8	C/1A	4													R	8C/1	В						
	ROM (Bytes)		4K			8	К			12	2K			16	δK		4	1K + 2	K		8K +	- 2K			12K	+ 2K			16K	+ 2K	
	RAM (Bytes)		384			51	12			76	68			1	K			384			51	2			76	68			1	К	
Memory	ROM Type*1															1	=														
	Data Flash								-														Y	es (2k	3)						
	Program Security											Yes	(ID co	de che	eck fur	iction,	ROM	1 code	prote	ct func	tion)										
	CPU															R8C	Core														
	Basic Instructions															8	9														
CPU	Minimum Instruction Execution Time (ns)													_	5	0(@2	20MH2	z)													
	Multiplier															16×1	6→32	2													
	Multiply-Accumulate Instruction														16	×16 ·	+ 32-	→32													
	Clock Generation Circuit												2	circuit	s (Maii	n cloc	k, On-	-chip o	scillat	or)											
	PLL															-															
	Subclock															-	_														
Clock	Real Time clock															-	_														
	On-Chip Oscillator										Y	es (Hi	gh pre	ecision	, High	spee	d : 8M	IHZ, LO	ow spe	ed : 1	25kHz	)									
	Oscillation Stop Detection	<u> </u>												_	41.1	Ye	es	10)													
	Frequency Divider	<u> </u>													1/n (	n=1, 2	2, 4, 8	, 16)													
	Power Save															vvaiu	Stop														
Power Supply Voltage Detection	Power-On Reset/POR	<u> </u>													(00 ())	Te ne	dotor	tion 0	1)												
Voltage Detection	Low voltage Detection/LVD														res (v	10 b	it v 4	clion 2	)												
A/D Converter	Resolution × Channels															0-01 V	1L × 4														
D/A Convertor	Bosolution × Channols															10	-														
DIA COnverter	8-bit														2 (T	mor )	Tim	or 7)													
	16-bit														- ( ! !	1 (Tin	ner C)														
	Input Capture														1 (sha	red w	ith Tir	ner C)	)												
	Output Compare														1 (sha	red w	ith Tir	mer C)	)												
Timer	PWM Output			1 (shared with Timer Z) —																											
	Real-Time Port			i (snared with Timer Z) – 1 (shared with Timer X)																											
	Event Counter			– 1 (shared with Timer X)																											
	2-Phase Encoder Input			1 (shared with Timer X) -																											
	3-Phase Inverter Control			1 (snared with Timer X) 																											
Watchdog Timer											1 (with	n auto	matic	startir	g fund	tion a	nd clo	ock so	urce p	rotecti	on fun	ction)									
	Clock Sync./ Clock Async.															1 (UA	RT0)														
Serial Interface	Clock Sync. Only															-	_														
.0	Clock Async. Only															1 (UA	RT1)														
I <sup>-</sup> C-bus	0											1 (sł	nared	with S	ynchro	onous	Seria	I Com	munic	ation	Jnit)						_				
Synchronous Serial	Communication Unit/Special Serial I/O	<u> </u>													1 (S	narec	1 with	FC)													
CAN	Magazara Roy (Numbera)	<u> </u>																													
	Input Only (Numbers)																2														
	CMOS I/O (Numbers)															1	3														
I/O Ports	N-Channel Open Drain Port (Numbers)																_														
1/01/01/13	High Current Drive Port																1														
	Pull-Up Besistor															1	3														
External Interrup	ots Pins															-	7														
Debugging	On-Chip Debug															Ye	es														
Function	On-Board Flash Program															Ye	es														
Other	ROM Correction Function															-	-														
Functions	Others																-														
Operating Frequ	ency/Supply Voltage	<b> </b>											2	20MHz	/3.0 to	5.5V,	10MF	Hz/2.7	to 5.5	V											
Operating Ambie	ent Temperature (°C)	– 40 to 85		-	20 to 1	85		- 40 to 85	- 20 to	o 85	- 40 to 85	- 20	to 85	- 40 to 85	- 20	to 85	- 40 to 85		- 20	to 85		- 40 to 85	– 20 to 85	– 40 to 85	-	20 to 8	85	- 40 to 85	- :	20 to 8	35
Package*2		0.IB_A	K-000	PBA-A	OUB-A	28KA-B	eoba-a	OUB-A		28KA-B	OUB-A	V V QU	K-KO0:			28KA-B		MB-A	OBA-A	28KA-B	V al o	5	OBA-A	<ul><li>a</li></ul>	2	28KA-B	OBA-A			28KA-B	OBA-A
Ŭ			Loruz	RDP002	LSP002	WQN00	RDP002	LSP002		WQN00	LSP002					WQN00		LSP002	RDP002	WQN00			RDP002			WQN00	RDP002			WQN00	RDP002
				•	œ.	Œ.	e.			E.	CL.	-			-	EL.			<u>م</u>	Œ.	•	-	۵.	0	-	α.	<u>م</u>	•	-	E.	<u>L</u>
Part No.		R5F211A1DSP	R5F211A1SP	R5F211A1DD	R5F211A2SP	35F211A2NP	R5F211A2DD	R5F211A2DSP	R5F211A3SP	R5F211A3NP	R5F211A3DSP	R5F211A3DD	R5F211A4DD	R5F211A4DSP	R5F211A4SP	35F211A4NP	R5F211B1DSP	R5F211B1SP	R5F211B1DD	R5F211B2NP	35F211B2SP	35F211B2DSP	35F211B2DD	35F211B3DSP	35F211B3SP	35F211B3NP	35F211B3DD	35F211B4DSP	35F211B4SP	35F211B4NP	35F211B4DD

### • Specifications (R8C/Tiny Series)

\*' F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (R8C/Tiny Series)

Group			R8C/22			R8C/23										
	ROM (Bytes)	32K	48K	RBC/23           64K         32K + 2K         48K + 2K         64K           3K         2K         2.5K         3           F         Yes (ID code check function)         Yes (2K)         Yes (2K)           7         7         Yes (2K)         Yes (2K)           7         89         50 (68 20MHz)         15 (15 -32           15 x 16 + 32 - 32           2 circuits (Main clock, On-chip oscillator)         -         -         -           -         -         -         -         -           -         -         -         -         -           Yes (High precision, High speed : 40MHz, Low speed : 125kHz)         Yes         -         -           Yes (Votage detection 2)         1/16 (n=1 2, 4, 8, 16)         -         -           Yes (Votage detection 2)         -         -         -         -           Yes (Votage detection 2)         -         -         -         -           Yes (Votage detection 2)         -         -         -         -           2 (Timer RD)         -         -         -         -         -           9 (shared with Timer RD)			64K + 2K									
	RAM (Bytes)	2K	2.5K	2.5K	ЗK											
Memory	ROM Type*1			F												
,	Data Flash		_			Yes (2K)										
	Program Security			Yes (ID code check function,	ROM code protect function)											
	CPU			R8C	Core											
	Basic Instructions			8	9											
CPU	Minimum Instruction Execution Time (ns)		50 (@ 20MHz) 16 × 16 → 32 16 × 16 + 32 → 32 2 circuits (Main clock, On-chip oscillator) 													
	Multiplier		89           50 (@20MHz)           16 × 16 → 32           16 × 16 → 32           2 circuits (Main clock, On-chip oscillator)           -           -           -           -           -           -           -           -           -           -           -           -           -           -           -           -           -           Yes (High precision, High speed : 40MHz, Low speed : 125kHz)           Yes           -           -           -           -           Yes           1/n (n=1, 2, 4, 8, 16)           Yes           Yes           Yes           Yes (Voltage detection 2)           10-bit × 12           Yes           -           3 (Timer RA, Timer RB, Timer RE)           2 (Timer RD)           8 (shared with Timer RD)           9 (shared with Timer RD, Timer RE)           7 (shared with Timer RD)           -           -           -													
	Multiply-Accumulate Instruction		16 × 16 + 32→32       2 circuits (Main clock, On-chip oscillator)       -       -       -       Yes (High precision, High speed : 40MHz, Low speed : 125kHz)       Yes       1/n (n=1, 2, 4, 8, 16)       Wait/Stop       Yes       Yes (Violtage detection 2)       10-bit × 12       Yes       2       2       2       3 (Timer RA, Timer RB, Timer RE)       2 (Timer RD)       8 (shared with Timer RD)       9 (shared with Timer RE)													
	Clock Generation Circuit		2 circuits (Main clock, On-chip oscillator) Yes (High precision, High speed : 40MHz, Low speed : 125kHz) Yes (High precision, High speed : 40MHz, Low speed : 125kHz) Yes 1/n (n=1, 2, 4, 8, 16) Wait/Stop Yes													
	PLL			-	-											
	Subclock															
Clock	Real Time clock															
CIOCK	On-Chip Oscillator															
	Oscillation Stop Detection	Yes (High precision, High speed : 40MHz, Low speed : 125kHz)           Yes           1/n (n=1, 2, 4, 8, 16)           Wait/Stop           Yes           Yes (Voltage detection 2)           10-bit × 12           Yes														
	Frequency Divider	Yes (High precision, High speed : 40MHz, Low speed : 125kHz)           Yes           1/n (n=1, 2, 4, 8, 16)           Wait/Stop           Yes           Yes (Voltage detection 2)           10-bit x 12           Yes														
	Power Save		1/n (n=1, 2, 4, 8, 16)           Wait/Stop           Yes           Yes (Voltage detection 2)           10-bit × 12													
Power Supply	Power-On Reset/POR		Yes (High precision, High speed : 40MHz, Low speed : 125kHz) Yes Yes Ves Wait/Stop Yes (Voltage detection 2) 10-bit × 12 Yes 3 (Timer RA, Timer RB, Timer RE)													
Voltage Detection	Low Voltage Detection/LVD															
A/D Converter	Resolution × Channels		2 circuits (Main dock, On-chip oscillator)													
	Sample and Hold		16 × 16 + 32->32           16 × 16 + 32->32           2 circuits (Main clock, On-chip oscillator)           -           -           -           Yes           Yes           Yes           1/n (n=1, 2, 4, 8, 16)           Wait/Stop           Yes           Yes (Voltage detection 2)           10-bit × 12           Yes           3 (Timer RB, Timer RE)           2 (Timer RD)           9 (shared with Timer RD)           9 (shared with Timer RD)           1 (with automatic starting function and clock source protection function)													
D/A Converter	Resolution × Channels															
	8-bit	2 circuits (Main clock, On-chip oscillator)														
	16-bit															
	Input Capture															
	Output Compare	1/n (n=1, 2, 4, 8, 16)         Wait/Stop         Yes         Yes (Volage detection 2)         10-bit × 12         Yes         2         Yes         3 (Timer RA, Timer RB, Timer RE)         2 (Timer RD)         8 (shared with Timer RD)         9 (shared with Timer RD, Timer RE)         7 (shared with Timer RD)														
Timer	PWM Output			7 (shared with Tin	ner RB, Timer RD)											
	Real-Time Port			-	-											
	Event Counter			1 (shared wi	th Timer RA)											
	2-Phase Encoder Input			-	-											
	3-Phase Inverter Control			1 (shared wi	th Timer RD)											
Watchdog Timer			1 (wit	h automatic starting function a	nd clock source protection fun	ction)										
	Clock Sync./ Clock Async.			1 (UA	.RT0)											
Serial Interface	Clock Sync. Only			-	-											
1201	Clock Async. Only			1 (UA	RI1)											
I-C-bus	0			1 (snared with Synchronous	Serial Communication Unit)											
Synchronous Senai	Communication Unit/Special Serial I/O			1 (snared	with FC)											
CAN	Channels Massage Dev (Numbers)				<u> </u>											
	Insut Only (Numbers)			I	0											
	CMOS I/O (Numbers)				1											
I/O Porto	N Channel Open Drain Part (Numbers)			4	-											
1/O FOILS	High Current Drive Port				_											
	Righ Current Drive Port			-	-											
Extornal Interrup	ta Ring			4	,											
Debugging					5 26											
Eunction	On-Board Elash Brogram				20											
Othor	BOM Correction Function				-											
Functions	Others															
Operating Freque	ency/Supply Voltage			20MHz/3.0 to 5.5V	10MHz/2 7 to 5 5V											
Operating Ambie	ent Temperature (°C)			_ 40	to 85											
Package*2				PI OPOr	48KB-A											
Lonago				. EQT 00												
Part No.		- Ves (PD code check function, PDM code protect function) RBC Core 88 88 89 80 80 80 80 80 80 80 80 80 80 80 80 80														

\*F F Hash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

	(1100		.,		,							_		1											
Group							R80	2/24											R8C	25					
	ROM (Bytes)		16K		24	K		32K		48	3K	64	ΙK	1	6K + 2ł	<	24K -	2K	3	2K + 2I	К	48K	+ 2K	64K	+ 2K
	RAM (Bytes)		1K				2K			2.	5K	3	K		1K				2K			2.5	5K	3	K
Memory	ROM Type*1												1	=											
	Data Flash							-											Yes	(2K)					
	Program Security									Yes (I	D code	check fi	unction	ROM	code pro	tect fur	nction)								
	CPU												R8C	Core											
	Basic Instructions												8	9											
CPU	Minimum Instruction Execution Time (ns)												50 (@2	20MHz)											
	Multiplier												16 × 1	6→32											
	Multiply-Accumulate Instruction											1	6×16·	+ 32→3	2										
	Clock Generation Circuit									3 ci	rcuits (I	Main clo	ock, Sub	o clock,	On-chip	oscilla	tor)								
	PLL												-	-											
	Subclock												'es (32.	768kHz	:)										
Clock	Real Time clock												Yes (Tir	mer RE)	)										
	On-Chip Oscillator	<u> </u>							Ye	es (High	i precisi	on, Hig	h speed	1:40MF	Hz, Low	speed	125kHz	:)							
	Oscillation Stop Detection	<u> </u>											Ye	es											
	Frequency Divider	<u> </u>										1/n	i (n=1, 2	2, 4, 8,	16)										
	Power Save	<u> </u>											Wait	Stop											
Power Supply	Power-On Reset/POR	<u> </u>											Ye	es											
voltage Detection	Low Voltage Detection/LVD	<u> </u>										Yes (	Voltage	detecti	on 3)										
A/D Converter	Resolution × Channels												10-bi	t×12											
B/1 0	Sample and Hold												Ye	es											
D/A Converter	Resolution × Channels												-	-	-	-									
	8-bit										3	I imer H	RA, Tim	er RB,	l imer R	E)									
	16-bit											0 ( )	2 (1 im	er RD)											
	Input Capture	<u> </u>		_								8 (sn	ared wi	th Time	r HD)										
<b>T</b>	Output Compare	<u> </u>									9 (	shared	with Tin	ner HD,	Timer F										
Timer	PWM Output		(shared with Timer RD) - 1 (shared with Timer RA)																						
	Real-Time Port		1 (shared with Timer RA)																						
	Event Counter		1 (shared with Timer RA) —																						
	2-Phase Encoder Input		(stared with Timer RA)																						
Match do a Timor	3-Phase Inverter Control																								
watchdog Timer	Clock Supp / Clock Apurp								T (WIL	nauton	iatic sta	rung iur			K SOUICE	e protec	uon iun	uon)							
Corial Interface	Clock Sync./ Clock Async.											2		, UANI	1)										
Senai Internace	Clock Sylic. Only																								
I <sup>2</sup> C-bus	Clock Asyric. Only									1 (sh:	ared wit	h Synch	ironous	Sorial	Commu	nication	( I Init)								
Synchronous Serial	Communication Unit/Special Serial I/O									1 (5110	area wit	1	(sharor	with I <sup>2</sup>	C)	noatioi									
oynomonouo oonar	Channels											·	-	_	•/										
CAN	Message Box (Numbers)												-	_											
	Input Only (Numbers)													3											
	CMOS I/O (Numbers)												4	1											
I/O Ports	N-Channel Open Drain Port (Numbers)												-	-											
	High Current Drive Port	1											1	3											
	Pull-Up Resistor	1											4	1											
External Interrup	ots Pins									-			1	3											
Debugging	On-Chip Debug												Ye	es											
Function	On-Board Flash Program												Ye	es											
Other	ROM Correction Function												-	-											
Functions	Others	1											-	_											
Operating Frequ	ency/Supply Voltage	1								20MH	z/3.0 to	5.5V, 1	0MHz/2	2.7 to 5.	5V, 5MH	Iz/2.2 t	5.5V								
Operating Ambig	ant Tomporatura (°C)	- 40	20	to 95	- 40	- 20	- 40		20 to 9	c .	40	to 95	- 20	- 40	200	to 95	- 40	- 20	- 40		20 to 9	-	- 40	- 20	- 40
Operating Amble	ent temperature ( C)	to 85	- 20	10 85	to 85	to 85	to 85		20 10 8	0	- 40	10 65	to 85	to 85	- 20	10 65	to 85	to 85	to 85		20108	5	to 85	to 85	to 85
		-	-			r		-				~			_			~			_				
			4		1			A-4			<				A-4			IA-I			A-4		4		
Package*2		52	64.		2	251		64J			C L	221			64.0			52,			640		5	2	
		8	0		2	3		00			6	3			00			00			00		6	3	
		ğ	길		č	ž					č	ž						ğ					č	Š	
		Ē	<u>م</u>		ā	E		Ŀ.			ā	E			Ŀ.			Ē			Ŀ.				
		e.	U.	<u>d</u>	<u>a</u>	e.	e.	Ű	<u>e</u>	<u>e</u>	<u>d</u> .	d.	<u>d</u>	e.	Ű	<u>0</u>	<u>A</u>	e.	<u>A</u>	<u>0</u>	U	<u>A</u>	<u>A</u>	<u>0</u>	<u>d</u>
Part No		SDF	SNL	SNF	SDF	SNF	SDF	SNL	SNF	SNF	SDF	SDF	SNF	3DF	SNL	SNF	SDF	SNF	SDF	SNF	SNL	SNF	SDF	SNF	SDF
		44	44	44	45	45	46	46	46	475	47	48	48	545	545	54	555	555	565	565	565	575	225	58	585
		212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212
		35F	SF.	SF.	SF.	35F	35F	SF.	SF.	SF.	35F	35F	35F	35F	35F	35F	35F	SF	SF.	35F	35F	35F	35F	35F	15F
		- E	- E	<u> </u>	- C	Œ	Œ	Œ	Ē	Œ	Ē	Œ	Œ	- E	ш.	Œ	Œ	Œ	Œ	Ē	ш.	Ē	Ē	Ē	Ē

#### • Specifications (R8C/Tiny Series)

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (R8C/Tiny Series)

ROM (Bytes)         8K         16K         24K         32K         8K+2K         16K+2K         24K+2K         32K+2K         8K           RAM (Bytes)         512         1K         1.5K         512         1K         1.5K         512         1K         512         512         1K         512         512         1K         512         1K         512	16K         8K + 2K         16K +           1K         512         1K           -         Yes (2K)         Yes (2K)														
RAM (Bytes)         512         1K	— Yes (2K)														
Memory         ROM Type*1         F           Data Flash         -         Yes (2K)         Second Secon	- Yes (2K)														
Inclusive         Inclusive <thinclusive< th="">         Inclusive         <thinclusive< th="">         Inclusive         Inclusive</thinclusive<></thinclusive<>	- Yes (2K)														
Detail rest         Test (Ar)           Program Security         Yes (ID code check function, ROM code protect function)           CPU         R8C Core           Basic Instructions         89           Minimum Instruction Execution Time (ns)         50 (@ 20MHz)           Multiplier         16 × 16 + 32           Multiplier         16 × 16 + 32 - 32           Clock Generation Circuit         3 circuits (Main clock, Sub clock, On-chip oscillator)           PLL         -           Subclock         Yes (32.768kHz)           Clock         Yes (Time RE)	I IES (2K)														
CPU         R8C Core           Basic Instructions         89           Multiply-Accumulate Instruction         16 × 16 + 32           Multiply-Accumulate Instruction         16 × 16 + 32 - 32           PL         -           Subclock         Yes (32.768kHz)           Clock         Yes (32.768kHz)															
CPU         Hol Core           Basic Instructions         89           CPU         Minimum Instruction Execution Time (ns)         50 (@ 20MHz)           Multiplier         16 × 16 → 32           Multiply-Accumulate Instruction         16 × 16 → 32           Multiply-Accumulate Instruction         16 × 16 → 32 → 32           Multiply-Accumulate Instruction         16 × 16 → 32 → 32           Multiply-Accumulate Instruction         16 × 16 → 32 → 32           Multiple-Accumulate Instruction         16 × 16 → 32 → 32           Multiple-Accumulate Instruction         16 × 16 → 32 → 32           Multiple-Accumulate Instruction         16 × 16 + 32 → 32           PL         -           Subclock         Yes (32.768kHz)           Real Time clock         Yes (Timer RE)															
Basic Instructions         B9           CPU         Minimum Instruction Execution Time (rs)         50 (@20MHz)           Multiplier         50 (@20MHz)           Multiply-Accumulate Instruction         16 × 16 → 32           Multiply-Accumulate Instruction         16 × 16 → 32 → 32           Clock Generation Circuit         3 circuits (Main clock, Sub clock, On-chip oscillator)           PLL         -           Subclock         Yes (32.768kHz)           Clock         Yes (Time RE)           Clock         Yes (Time RE)															
CPU         Minimum instruction Secution Time (ins)         50 (@20MH2)           Multiply-Accumulate Instruction         16 × 16 + 32           Multiply-Accumulate Instruction         16 × 16 + 32 - 32           Clock Generation Circuit         3 circuits (Main clock, Sub clock, On-chip oscillator)           PLL         -           Subclock         Yes (32.768kHz)           Real Time clock         Yes (Timer RE)															
Multiplier         16×16→32           Multiply-Accumulate Instruction         16×16+32→32           Clock Generation Circuit         3 circuits (Main clock, Sub clock, On-chip oscillator)           PLL         -           Subclock         Yes (32.768kHz)           Real Time clock         Yes (Timer RE)															
Clock Generation Circuit         16 × 16 + 32 → 32           Very State         3 circuits (Main clock, Sub clock, On-chip oscillator)           PLL         -           Subclock         Yes (32.768kHz)           Real Time clock         Yes (Timer RE)															
Clock Generation Circuit 3 circuits (Main clock, Sub clock, On-chip oscillator) PLL															
PLL     -       Subclock     Yes (32.768kHz)       Real Time clock     Yes (Timer RE)															
Subclock         Yes (32.768kHz)           Real Time clock         Yes (Timer RE)															
Clock Real Time clock Yes (Timer RE)															
Un-Chip Oscillator Yes (High precision, High speed : 40MHz, Low speed : 125kHz)															
Oscillation Stop Detection Yes															
Frequency Divider 1/n (n=1, 2, 4, 8, 16)															
Power Save Wait/Stop															
Power-On Reset/POR Yes															
Voltage Detection Low Voltage Detection/LVD Yes (Voltage detection 3)															
Besolution × Channels 10-bit × 12	10-bit × 4														
A/D Converter Sample and Hold Yes	Yes 														
Dia Converter Beschitton y Channels	3 (Timer RA, Timer RB, Timer RE) 1 (Timer RC)														
2/15 Convolution A Containing State Stat															
	Yes              3 (Timer RA, Timer RB, Timer RE)           1 (Timer RC)           4 (shared with Timer RC)           5 (shared with Timer RE)														
10-bit 1 (inter RC)	1 (Timer RC) 4 (shared with Timer RC) 5 (shared with Timer RC, Timer RE)														
	4 (shared with Timer RC) 5 (shared with Timer RC, Timer RE) 4 (shared with Timer RB, Timer RC)														
S (shared with Timer RE)	4 (shared with Timer RC) 5 (shared with Timer RC, Timer RE) 4 (shared with Timer RB, Timer RC)														
Timer PWM Output 4 (shared with Timer HB, Timer HC)	3 (Timer RA, Timer RB, Timer RE) 1 (Timer RC) 4 (shared with Timer RC) 5 (shared with Timer RC, Timer RE) 4 (shared with Timer RB, Timer RC)														
Real-Time Port -	3 (Timer RA, Timer RB, Timer RE) 1 (Timer RC) 4 (shared with Timer RC) 5 (shared with Timer RC, Timer RE) 4 (shared with Timer RB, Timer RC) 														
Event Counter 1 (shared with Timer RA)															
2-Phase Encoder Input –															
3-Phase Inverter Control –															
Watchdog Timer 1 (with automatic starting function and clock source protection function)															
Clock Sync./ Clock Async. 2 (UART0, UART1)	1 (UART0)														
Serial Interface Clock Sync. Only -															
Clock Async. Only –	1 (UART1)														
I <sup>2</sup> C-bus 1 (shared with Synchronous Serial Communication Unit)															
Synchronous Serial Communication Unit/Special Serial I/O 1 (shared with I <sup>2</sup> C)															
Channels –															
CAN Message Box (Numbers)															
Inut Only (Numbers)															
CMOSI/O (Humbers) 25	13														
V/O Porte N/O (Valmed) One Data (Multiply)	10														
Horistian Horistian Britan Toristian Bart															
	10														
Pull-up Hesistor 25	13														
External interrupts Pins 7															
Debugging On-Chip Debug Yes															
Function On-Board Flash Program Yes															
Other ROM Correction Function -															
Functions Others -															
Operating Frequency/Supply Voltage 20MHz/3.0 to 5.5V, 10MHz/2.7 to 5.5V, 5MHz/2.2 to 5.5V															
	- 20 to 85 - 40 - 20 - 40 to 85														
to 85 2 to 85 to 8	to 85 to 85														
Package*2 PLQP0032GB-A	PLSP0020JB-A														
outure 5F21282S0FP 5F21282S0FP 5F21282S0FP 5F21284S0FP 5F21285S0FP 5F21285S0FP 5F21285S0FP 5F21285S0FP 5F21274S0FP 5F21274S0FP 5F21275S0F	1282SNSP 1284SNSP 1282SNSP 1282SNSP 1282SNSP 1282SNSP 1284SDSP														

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

opeen				,			/						_				_	_													
Group								R	8C/2/	4													R	3C/2	3						
	ROM (Bytes)		4	8K			64K				96K			12	8K			48K	+ 2K		(	4K + 2	К		96	( + 2K			128K	+ 2K	
	RAM (Bytes)		2.	.5K			ЗK				7K			7.	5K			2.5	5K			ЗK				7K			7.	5K	
Memory	ROM Type*1															F															
	Data Flash								-														Ye	s (2K	)						
	Program Security											Yes (I	ID coo	de che	ck fur	ction,	ROM	code	protec	t func	tion)										
	CPU															R8C	Core														
	Basic Instructions															8	9														
CPU	Minimum Instruction Execution Time (ns)														5	0(@2	OMH:	<u>z)</u>													
	Multiplier															16×1	6→32	2													
	Multiply-Accumulate Instruction	1													16	× 16 +	32-	32													
	Clock Generation Circuit											3 c	circuits	s (Mai	n cloc	k, Sub	clock	, On-	chip os	cillate	or)										
	PLL																-														
	Subclock														Ye	s (32.	768kH	łz)													
011	Real Time clock														Ye	s (Tin	ner R	E)													
CIOCK	On-Chip Oscillator										Ye	s (Higl	h prec	cision,	High	speed	: 401	1Hz, L	.ow spe	ed :	125kF	z)									
	Oscillation Stop Detection															Ye	s														
	Frequency Divider														1/n (	n=1, 2	2, 4, 8	, 16)													
	Power Save	1														Wait/	Stop														
Power Supply	Power-On Reset/POR									_						Ye	es .														_
Voltage Detection	Low Voltage Detection/LVD									_				)	es (Vo	oltage	deteo	tion 3	i)												
	Resolution × Channels	1														10-bit	× 12		,												
A/D Converter	Sample and Hold															Ye	s														
D/A Converter	Resolution × Channels															8-bit	×2														
	8-bit													3 (Tin	ner R4	. Tim	er RR	. Time	er RE)												
	16-bit													4 (Tin	her R(	. Tim	er RD	Time	er BF)												
	Input Capture											1	13 (sh	ared v	vith Ti	ner B	C Tir	ner Rl	D Time	r BF)											
	Output Compare											14 (ch	ared	with T	mor F	C Tir	nor R	D Tim	or BE	Time	r BF)										
Timor	PW/M Output											1	0 (ch	arod y	vith Ti	nor P	B Tin	Dor D	Timo												
TIME	Pool-Timo Port		- 1 (shared with Timer RA)																												
	Event Counter	-	1 (shared with Timer RA)																												
	2 Rhase Encoder Input		1 (shared with Timer RA) —																												
	2 Phase Inverter Central	-	1 (shared with Timer RD)																												
Watabdag Timor	3-Friase Inverter Control	-	1 (shared with Timer RD)																												
watchdog Timer	Clash Cons / Clash Asses										T (with	auton	natics	startin	g lund	uon a		DTO	urce pr	otect	on iu	cuon)									
0	Clock Sync./ Clock Async.	<u> </u>													3 (0/	ARTU		R12)													
Serial Interface	Clock Sync. Only																-														
1201	Clock Async. Unly	<u> </u>										4.6.1					-			12.5.5.1	1.20										
I-C-bus	0	-										1 (sn	ared v	with S	ynchro	onous	Seria	Com	imunica	ation	Unit)					_	_				
Synchronous Serial	Communication Unit/Special Serial I/O	<u> </u>													1 (S	nared	with	FC)								_	_				
CAN	Channels																-														
	Message Box (Numbers)																-														
	Input Only (Numbers)															2	2														
	CMOS I/O (Numbers)															5	5														
I/O Ports	N-Channel Open Drain Port (Numbers)																-														
	High Current Drive Port															8	3														
	Pull-Up Resistor															5	5														
External Interrup	ts Pins															6	3														
Debugging	On-Chip Debug															Ye	s											_			
Function	On-Board Flash Program															Ye	s														
Other	ROM Correction Function																-														
Functions	Others																-														
Operating Freque	ency/Supply Voltage											20MF	lz/3.0	to 5.5	V, 10	/Hz/2	.7 to	5.5V, s	5MHz/2	.2 to	5.5V										
Operating Ambie	ent Temperature (°C)	- 2	20 to	1 _	40 to	85	- 20		- 40		- 20	-	40	-	20	- 40	- 1	20	_	40 tr	85		_ 5	0 to 9	15		_ 40	to 85		-2	20
- portaing randle		8	35	1		~	to 8	5	to 85	1	to 85	to	85	to	85	to 85	to	85								_				to	35
		4	Ą	Y-	Ă	4		Ā	4	4	< 4		Ă			A-1		Ą	A-1	<b>ج</b>	4-	٩ ·	5	Å	Y-	Ą	4	ج ا	A-1	Ă	A-1
*1		B B	19	- B	8	0		Æ	d B B	19	2 5		9			g		- 22	g	딸	g	2   3	5	Æ	dg	19	₫	192	¶ B	99	gA
Package <sup>**2</sup>		120	04	064	964	190		964	064	190	5   5		964			90		90	100	8	964	2 2	5	964	64	064	64	64	964	90	90
		ğ	N N	۲ d	POC			POC	DO L	1 OC	S   S		DQ DQ			20		ğ	õ	ğ	PO	ĕ   à	5	20	1 M	P O C	N N	N N	P O C	N N	20
		g	g	2	g	<u> </u>		g	9	9	3   3		g			g		g	2	g	g	3   9	Ž	g	g	g	g	g	g	g	g
			۵.	_ ₽_	۵.	<u>م</u>		۵.	۵		. 🗠		۵.			٩.		₽.	₽.	٩.	۵.	r (	-	۵.	_ ₽	_	_ ₽_		٩.	₽.	٩
												*	+	*	*	*					-					*		*	*	*	
		F.	L L	FA.	Ъ	F,	FA			L L	E Į	L L	L L	E E	FA	FA	FA'	Ъ	FA'	d l	FA			: 6	E A	ЦЦ	FA	L L	FA	ЪР	FA
Part No.		SN	SN I	SD	SD	SD	SN	NS C	SD	Z	NSN NS	SD	SD	SN	SN	SD	SN	SN	SD	S	SD	S S			SN SN	SD	SD	SD	SD	SN	SN
		A7	A7	A7	A7	A8	AB	A8	A A	A	A	¥	AO	AC	AC	AC	B7	B	B7	81	8	89 6	3 8	AA	BA	BA	BA	B	BC	B	BC
		212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	212	10	210	212	212	212	212	212	212	212
		5F	5F	5F	5F	2E	12F	E SF	EF 01	2E	2E	25	2E	5F	5F	5F	5F	SF:	SF:	2E	12L	1 21		L L	5F	5F	2E	5F	5F	5F	5F
		1	1	1	Ē	E	Œ			1	- L CC	<u>۳</u>	1	<u>۳</u>	<u>م</u>	Æ	£	Ē	œ	Œ	Œ	I [ [		. α		1	1	L CC	Œ	Œ	Œ

### • Specifications (R8C/Tiny Series)

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (R8C/Tiny Series)

Group		R8C/2C									R8C/2D							
	ROM (Bytes)	48	ВK	6	4K	96	5K	12	8K	48K	+ 2K	64K	+ 2K	96K	+ 2K	128K	+ 2K	
Memory	BAM (Bytes)	2.	5K	3	K	7	K	7.	5K	2	5K	3	K	7	'K	7.	5K	
	BOM Type*1		F															
	Data Flash					_							Vas	(2K)				
	Program Security						Vas (I	D code che	ck function	BOM code	nrotect fu	nction)	103	(210)		-		
	CPU						105 (1	D couc one		Coro		nouony						
	Basic Instructions								1100	0010								
CRU	Minimum Instruction Execution Time (no)								E0 (@/	20MU-7)								
CFU	Multiplier	00 (250m 2) 16 k 16-32																
	Multiplier								1 × 01	10→32								
	Multiply-Accumulate Instruction	3 circuits (Main clock Sub clock Duckin oscillator)																
Clock	Clock Generation Circuit						30	ircuits (iviai	n clock, Sul	D CIOCK, UN	-cnip oscilla	llor)						
	PLL																	
	Subclock	165 (22.7 00ATZ)																
	Real Time clock						Mar all a		Yes (1)	mer RE)		105111.)	-			-	-	
	On-Chip Oscillator					_	Yes (High	n precision,	High speed	d : 40MHz, I	Low speed	: 125kHz)			_			
	Oscillation Stop Detection																	
	Frequency Divider	1/n (n=1, 2, 4, 8, 16)																
	Power Save	wait/Stop																
Power Supply	wer Supply Power-On Reset/POR								Y	es								
Voltage Detection Low Voltage Detection/LV		Yes (Votage detection 3)																
A/D Converter	Resolution × Channels	10-bit × 20																
	Sample and Hold	Yes																
D/A Converter	Resolution × Channels		8-bit × 2															
Timer	8-bit	3 (Timer RA, Timer RB, Timer RE)																
	16-bit							4 (Tin	ner RC, Tim	ner RD, Tim	er RF)							
	Input Capture						1	3 (shared v	vith Timer F	RC, Timer R	D, Timer R	F)						
	Output Compare						14 (sh	ared with T	imer RC, Ti	mer RD, Tir	ner RE, Tin	ner RF)						
	PWM Output						1	0 (shared v	vith Timer F	RB, Timer R	C, Timer RI	D)						
	Real-Time Port																	
	Event Counter	1 (shared with Timer RA)																
	2-Phase Encoder Input								-	_								
	3-Phase Inverter Control							1	(shared wi	th Timer R	D)							
Watchdog Timer						1	(with auton	natic startin	g function a	and clock so	ource protect	ction functio	n)					
	Clock Sync./ Clock Async.								3 (UARTO	to UART2)								
Serial Interface	Clock Sync. Only								-	-								
	Clock Async. Only								-	-								
l <sup>2</sup> C-bus							1 (sha	ared with S	ynchronous	Serial Con	nmunication	n Unit)						
Synchronous Serial Communication Unit/Special Serial I/O									1 (shared	d with I <sup>2</sup> C)								
Channels									-	-								
CAN	Message Box (Numbers)								-	-								
I/O Ports	Input Only (Numbers)	2																
	CMOS I/O (Numbers)	71																
	N-Channel Open Drain Port (Numbers)	-																
	High Current Drive Port	8																
	Pull-Up Resistor	71																
External Interrupts Pins		8																
Debugging	On-Chip Debug												-					
Function	On-Board Flash Program								Y	es								
Other	BOM Correction Function																	
Functions	Others																	
Operating Frequency/Supply Voltage							20MH	Iz/3 0 to 5 5	V 10MHz/2	2 7 to 5 5V	5MHz/2.2.t	o 5 5V						
Operating Ambient Temperature (°C)		- 20	1		- 20	- 40	- 20	- 40	- 20	_ 40	- 20	- 40			- 40	- 20	- 40	
		- 20 to 85 - 40 to 85		to 85	to 85	= 20 to 85	- 40 to 85	to 85	- 40 to 85	to 85	= 40 to 85	- 20	to 85	to 85	to 85 to 85 to			
Package*2			1						PLOP00	180KB-A			1					
Part No.		F212C7SNFP*	F212C7SDFP*	F212C8SDFP*	F212C8SNFP*	F212CASDFP*	F212CASNFP*	F212CCSDFP*	F212CCSNFP*	F212D7SDFP*	F212D7SNFP*	F212D8SDFP*	F212D8SNFP*	F212DASNFP*	F212DASDFP*	F212DCSNFP*	F212DCSDFP*	
		35	35	R5	R5	H5	R5	R5	H5	35	R5	R5	35	35	H5	H5	35	

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code
00000									
Group			R8C	C/2E			R80	C/2F	
	BOM (Bytes)	8	K	16	3K	8K -	+ 2K	16K	+ 2K
	DAM (Butes)		10	4		010	10	1010	
	RAIVI (Bytes)	5	12	1	n .	5	12	1	n
Memory	ROM Type*1					-			
	Data Flash		-	-			Yes	(2K)	
	Program Security			Yes (I	D code check function.	ROM code protect fur	nction)		
	CPU				B8C	Core			
	Basic Instructions					0			
0.011	Dasic Instructions				50 ( 0)	3			
CPU	Minimum Instruction Execution Time (ns)				50 (@2	20MHZ)			
	Multiplier				16×1	6→32			
	Multiply-Accumulate Instruction				16×16 ·	+ 32→32			
	Clock Generation Circuit				2 circuits (Main cloc	k, On-chip oscillator)			
	PLL				-	-			
	Subclock				-				
	Bult								
Clock	Real Time clock								
	On-Chip Oscillator			Yes (High	n precision, High speed	: 40MHz, Low speed	: 125kHz)		
	Oscillation Stop Detection				Ye	es			
	Frequency Divider				1/n (n=1, 2	2, 4, 8, 16)			
	Power Save				Wait	Stop			
Davies Conselo	Power-On Resot/POP				V				
Voltage Detection	Law Valtage Detection (LVD					datastica ()			
Voltage Detection	Low voltage Detection/LVD				Yes (Voltage	detection 2)			
A/D Converter	Resolution × Channels				10-bi	t×12			
	Sample and Hold				Ye	es			
D/A Converter	Resolution × Channels				8-bi	t×2			
	8-bit				3 (Timer BA, Tim	er BB. Timer BE)			
	16-bit				1 (Tim	or PC)			
	Insut Casture				4 (abased wi	t Times DO			
	Input Capture				4 (shared wi	(n Timer RC)			
	Output Compare				5 (shared with 1 in	ner RC, Timer RE)			
Timer	PWM Output				4 (shared with Tin	ner RB, Timer RC)			
	Real-Time Port				-	-			
	Event Counter				1 (shared wi	th Timer RA)			
	2-Phase Encoder Input				-	_			
	3-Phase Inverter Control				-	_			
Watabdag Timor				1 (with outom	atio starting function o	nd alaak aauraa proto	tion function)		
watchuog miner				i (with auton	ialic starting function a	The clock source protect	aon function)		
	CIOCK SYNC./ CIOCK ASYNC.				1 (U <i>F</i>	(HTU)			
Serial Interface	Clock Sync. Only				-				
	Clock Async. Only				-	-			
I <sup>2</sup> C-bus					-	-			
Synchronous Serial	Communication Unit/Special Serial I/O				-	-			
	Channels				-	_			
CAN	Message Box (Numbers)				-	_			
	Input Only (Numbers)					2			
	input Only (Numbers)				,	-			
	CIVIOS I/O (Numbers)				2	5			
I/O Ports	N-Channel Open Drain Port (Numbers)				-	-			
	High Current Drive Port				1	3			
	Pull-Up Resistor				2	5			
External Interrup	ots Pins				-	7			
Dobugging	On-Chin Debug				Y	20			
Eunction	On-Board Elash Program				V	20			
	DOM Correction Function								
Other	ROM Correction Function								
FUNCTIONS	Others				compar	ator×2			
Operating Frequ	ency/Supply Voltage				20MHz/3.0 to 5.5V,	10MHz/2.7 to 5.5V			
Operating Ambie	ent Temperature (°C)	- 40 to 85	- 20 to 85	- 40 to 85	- 20 to 85	- 40 to 85	- 20 to 85	- 40 to 85	- 20 to 85
Package*2					PLQP00	32GB-A			
Part No.		212E2DFP**	212E2NFP**	212E4DFP**	212E4NFP**	212F2DFP**	212F2NFP**	212F4DFP**	212F4NFP**
		35 F	35F	15F	35F	35 F	35 F	35 F	35 F

### • Specifications (R8C/Tiny Series)

\*' F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (R8C/Tiny Series)

Group				R8C	/2G				R8C	/2H			R80	C/2J	
	ROM (Bytes)	16	δK	24	ιK	32	2K	4	к	8	K	2	ĸ	4	ĸ
	RAM (Bytes)	51	12		1	К		25	56	38	34	25	6	38	34
Memory	ROM Type*1							ŀ							
	Data Flash							-	-						
	Program Security					Yes	s (ID code ch	eck function,	ROM code p	protect function	on)				
	CPU							R8C	Core						
	Basic Instructions							8	9						
CPU	Minimum Instruction Execution Time (ns)							125 (@	8MHz)						
	Multiplier							16×1	6→32						
	Multiply-Accumulate Instruction							16×16-	+ 32→32						
	Clock Generation Circuit				2 circu	its (Sub clock	, On-chip os	cillator)				1	circuit (On-o	chip oscillator	)
	PLL							-	-						
	Subclock			Yes (32.	768kHz)				Yes (32.	768kHz)			-	-	
Clock	Real Time clock					Yes (Tin	ner RE)						-	-	
CIOCIC	On-Chip Oscillator					Yes (H	High precisio	n, High spee	d : 8MHz, Lo	w speed : 12	5kHz)				
	Oscillation Stop Detection								-						
	Frequency Divider							1/n (n=1, 2	2, 4, 8, 16)						
	Power Save							Wait	Stop						
Power Supply	Power-On Reset/POR							Ye	es						
Voltage Detection	Low Voltage Detection/LVD							Yes (Voltage	detection 3)						
A/D Converter	Resolution × Channels							-	-						
	Sample and Hold							-	-						
D/A Converter	Resolution × Channels							-	-						
	8-bit				3 (T	imer RA, Tim	er RB, Timer	RE)					2 (Timer RA	, Timer RB)	
	16-bit							1 (Tim	er RF)						
	Input Capture							4 (shared wi	th Timer RF)						
	Output Compare				2 (sh	ared with Tim	ner RE, Time	r RF)					1 (shared wi	th Timer RF)	
Timer	PWM Output							1 (shared wi	th Timer RB)						
	Real-Time Port								-						
	Event Counter							1 (shared wi	th Timer RA)						
	2-Phase Encoder Input								-						
	3-Phase Inverter Control								-						
Watchdog Timer						1 (with aut	tomatic starti	ng function a	nd clock sou	rce protection	n function)				
	Clock Sync./ Clock Async.					2 (UARTO	), UART2)					I	1 (UA	(RT0)	
Serial Interface	Clock Sync. Only								-						
1201	Clock Async. Only								-						
PU-bus									-						
Synchronous Serial	Communication Unit/Special Senai 1/0														
CAN	Magazana Day (Numbers)														
	Message Box (Numbers)														
	Chaos I/O (Numbers)				0				-	0				0	
I/O Danta	N Charged Orga Data Data (Numbers)			2	8				-	0		I	1	2	
I/O Ports	N-Channel Open Drain Port (Numbers)														
	Right Current Drive Fort				0					e					
Extornal Interrup	ta Rina			2	8				1	0		Ļ		2	
External Interrup	On-Chip Dobug				5			v	20			0			
Eunction	On-Board Elash Brogram							V	*5						
Other	POM Correction Eurotion								-						
Functions	Othors						omparator v	2 (charod wit	h voltago mo	nitor 1 and 3	)				
Operating Freque	ency/Supply Voltage						8MH	$\frac{2}{7}$ 2 7 to 5 5V	4MHz/2 2 to	5.5V	)				
Operating Ambig	ant Tomporature (°C)	- 40 to 95	- 20 to 85	- 40 to 95	- 20 to 85	- 40 to 85	- 20 to 85	40 to 95	- 20 to 95	- 40 to 85	- 20 to 85	- 40 to 95	- 20 to 85	- 40 to 95	- 20 to 85
Package*2	ant temperature ( C)	- 40 10 05	- 20 10 05	PI OP00	32GB-A	- 40 10 05	- 20 10 05	- 40 10 05	- 20 10 05	- 40 10 05	PI SP00	120 IB-A	- 20 10 05	- 40 10 05	- 20 10 03
Part No.		Yes (Voltage detection 3)												212J1SNSP**	
		35 F.	35 F.	35 F.	35 F.	35 F.	35F;	35 F.	35 F.	35 F.	35 F.	35 F.	35 F.	35 F.	35 F.

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

- opeen			(03)						
Group			R80	C/2K			R80	C/2L	
	ROM (Bytes)	8	К	16	бК	8K -	+ 2K	16K	+ 2K
	RAM (Bytes)	1	К	1.	5K	1	К	1.5	δK
Memory	ROM Type*1			1		=			·
,	Data Flash		-	_			Yes	(2K)	
	Program Security			Yes (I	D code check function.	ROM code protect fur	nction)		
	CPU				R8C	Core			
	Basic Instructions				8	9			
CPU	Minimum Instruction Execution Time (ns)				50 (@2	20MHz)			
	Multiplier				16×1	6→32			
	Multiply-Accumulate Instruction				16×16 ·	+ 32→32			
	Clock Generation Circuit				2 circuits (Main cloc	k, On-chip oscillator)			
	PLL				-	_			
	Subclock				-	_			
Clash	Real Time clock				-	_			
CIOCK	On-Chip Oscillator			Yes (High	precision, High speed	1:40MHz, Low speed	: 125kHz)		
	Oscillation Stop Detection				Ye	es			
	Frequency Divider				1/n (n=1, 2	2, 4, 8, 16)			
	Power Save				Wait	/Stop			
Power Supply	Power-On Reset/POR				Ye	es			
Voltage Detection	Low Voltage Detection/LVD				Yes (Voltage	detection 3)			
	Resolution × Channels				10-b	it×9			
AD Converter	Sample and Hold				Ye	es			
D/A Converter	Resolution × Channels				-	-			
	8-bit				2 (Timer RA	, Timer RB)			
	16-bit				3 (Timer RC	, Timer RD)			
	Input Capture				12 (shared with Tir	ner RC, Timer RD)			
	Output Compare				12 (shared with Tir	ner RC, Timer RD)			
Timer	PWM Output			1	0 (shared with Timer R	B, Timer RC, Timer RI	)		
	Real-Time Port				-	-			
	Event Counter				1 (shared wi	th Timer RA)			
	2-Phase Encoder Input					-			
	3-Phase Inverter Control				1 (shared wi	th Timer RD)			
watchdog Timer				1 (with autom	latic starting function a	ind clock source protec	ction function)		
Carial Interferes	Clock Sync./ Clock Async.				2 (UARTO	), UART2)			
Serial Interface	Clock Sync. Only								
l <sup>2</sup> C-bus	CIOCK ASYIC: Only								
Synchronous Serial	Communication Unit/Special Serial I/O					_			
oynomonouo oonar	Channels					_			
CAN	Message Box (Numbers)				-	_			
	Input Only (Numbers)					3			
	CMOS I/O (Numbers)				2	5			
I/O Ports	N-Channel Open Drain Port (Numbers)				-	_			
	High Current Drive Port				1	3			
	Pull-Up Resistor				2	5			
External Interrup	its Pins				-	7			
Debugging	On-Chip Debug				Ye	es			
Function	On-Board Flash Program				Ye	es			
Other	ROM Correction Function				-	_			
Functions	Others				-	_			
Operating Freque	ency/Supply Voltage			20MH	z/3.0 to 5.5V, 10MHz/2	2.7 to 5.5V, 5MHz/2.2 to	o 5.5V		
Operating Ambie	ent Temperature (°C)	- 40 to 85	- 20 to 85	- 40 to 85	- 20 to 85	- 40 to 85	- 20 to 85	- 40 to 85	- 20 to 85
Package*2					PLQP00	32GB-A			
Part No.		5F212K2SDFP**	5F212K2SNFP**	5F212K4SDFP**	5F212K4SNFP**	5F212L2SDFP**	5F212L2SNFP**	5F212L4SDFP**	5F212L4SNFP**
		Ě	Ĕ	Ě	Ě	Ĕ	Ě	Ĕ	Ě

## • Specifications (R8C/Tinv Series)

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

Automotive MCUs

### • Specifications (M32C/80 Series)

Group											M32	C/84 (	M32C/	'84T)										
	ROM (Bytes)		128K			256k	<			32	0K			38	4K			384K	+ 4K			512K	+ 4K	
Momony	RAM (Bytes)		10K			20K			4							24	1K				-			
Memory	Data Flash								-											Yes	(4K)			
	Program Security							-	-								Yes (ID	Code 0	Check F	unction	, ROM C	Code Pr	otect Fu	nction)
	CPU				_							M32C/	80 Core											
	Basic Instructions Minimum Instruction Execution Time (ns)											1	08 32MH7	)										
CPU	Multiplier											16 × 1	6→32	)										
	Multiply-Accumulate Instruction										1	6×16	+ 48→4	8										
	Barrel Shifter											Y	es											
DMA	DMAC (Channels)							DMAC	III (Star	tun Pos	sciblo wi	th All D	4 oriphor	al Euroct	ion Into	rrupt C								
	Address Space (Bytes)							DIVIAC	ii (Stai	tup Fos	SIDIE WI		–		Ion me	inupi C	auses)							
External Bus	External Bus Interface												-											
Expansion	Bus Structure											-	_											
	DRAM Controller								4 circ	uits (Ma	in clock	PIL	- Sub clor	k On-c	hin osc	illator)								
	PLL								4 0110			Y	es	sk, on c	anp 030	inatory								
	Subclock											Y	es											
Clock	RTC												_								-			
	On-Chip Oscillator											Y	es											
	Frequency Divider									1/n	(n=1, 2	. 3. 4. 6	es 6. 8. 10.	12, 14,	16)									
	Power Save										<b>X</b>	Wait	/Stop		- /									
Power Supply	Power-On Reset/POR												-											
voltage Detection	Low Voltage Detection/LVD	40.1.11		40.1.1	40.1.1			40.1.1					-			40.1.1								
	Resolution × Channels	× 34	10-bit × 26	×34	×26	10-bit ×	34	10-bit ×26	10-bi	t×34	10-bi	$t \times 26$	×34	10-bi	t × 26	10-bit ×34	10-bit	×26		10-bi	t×34		10-bit	×26
A/D Converter	Sample and Hold											Y	es											
	Multi-Channel Sample and Hold												-											
D/A Converter	Resolution × Channels		8-bit × 2 																					
	16-bit																							
	Input Capture																							
	Output Compare																							
Timer	PWM Output			8 (Intelligent VO) 8 (Intelligent VO) 13 (Timer A, Intelligent VO)																				
	Event Counter										11	(Timer	A Time	r B)										
	2-Phase Encoder Input										3 (Time	r A) + 1	(Intellig	gent I/O	)									
	3-Phase Inverter Control							1 (shar	ed with	Timer A	A4, Time	er A1, T	imer A2	2, Timer	B2, De	ad Time	e Timer)							
Watchdog Timer	Clash Cura / Clash Asura										C (11		1											
Serial Interface	Clock Sync. / Clock Async.										0 (0	(Intelli	aent I/C	))										
	Clock Async. Only												_	/										
I <sup>2</sup> C-bus												5 (U	ART)											
IEBus Smart Card/SIM												5 (U	ARI)											
Synchronous Serial	Communication Unit/Special Serial I/O											5 (U	ART)											
CAN	Channels												1											
CAN	Message Box (Numbers)											1	6											
IrDA CBC Calculation	Circuit									1 (	CBC_C	CITT	- × <sup>16</sup> ⊥ × <sup>1</sup>	<sup>2</sup> ± X <sup>5</sup> ±	1))									
X/Y Converter	- Circuit										0110-0	Y Y	es .	<u> </u>	1))									
	Input Only (Numbers)												1											
	CMOS I/O (Numbers)	121	85	121	85	121		85	1:	21	8	5	121	8	5	121	8	5		12	21		85	5
I/O Ports	N-Channel Open Drain Port (Numbers)												2											
	Pull-Up Resistor	121	85	121	85	121		85	1:	21	8	5	121	8	5	121	8	5		12	21		85	5
External Interrup	ots Pins											1	1											
Debugging	On-Chip Debug							-												Ye	es			
Other	On-Board Flash Program BOM Correction Euroction								-											Ye	es -			
Functions	Others												_				L							
Operating Freque	ency/Supply Voltage										32	2MHz/4	.2 to 5.9	5V										
Operating Ambie	ent Temperature (°C)	- 40	- 40 - 40	-	40 to 10	05	- 40	to 85	- 40	- 40	to 85	- 40	- 40	- 40	- 40	- 40	- 40	- 40	- 40	- 40	- 40	- 40	- 40	- 40
		10 85	10 105 10 85					<u> </u>	10 105			10 105	10 85	10 105	10 85	10 105	10 85	10 105	10 85	10 105	10 85	10 105	10 85	10 105
			-	_	_	_		-								-					-			
		4-4	(B-/	A-A		(A-P		(B-/		+		ģ	4-4	ę		(A-4	d d				+		E-4	j
Package*2		144	1001	144	100	144		1001		44			144			144				14.44	44		00	5
		Pod													DEC	2								
		PLO	PLG	PLO	PLO	PLO		PLO		2			PLO		2	PLO		3			2			1
					*	*			*			*				*								
		GP	GP GP	(GP	KGP	XGP	GP	GP	XGP	GP	GP	XGP	GP	(GP	GP	(GP								
		XX	XXX	×.	×-	XX-	XX	XXX	XX-	××:	××	XX-	XX	XX.	XXX	×.	d.	d.	с,	d.	٩	<u>0</u>	٩	<u>0</u>
Part No.		ACT-	ACU ACT-	VCU.	1GU	VGU	AGT-	AGT-	MN	TWL	TWL	MN	HT	AHU.	L H	AHU.	HTG	NUH	HTG	UH:	JTG	nuc:	JTG	ากด
		342N	340N	342N	343N	345N	345N	343N	345N	345N	343N	343N	345N	343N	343N	345N	343F	343F	345F	345F	345F	345F	343F	343F
		M306	M306 M306	M306	M306	M306	M308	M306	M306	M306	M306	M306	M306	M306	M306	M306	M306	M306	M306	M306	M306	M306	M306	M306

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

\*: New product \*\*: Under development

## • Specifications (M32C/80 Series)

Group												M32	C/85 (	M32C	/85T)										
	ROM (Bytes)		25	6K			32	0K			320K	+ 4K			38	4K			384K	+ 4K			512K	+ 4K	
	RAM (Bytes)		2	ОK											24	1K									
Memory	ROM Type*1				N						F	-			N	Л						-			
	Data Flash									Ves (ID	res Code C	(4K)	inction							Ves (ID	Code C	(4N)	unction		
	Program Security				-					ROM	Code Pre	otect Fu	nction)		-	-				ROM C	ode Pr	otect FL	inction)		
	CPU												M32C/	B0 Core	)										
	Basic Instructions	<u> </u>											1	08	->										
CPU	Multiplier	<u> </u>											16 × 1	32IVIFI2 6→32	<u>()</u>										
	Multiply-Accumulate Instruction											1	6×16	+ 48→4	18										
	Barrel Shifter												Y	es											
DMA	DMAC (Channels)								DMAG	NII (Ctor	tun Doo	oible wi	+b All D	4 orinhor	ol Eurot	ion Into	rrupt C								
	Address Space (Bytes)								DIVIA	ii (Stai	tup Fos	SIDIE WI		-	ai Funci	ion inte	inupi Ga	iuses)							
External Bus	External Bus Interface												-	-											
Expansion	Bus Structure												-	-											
	DRAM Controller									4 circi	uite (Ma	in clock		- Sub clo	ck On-c	hin occ	illator)								
	PLL									4 0100	uns (ivia		., T LL, V	es	ck, OII-C	nip osc	illator)								
	Subclock												Y	es											
Clock	RTC	L	_										-	-											
	On-Chip Oscillator												Y	es											
	Frequency Divider										1/n	(n=1, 2	. 3. 4. 6	5. 8. 10.	12, 14,	16)									
	Power Save												Wait	/Stop		- /									
Power Supply	Power-On Reset/POR												-	-											
voltage Detection	Low Voltage Detection/LVD	10 bit	10 bit	10 bit			10 bit	10 bit	10 bit	10 bit			10 hit	-											
	Resolution × Channels	×26	× 34	×26	10-bit	× 34	×26	×34	×26	× 34	10-bi	t×26	×34	10-b	it×26		10-bi	t × 34			10-bi	t × 26		10-bi	it×34
A/D Converter	Sample and Hold												Y	es											
D/A Convertor	Multi-Channel Sample and Hold																								
DIA CONVENCI	8-bit		8-bit x 2 - 11 (Timer A, Timer B) 2 (Intelligent I/O)																						
	16-bit											11	(Timer	A, Time	er B)										
	Input Capture											8	8 (Intelli	gent I/C	<u>)</u>										
Timer	Output Compare	<u> </u>										13 (Ti	l (Intelli mor Δ	gent I/C	) ant I/O)										
Timer	Real-Time Port											13 (11		-	int 1/0)										
	Event Counter											11	(Timer	A, Time	er B)										
	2-Phase Encoder Input										;	3 (Time	r A) + 1	(Intelli	gent I/O	)									
Watebdog Timor	3-Phase Inverter Control								1 (shar	ed with	Timer A	A4, Time	er A1, T	imer A2	2, Timer	B2, De	ad Time	Timer)							
Wateridog Timer	Clock Sync./ Clock Async.											6 (U	ART, In	telligen	t I/O)										
Serial Interface	Clock Sync. Only											1	(Intelli	gent I/C	D)										
l <sup>2</sup> C-bus	Clock Async. Only												5 (11												
IEBus													5 (U	ART)											
Smart Card/SIM													5 (U	ART)											
Synchronous Serial	Communication Unit/Special Serial I/O	—											5 (U	ART)											
CAN	Message Box (Numbers)												16	×2											
IrDA													-		0 6										
CRC Calculation	Circuit										1 (	CRC-C	CITT ()	K <sup>10</sup> + X <sup>1</sup>	² + X° +	1))									
X/1 Converter	Input Only (Numbers)												1	1											
	CMOS I/O (Numbers)	85	121	85	12	1	85	121	85	121	8	5	121	8	35		12	21			8	5		12	21
I/O Ports	N-Channel Open Drain Port (Numbers)													2											
	Pull-Up Resistor	85	121	85	12	1	85	121	85	121	8	5	121	- 8	35		1:	21			8	5		12	21
External Interrup	ts Pins												1	1											
Debugging	On-Chip Debug	L			_						Ye	es			-	_					Ye	es			
Function	On-Board Flash Program				V						Ye	es -			-	-					Ye	es			
Functions	Others					5							-	_											
Operating Freque	ency/Supply Voltage											32	2MHz/4	.2 to 5.	5V										
Operating Ambie	ent Temperature (°C)	- 40	- 40	to 85	- 40	- 40	to 85	- 40 t	o 105	- 40	- 40	- 40	- 40	to 105	- 40	- 40	- 40	- 40	– 40 t	o 105	- 40	- 40	- 40	- 40	- 40
		10 103			10 103					10 05	10 103	10 05			10 05	10 103	10 05	10 103			10 103	10 05	10 103	10 05	10 105
		∢	∢	∢			∢	٨	∢	∢		4	∢		∢			¢				4		<	<
Deales = *2		KB-A         KA-A         KA-A           KB-A         KA-A         KA-A           KB-A         KB-A         KB-A           KB-A         KB-A         KB-A           KB-A         KB-A         KB-A														-YA									
гаскауе		0100 01441 0100 01441 0100 01441 0100 01441 0100 00000 0000 0000 0														410									
														Č	2										
														ā	1										
		*d	<u>0</u> _	<u>d</u>	*d	d.	d.	*d5	*d5					*d	۹.	*d	<u> </u>								
		XX	XXG	XXG	XX	XX	XX	XXX	XXX	0		0	٩	XXC	XXG	XXX	XXG	0	0		0				
Part No.		(-DE	X-TE	Х-ТЕ	K-DE	X-1/V	X-LV	NU-	NU-	ИG	VUG	ИС	NUG	Â-Ţ	X÷Ļ	Â-Ĵ-	X	IUG	ITGF	TGF	IUG	TGP	UGF	TGP	UGF
		33M	55M(	33MG	55M	55M)	33M)	55M	33MV	55FV	33FV	33FV	55FV	33M	33M	55M	55M	55FF	55FF	53FF	33FH	53FJ	53FJ	55FJ	55FJ
		3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085	3085
		ž	ž	ž	ž	ž	ž	ž	ž	ž	ž	ž	ž	ž	Ξ	ž	ž	ž	ž	ž	ž	ž	ž	ž	ž

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

Automotive MCUs

## • Specifications (M32C/80 Series)

Group							M32C/88 (	M32C/88T)					
	ROM (Bytes)		320K	+ 4K			384K	. + 4K			512K	( + 4K	
	RAM (Bytes)						18	3K -					
wemory	Data Flash						Yes	- (4K)					
	Program Security					Yes (ID Code C	heck Function	, ROM Code Pr	rotect Function	)			
	CPU						M32C/8	30 Core					
	Basic Instructions						10	08					
CPU	Minimum Instruction Execution Lime (ns)						31.3 (@ 16 × 1	32MHZ) 6→32					
	Multiply-Accumulate Instruction						16 × 16	+ 48→48					
	Barrel Shifter						Y	es					
DMA	DMAC (Channels)							4					
	DTC/DMACII				DMAG	CII (Startup Pos	sible with All P	eripheral Funct -	ion Interrupt C	auses)			
External Bus	External Bus Interface							_					
Expansion	Bus Structure						-	-					
	DRAM Controller						-	-					
	Clock Generation Circuit					4 circuits (Mai	in clock, PLL, S	Sub clock, On-c	chip oscillator)				
	Subclock						Y	es				-	
Clask	RTC							-					
CIOCK	On-Chip Oscillator						Y	es					
	Oscillation Stop Detection						Y	es	( *)				
	Frequency Divider					1/n	(n=1, 2, 3, 4, 6) Wait	i, 8, 10, 12, 14, /Stop	16)				
Power Supply	Power-On Reset/POR						-	-					
Voltage Detection	Low Voltage Detection/LVD						-	-		-			
	Resolution × Channels	$10$ -bit $\times 26$	10-bit  imes 34	$10$ -bit $\times 26$		10-bit $ imes$ 34		10-bi	t × 26	10-bit $ imes$ 34	10-bi	t × 26	10-bit × 34
A/D Converter	Sample and Hold Multi-Channel Sample and Hold						Y	es -					
D/A Converter	Resolution × Channels						8-bi	t×2					
	8-bit						-	-					
	16-bit						11 (Timer	A, Timer B)					
	Input Capture						8 (Intelli 8 (Intelli	gent I/O)					
Timer	PWM Output						13 (Timer A.	Intelligent I/O)					
	Real-Time Port												
	Event Counter						11 (Timer	A, Timer B)					
	2-Phase Encoder Input				1 (shar	od with Timor A	3 (Timer A) + 2	(Intelligent I/O	) B2 Doad Tim	Timor)			
Watchdog Timer					1 (51141		A, HINELAT, I	1	DZ, Deau Time				
	Clock Sync./ Clock Async.						6 (UART, In	telligent I/O)					
Serial Interface	Clock Sync. Only						1 (Intelli	gent I/O)					
l <sup>2</sup> C-bus	Clock Async. Unly						5 (1)						
IEBus	·						5 (U	ART)					
Smart Card/SIM							5 (U	ART)					
Synchronous Serial	Communication Unit/Special Serial I/O						5 (U	ART)					
CAN	Message Box (Numbers)						16	> × 3					
IrDA	[							-					
CRC Calculation	n Circuit					1 (0	CRC-CCITT ()	$X^{16} + X^{12} + X^5 +$	1))				
X/Y Converter							Y	es					
	CMOS I/O (Numbers)	85	121	85		121		1 8	5	121	6	15	121
I/O Ports	N-Channel Open Drain Port (Numbers)	00					:	2					
	High Current Drive Port						-	-					
Extornel later	Pull-Up Resistor	85	121	85		121		1 8	5	121	8	35	121
External Interrup	On-Chin Debug						Y	1					
Function	On-Board Flash Program						Y	es					
Other	ROM Correction Function						-	-					
Functions	Others						-	-					
Operating Freque	ency/Supply voltage	- 40 to 105	- 40	to 85	- 40 to 105	- 40 to 85	32MHZ/4 - 40 t	.2 to 5.5V	- 40	to 85	- 40 to 105	- 40 to 85	- 40 to 105
Operating Amble		40 10 100		10 00	40 10 100	401000	401		1 40	0.00	40 10 100	401000	40 10 100
		∢	<	∢		<			<	▲		<	▲
**		ц Ц	KĄ-	ц Ц Ц		KĄ-		5	b ≤	Υ Υ Υ		± ∠	KA K
Раскаде**		100	144	100		144				144			144
		aPc	aPc	aPo		apo			2	ap c		10	QPC
		L L	P	- L		L L		ā	1		i	L L	L L
Port No.		UGF	TGP	TGF	UGF	ЦGР	JGP	JGP	IGP	GP	IGP	GP	GP
Fart NO.		PW	ΡW	NFW	EW.	H	EHL	DEHL	EHU	FJ	FJU	IFJT	FJU
		3880	0882	3880	3882	3882	3882	3880	3880	3882	3880	3880	3882
		M3(	M3(	M3(	M3(	M3(	M3(	M3(	W3(	M3(	M3(	M3(	M3(

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

## • Specifications (M16C/60 Series)

Group					M16C/62P (	M16C/62PT)			
	ROM (Bytes)	48K	64K	64K + 4K	96K	128K	128K + 4K	384K	+ 4K
	RAM (Bytes)		4K	1	5K	10	Ж	31	IK
Memory	ROM Type*1	N	A.	F		N		F	
	Data Flash			Yes (4K)		_	Vaa	Yes (4K)	tion
	Program Security	-	-	ROM Code Protect Function)		-	RO	M Code Protect Funct	ion)
	CPU				M16C/	60 Core			
	Basic Instructions				ę	91			
CPU	Minimum Instruction Execution Time (ns)		-	-	41.7 (@	24MHz)			
	Multiplier Multiply-Accumulate Instruction				16×1	6→32			
	Barrel Shifter				10×10	-			
DMA	DMAC (Channels)					2			
DIVIA	DTC/DMACII								
	Address Space (Bytes)					_			
External Bus Expansion	External Bus Interface								
	DRAM Controller				· · ·				
	Clock Generation Circuit			4 circi	uits (Main clock, PLL,	Sub clock, On-chip osc	illator)		
	PLL				Y	es			
	Subclock				Y	es			
Clock	RIC On Chin Oppillator								
	Oscillation Stop Detection				Y	es			
	Frequency Divider				1/n (n=1,	2, 4, 8, 16)			
	Power Save				Wait	/Stop			
Power Supply	Power-On Reset/POR					_			
Voltage Detection	Low Voltage Detection/LVD					-			
A/D Converter	Sample and Hold				0-01 V	1×20			
AD COnverter	Multi-Channel Sample and Hold					_			
D/A Converter	Resolution × Channels			-	8-b	t×2			
	8-bit					-			
	16-bit				11 (Timer	A, Timer B)			
	Input Capture					-			
Timer	PWM Output				5 (Tir	ner A)			
	Real-Time Port								
	Event Counter				11 (Timer	A, Timer B)			
	2-Phase Encoder Input			4.7.1	3 (Tir	ner A)			
Watchdog Timer	3-Phase Inverter Control			1 (snared with	Timer A4, Timer A1, T	Imer A2, I Imer B2, De	ad Time Timer)		
Wateridog Timer	Clock Sync./ Clock Async.				3 (U	ART)			
Serial Interface	Clock Sync. Only				2 (5	6I/O)			
	Clock Async. Only					_			
I*C-bus					3 (U	ART)			
Smart Card/SIM					1 (U	ART)			
Synchronous Serial	Communication Unit/Special Serial I/O				3 (U	ART)			
CAN	Channels					-			
URI	Message Box (Numbers)					_			
IrDA CPC Calculation	Circuit			-		$(16 + V^{12} + V^5 + 1))$			
X/Y Converter	Girdan				1 (0110-0111)	-			
	Input Only (Numbers)					1			
	CMOS I/O (Numbers)				8	15			
I/O Ports	N-Channel Open Drain Port (Numbers)					2			
	Pull-Un Resistor			-	5	-			
External Interrup	its Pins				1	1			
Debugging	On-Chip Debug	-	-	Yes				Yes	
Function	On-Board Flash Program	-	-	Yes		-		Yes	
Other	ROM Correction Function	Ye	es	-	Y	es		_	
Operating Freque	ency/Supply Voltage				24MHz/4	0 to 5 5V			
Operating Ambie	ent Temperature (°C)				- 40	to 85			
					4			4	ج.
Packago*2								S BB	EXE BX
1 ackage								010	0100
				i (	ī.			d D	a a
					<u> </u>			4	
		P-	0		0	۵.			
		8 N N	8 NG		NO NO	9X)			
5		X:	× ×	GP	X'	X-1	TGP	<u>н</u>	GP
Part No.		.9WC	.8W	5F81	MA	WC	EC.	E	E
		162C	162C	162C	162C	162A	162A	162.1	162.1
		W3C	W3C	M30	W3G	M3G	M3C	M3C	M3C

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

Automotive MCUs

### • Specifications (M16C/60 Series)

Group													M16C	/62A	(M160	C/62T)											
	ROM (Bytes)	32K		64	ιK										128K										25	6K	
Momony	RAM (Bytes)	ЗK		4	K	М						5	К								10K		F		20	)K	
Memory	Data Flash					101								-	-												
	Program Security									-									Yes (I	D Code	Chec	k Func	tion, R0	DM Co	de Prot	ect Fun	ction)
	CPU Basic Instructions													M16C/6	50 Core	9											
CPU	Minimum Instruction Execution Time (ns)												6	2.5 (@	16MH:	z)											
CFU	Multiplier													16×1	6→32												
	Multiply-Accumulate Instruction Barrel Shifter												10	5 × 16 -	+ 32→: -	32	-										
DMA	DMAC (Channels)													2	2												
DMA	DTC/DMACII														-												
External Bus	External Bus Interface																										
Expansion	Bus Structure													-	-												
	DRAM Controller											2	ircuite	- (Main (	- Nock 9	Sub clo	ck)										
	PLL											21	incuits	(1912111)	-	500 010	ur)										
	Subclock													Ye	es												
Clock	RTC On-Chin Oscillator																										
	Oscillation Stop Detection													-	_												
	Frequency Divider												1/n	(n=1, 2	2, 4, 8,	16)											
Power Supply	Power Save Power-On Reset/POR													Wait	Stop												
Voltage Detection	Low Voltage Detection/LVD																										
	Resolution × Channels													10-bi	$t \times 26$												
A/D Converter	Sample and Hold Multi-Channel Sample and Hold													- Ye	- -												
D/A Converter	Resolution × Channels													8-bi	t×2												
	8-bit													-	- • T:												
	Input Capture																										
	Output Compare			- 5 (Timer A) 3 (Timer A) 5 (																							
	PWM Output Roal Time Port	3 (Timer A)	5 (Tim	5 (Timer A)       3 (Timer A)       3 (Timer A)       \$ (Timer A)														ner A)									
	Event Counter			5 (Timer A)       3 (Timer A)       3 (Timer A)       3 (Timer A)       3 (Timer A)       5 (Timer A)       3 (Timer A)       5 (Timer A)																							
Timer	2-Phase Encoder Input	2 (Timer A)	3 (Tim	11 (Timer A, Timer B)           3 (Timer A)         2 (Timer A)         3 (Timer A)         2 (Timer A)         3 (Timer A)														ner A)									
	3-Phase Inverter Control	-	Interview     Interview       A)     3 (Timer A)     2 (Timer A)       1     (shared with Timer A4, Timer A2, Timer A2, Timer B2, Dead Time Timer)     1     1       1     (shared with Timer A4, Timer A4, Timer A2, Timer B2, Dead Time Timer)     1     1       1     (shared with Timer A4, Timer A4, Timer A2, Timer B2, Dead Time Timer)     1     1														er A4, imer B2 er)	2,									
Watchdog Timor			Tim	er)			Tim	ner)				Timer)			Timer)												
Watehoog Hinei	Clock Sync./ Clock Async.	2 (UART)	3 (UA	RT)	2 (UA	RT)	3 (U/	ART)	2	2 (UAR	T)	3 (UART)	2 (U	ART)	3 (UART)	2 (UART)	3	UAR	Г)	2 (U/	RT)			3 (U	ART)		
Serial Interface	Clock Sync. Only	4.04070								(114.5)	<b>T</b> )		1.01	2 (S	I/O)	4 GUADTA				1.4.01	DT)						
I <sup>2</sup> C-bus	Clock Async. Only	T (UART)			T (UA	RI)				I (UAR	1)		1 (0/	1 (U	ART)	[ I (UAHI)				1 (0/	RT)						
IEBus														1 (U	ART)												
Smart Card/SIM	Communication Unit/Special Serial I/O													1 (U	ART)				_								
CAN	Channels													-	_												
CAN	Message Box (Numbers)														-												
CRC Calculation	Circuit											1 (0	RC-C	CITT ()	- ( <sup>16</sup> + X	<sup>12</sup> + X <sup>5</sup>	+ 1))										
X/Y Converter														-	_												
	Input Only (Numbers)	68	84		68		8	5		68		85	6		85	68		85		6	3	1			15		
I/O Ports	N-Channel Open Drain Port (Numbers)	00					0	0				00		2	2	00		00			, 	1					
	High Current Drive Port		01		00		0	r		<u></u>		05		-	-	60		05									
External Interrup	ts Pins	8	11		8	)	1	1		8		11	8	3	11	8		11		6	5			1	1		
Debugging	On-Chip Debug									-													Yes				
Function	On-Board Flash Program									- Vas													Yes				
Functions	Others									100				-	_												
Operating Freque	ency/Supply Voltage				16MHz	/4.2 to	5.5V			-			16	MHz/4	.5 to 5.	5V						16MF	lz/4.2 t	o 5.5V			
Operating Ambie	ent Temperature (°C)	- 40 to 85	- 40 to 125	- 40	to 85	– 40 t	o 125	- 40	to 85	-	40 to 1	25	- 40 to 85	- 40 to 125	- 40	to 85	- 40 to 125	-	40 to 8	35	- 40 1	to 105	-40	to 85	- 40 to 105	- 40 to 85	- 40 to 105
Package*2		PRQP0080JA-A	PROP0100.IB-A		PROP0080JA-A					PRQP0080JA-A		PRQP0100JB-A			PRQP0100JB-A	PRQP0080JA-A		PRQP0100JB-A					PRQP0100JB-A	PLQP0100KB-A	PRQP0100JB-A	PLQP0100KB-A	PRQP0100JB-A
Part No.		M30623M4T-XXXGP	M30622M8V-XXFP	M30622M8T-XXXFP	M30623M8T-XXXGP	M30623M8V-XXXGP	M30622MCV-XXXFP	M30622MCT-XXXFP	M30623MCT-XXXGP	M30623MCV-XXXGP	M30623ECVGP	M30622ECVFP	M30623ECT-XXXGP	M30623ECV-XXXGP	M30622ECTFP	M30623ECTGP	M30622ECV-XXXFP	M30622ECT-XXXFP	M30620FCT-XXXFP	M30621FCTGP	M30621FCUGP	M30620FCUFP	M30620FCTFP	M30624FGT-XXXGP	M30624FGUFP	M30624FGTGP	M30624FGU-XXXFP

\*' F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Q : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/60 Series)

Group					,				M160	C/6N4											M160	C/6N5			
	DOM (D. L)		- 10	01/			1001/	416				01/			05.01/	414			10	01/			1001/	414	
	ROM (Bytes)		12	8K	-	V	128K	+ 4K			25	6K	10	NK.	256K	+ 4K			128	BK	5	V V	128K	+ 4K	
	RAW (Bytes)			4	5	n		-				4	IC	n.						4	5	r.	F		
Memory	Data Elash	<u> </u>		_			Voc	(4K)				_			Voc					-			Voc (	414)	
	Data Hash					Vas (ID	Code C	heck Fi	Inction					Vas (ID	Code C	hock Fi	nction					Vas (ID	Code Cl	heck Fu	Inction
	Program Security		-	-		ROM	Code Pro	otect Fu	nction)		-	-		ROM	Code Pro	tect Fu	nction)		-	-		ROM C	ode Pro	tect Fur	nction)
	CPU												M16C/6	50 Core											
	Basic Instructions												9	1											
0.011	Minimum Instruction Execution Time (ns)												50 (@2	20MHz)											
CPU	Multiplier												16×1	6→32											
	Multiply-Accumulate Instruction											1	6×16-	⊦ 32→3	2										
	Barrel Shifter												-	-											
DMA	DMAC (Channels)												2	2											
	DTC/DMACII												-	-											
E	External Rua Interface	<u> </u>							Cupp	ort for i	oortion	of 1 to	2 woit c	vi	Jutouto	4 obin c	alaat a	apolo							
External Bus Expansion	Bus Structure		9	oloctabl	e from	Sonarat	o hus M	Multinle	bus F	ata Ru	s Width	can be	solocto	d (8/16-	bit) The	a numbe	elect si	yriais tout addr	ose hi	1909 001	n ha sa	lected (	12/16/20	0	
	DBAM Controller			cicotabi		ocpuiu	0 003, 1	iumpics	( Du3, L		5 WIGHT	can be	-	-	big, m	, 11011100	1 01 04	iput uuui	035 00	1303 04	11 00 30		12/10/20	·	
	Clock Generation Circuit									4 circi	uits (Ma	in clock	PLLS	Sub cloc	k. On-c	hip osci	llator)								
	PLL												Ye	es											
	Subclock												Ye	es											
Clash	RTC	1											-	-											
CIOCK	On-Chip Oscillator												Ye	es											
	Oscillation Stop Detection										_		Ye	es		_									
	Frequency Divider											1/1	n (n=1, 2	2, 4, 8, '	16)										
	Power Save												Wait/	Stop											
Power Supply	Power-On Reset/POR												-												
voltage Detection	Low voltage Detection/LVD	<u> </u>											10.1	-											
	Resolution × Channels												10-DI	1×20											
AVD COnverter	Multi-Channel Sample and Hold												-	-											
D/A Converter	Besolution × Channels		8-bit×2 																						
Birtoontoitoi	8-bit												-	-											
	16-bit											11	(Timer /	A, Time	r B)										
	Input Capture												-	-	,										
	Output Compare												-	-											
Timer	PWM Output												5 (Tin	ner A)											
	Real-Time Port												-	-	-										
	2 Rhass Encoder Input											11	(Timer /	A, Timei	rB)										
	3-Phase Inverter Control								1 (shar	ed with	Timer /	A Tim	or Δ1 Ti	mor Δ2	Timer	R2 Des	d Time	Timer)							
Watchdog Timer	o i nase inventer control		5 (Timer A, Timer B) 																						
	Clock Sync./ Clock Async.												3 (U/	ART)											
Serial Interface	Clock Sync. Only												1 (S	i/O)											
-	Clock Async. Only												-												
I <sup>c</sup> C-bus		<u> </u>											3 (U/	ART)											
Smart Card/SIM		——											3 (0/												
Synchronous Serial	Communication Unit/Special Serial I/O												3 (U)	ABT)											
	Channels								1	2			- (	,							1	1			
CAN	Message Box (Numbers)								16 -	+ 16											1	6			
IrDA													-	-											
CRC Calculation	Circuit				-						1 (	CRC-C	CITT ()	( <sup>16</sup> + X <sup>12</sup>	+ X <sup>5</sup> +	1))									
X/Y Converter																									
	CMOS I/O (Numbers)													5											
I/O Ports	N-Channel Open Drain Port (Numbers)												0	5											
1/01/01/13	High Current Drive Port												-	-											
	Pull-Up Resistor												8	5											
External Interrup	its Pins												1	1											
Debugging	On-Chip Debug	1	-	-			Ye	es			-	-			Ye	S			-	-			Ye	s	
Function	On-Board Flash Program		-	-			Ye	es			-	_			Ye	S			-	-			Ye	s	
Other	ROM Correction Function		Y	es				-			Y	es				-			Ye	es			_		
Functions	Others												-	-											
Operating Ambie	ant Temperature (°C)	- 40 1	to 85	_ 40 t	0 125	- 40 to 85	_ 40 t	0 125	_	40 to 8	15	- 40	125 10 125	_ 40	to 85	- 40 t	125	- 40 to 85	- 40 t	0 125	- 40 to 85	_ 40 t	0 125	- 40 1	to 85
oporating / more						10 10 00	.01	0.20		10 10 0		.0		10	.0 00	101		10 10 00		0 120	10 10 00		0 120		
			_	_			_	_		_		_		_		_		_			_		_		_
		6	B-	d d	4	Ę.	B-/	E,	H-	ď.		ĥ	l d	1B-/	B-4	4		8			H-		d d		<u>B</u> /
Package*2		ð	00	8 8	00	00 X	00	00 ¥	00	8	6	2	8 8	00	00 ×	0°		90 X			00		8 8		00
		6	P01	01	P01	-01	P01	201	P01	-01		5	01	P01	-01	P01		-01			P01		201		P01
		Ē	Å	Ē	ĝ	ē	В В	Ē	ğ	Ē		Ž	Ē	ğ	ГŐ	ğ		ğ			В		ē		В
														۵.		۵.									
													Ę.	GP	GP	£									
Part No.		No.	MCI	NC	NC	CT	No.	No.	CT	NG.	MG	NGN	NGN	GT	-GT	́Оц	١ ال	NG I	NC	MC	NC.	S I	S S	FCT	ECT
		1 Z	N41	N4	N4	N41	N4I	N4I	N41	N41	N41	N41	N41	N4I	SN41	N4	N41	ISN5	ISN51	SN51	SN51	ISN51	ISN5	ISN5	ISN51
		1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306	1306
		ž	Σ	ž	ž	ž	ž	ž	ž	ž	Σ	Σ	Σ	ž	ž	ž	ž	2	2	ž	ž	ž	2	2	ž
*1 F : Flash memo	ry version, L : ROM-less version,	M : Mas	k ROM	version	, O : Or	e time	PROM	version,	Qz:Q	ZROM	version									* : Ne	w prod	uct ★	r:Unde	r develo	opment

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Oz : OzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

Automotive MCUs

### • Specifications (M16C/60 Series)

Group			M160	C/6NK			M16C	/6NM	
	ROM (Bytes)	384K	+ 4K	512K	( + 4K	3848	( + 4K	512K	+ 4K
	RAM (Bytes)				31	К			
Memory	ROM Type*1				F				
	Data Elash				Yes	(4K)			
	Program Security			Yes (ID	Code Check Function	ROM Code Protect F	unction)		
	CPU				M16C/6	0 Core	,		
	Basic Instructions				9	1			
	Minimum Instruction Execution Time (ns)				50 (@2	OMHz)			
CPU	Multiplier				16×1	6→32			
	Multiply-Accumulate Instruction				16×16-	+ 32→32			
	Barrel Shifter				-	-			
D144	DMAC (Channels)				2	2			
DMA	DTC/DMACII				-	-			
	Address Space (Bytes)				-	-			
External Bus	External Bus Interface				-	-			
Expansion	Bus Structure				-	-			
	DRAM Controller				-	-			
	Clock Generation Circuit			4 circi	uits (Main clock, PLL, §	Sub clock, On-chip osc	cillator)		
	PLL				Ye	es			
	Subclock				Ye	es			
Clock	RTC				-	-			
CIOCK	On-Chip Oscillator				Ye	es			
	Oscillation Stop Detection				Ye	es			
	Frequency Divider				1/n (n=1, 2	2, 4, 8, 16)			
	Power Save				Wait	Stop			
Power Supply	Power-On Reset/POR				-	-			
Voltage Detection	Low Voltage Detection/LVD					-			
	Resolution × Channels				10-bi	t × 26			
A/D Converter	Sample and Hold				Ye	es			
	Multi-Channel Sample and Hold				-	-			
D/A Converter	Resolution × Channels				8-bi	t×2			
	8-bit				-	-			
	16-bit				11 (Timer J	A, Timer B)			
	Input Capture				-	-			
	Output Compare					-			
Timer	PWM Output				5 (Tin	ner A)			
	Real-Time Port				-	-			
	Event Counter				11 (Timer )	A, Timer B)			
	2-Phase Encoder Input				3 (1 in	ner A)			
	3-Phase Inverter Control			1 (shared with	Timer A4, Timer A1, T	mer A2, Timer B2, De	ad Time Timer)		
watchdog Timer					0.44				
Carial Interface	Clock Sync./ Clock Async.		0./0		3 (U)	ARI)	4.0		
Senai Interiace	Clock Sync. Only		2 (8	si/O)			4 (8	1/0)	
I <sup>2</sup> C buo	Clock Asylic. Offiy				2 /11				
IEBue					3 (0)				
Smart Card/SIM					1 (1)	ART)			
Synchronous Serial	Communication Unit/Special Serial I/O				3 (U	ABT)			
Cynonionous Serial	Channels				3 (0)	,			
CAN	Message Box (Numbers)				16	- 16			
IrDA	meeerage Dext (Hambere)					-			
CRC Calculation	Circuit				1 (CRC-CCITT ()	$(^{16} + X^{12} + X^5 + 1))$			
X/Y Converter						-			
	Input Only (Numbers)								
	CMOS I/O (Numbers)		8	5			1	11	
I/O Ports	N-Channel Open Drain Port (Numbers)					2			
	High Current Drive Port				-	-			
	Pull-Up Resistor		8	15			1.	11	
External Interrupt	ts Pins		1	1			1	4	
Debugging	On-Chip Debug				Ye	es			
Function	On-Board Flash Program				Ye	es			
Other	ROM Correction Function				-	-			
Functions	Others				-	-			
Operating Freque	ency/Supply Voltage				20MHz/4	2 to 5.5V			
Operating Ambie	nt Temperature (°C)	- 40 to 125	- 40	to 85	- 40 to 125	- 40 to 85	- 40 to 125	- 40 to 85	- 40 to 125
Package*2			PLQP0	IOOKB-A			PLQP01	28KB-A	
Part No.		M306NKFHVGP	M306NKFHTGP	M306NKFJTGP	M306NKFJVGP	M306NMFHTGP	M306NMFHVGP	M306NMFJTGP	M306NMFJVGP

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

### • Specifications (M16C/Tiny Series)

			-							-							
Group		M	16C/26A	(M16C/26	T)						M16	C/28					
	ROM (Bytes)	24K + 4K	48K + 4K	64K	+ 4K		6	4K			96	δK			96K	+ 4K	
	RAM (Bytes)	1K		2K			4	K					8	К			
	BOM Type*1			F						M					F		
Memory	Data Elash		Yes	(4K)						_					Yes	(4K)	
	Bala Fidoli	Voc	(ID Code (	Chock Euro	tion									Voc	(ID Code C	bock Eurod	tion
	Program Security	RO	M Code Pr	otect Functi	on)					-				RO	M Code Pro	otect Functi	ion)
	CPU				. ,				M16C/	60 Core							
	Basic Instructions								101100/	1							
	Minimum Instruction Execution Time (ns)	50 (@2		62.5 (@16MHz)	50 (@S		62.5 (@16MH+)	50 (@20MHz)	62.5.(@	16MHz)	50 (@ 20MHz)	62.5 (@16MHz)	50 (@20MHz)	62.5 (@16MHz)	50 (@20MHz)	62.5 (@16MHz)	50 (@20MHz)
CPU	Multiplier	50 (@Z	20101112)	02.5 (@100012)	50 (@2		02.3 (@100012)	JU (@ZUNIFIZ)	16 1		50 (@20MH2)	02.3 (18 10MHZ)	30 (@20MH2)	02.3 (@10MHZ)	50 (@20MH2)	02.3 (18 10MHZ)	00 (@20WIHZ)
	Multiplier								× 01	0732							
	Remail Chiftee								10 × 10	+ 32-732							
	Daner Sinner									0							
DMA	DMAC (Channels)									2							
	Address Cases (Putes)									-							
	Address Space (Bytes)									-							
External Bus	External Bus Intenace									_							
LAPAIISION	Bus Structure																
	DRAM Controller																
	Clock Generation Circuit						4 circ	uits (Main c	lock, PLL,	Sub clock, (	On-chip osc	illator)					
	PLL								Y	es							
	Subclock								Y	es							
Clock	RIC									_							
	On-Chip Oscillator								Y	es							
	Oscillation Stop Detection								Y	es							
	Frequency Divider								1/n (n=1,	2, 4, 8, 16)							
	Power Save								Wait	/Stop							
Power Supply	Power-On Reset/POR									-							
voltage Detection	Low Voltage Detection/LVD									-							
	Resolution × Channels		10-b	it × 12		10-bit × 16	10-bi	it × 27	10-bit × 16	10-bit × 27	10-bi	t×16		10-bit × 27		10-bit	1×16
A/D Converter	Sample and Hold								Y	es							
	Multi-Channel Sample and Hold								Y	es							
D/A Converter	Resolution × Channels									_							
	8-bit																
	16-bit								8 (Timer A	A, Timer B)							
	Input Capture										8 (Tin	ner S)					
	Output Compare			_							8 (Tin	ner S)					
Timer	PWM Output		5 (Tir	ner A)							13 (Timer )	A, Timer S)					
	Real-Time Port									-							
	Event Counter								8 (Timer A	A, Timer B)							
	2-Phase Encoder Input		3 (Tir	ner A)						3	(Timer A) -	1 (Timer S	5)				
	3-Phase Inverter Control					1 (s	shared with	Timer A4,	Timer A1, T	imer A2, Ti	mer B2, De	ad Time Tin	ner)				
Watchdog Timer										1							
	Clock Sync./ Clock Async.								3 (U	ART)							
Serial Interface	Clock Sync. Only					1 (SI/O)	2 (5	SI/O)	1 (SI/O)	2 (SI/O)	1 (S	I/O)		2 (SI/O)		1 (S	1/0)
.2	Clock Async. Only									-		.2					
I <sup>-</sup> C-bus			1 (U	ART)						2	(Multi mast	er I°C, UAR	T)				
IEBus									1 (U	ART)							
Smart Card/SIM									1 (U	ART)							
Synchronous Serial	Communication Unit/Special Serial I/O								1 (U	ART)							
CAN	Channels									-							
	Message Box (Numbers)									-							
IrDA									10	_							
CRC Calculation	Circuit						1 (CRC-0	CCITT (X <sup>10</sup>	+ X <sup>12</sup> + X <sup>5</sup> +	- 1)/CRC-1	6 (X <sup>10</sup> + X <sup>15</sup>	+ X <sup>2</sup> + 1))					
X/Y Converter										-							
	Input Only (Numbers)									-							
	CMOS I/O (Numbers)		3	39		55	7	71	55	71	5	5		71		5	5
I/O Ports	N-Channel Open Drain Port (Numbers)									_							
	High Current Drive Port									-	1						
	Pull-Up Hesistor		3	19		55	7	1	55	71	5	5		71		5	5
External Interrup	ts Pins								1	1							
Debugging	Un-Chip Debug		Y	es						_					Ye	es	
Function	On-Board Flash Program		Y	es						_					Ye	es	
Other	ROM Correction Function			_				)	les (Addres	is match × 2	2)					-	
Functions	Others									-							
Operating Freque	ency/Supply Voltage	20MHz/3	0 to 5.5V	16MHz/	20MHz/3	0 to 5.5V	16MHz/	20MHz/	16MHz/4	2 to 5.5V	20MHz/	16MHz/	20MHz/	16MHz/	20MHz/	16MHz/	20MHz/
- 1 · · · · · · · · · · · · · · · · · ·				4.2 to 5.5V			4.2 to 5.5V	3.0 to 5.5V			3.0 to 5.5V	4.2 to 5.5V	3.0 to 5.5V	4.2 to 5.5V	3.0 to 5.5V	4.2 to 5.5V	3.0 to 5.5V
Operating Ambie	nt Temperature (°C)	-40 to 85 -40 to 125 -40 to 85 -40 to 125 -4									- 40 to 85	- 40 to 125	- 40 to 85	- 40 to 125	- 40 to 85	- 40 to 125	40 to 85
												<	۲.				
		%         44         %         44         %         44         %         84										2	ė.				
Package*2		0080 0082 0082 0084 000 0084 000 0098 000 0098 000 0098 000 0098 000 0098 000 0098 000 000										19	10				
						ğ			D D D	POC	È			DO DO			2
				g		ğ		g	ğ	g		ž		g		G	ž
			i	r		Ē	Ĺ í	<u>г</u>	<u> </u>	<u> </u>				<u> </u>		ā	L
						무	E E	보	E E	HP	보	H H	HP				
		P	0	0	0	X	X	X	X	×.	X	8	X	0	0	0	
Part No		Ū	GF	/GF	10	×⊢	X->	×	X->	×->	×	×->	×÷	Ŧ	H	ΉF	Ë
. urt NO.		F3	F6	F8/	F81	W8	M8	W8	M8	MA	MA	MA	MA	FA	FAI	FA	FAI
		260	260	260	260	281	580	580	281	280	281	281	280	280	280	281	281
		1302	130	1302	130	302	1302	1302	1302	1302	1302	130	302	302	302	305	305
		≥	≥	≥	≥	≥	≥	≥	2	≥	≥	≥	≥	≥	≥	≥	≥

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

Automotive MCUs

## • Specifications (M16C/Tiny Series)

Group											M16	C/29									
	ROM (Bytes)		64	1K			9	6K			96K	+ 4K			12	8K			128K	+ 4K	
	RAM (Bytes)		4	К					8	к							12	2K			
Memory	ROM Type*'				N	- N					F	(412)			N	Λ			F		
	Data FidSh									Vas (II	Code C	(4K)	oction					Vos (I	Code C	heck Fur	oction
	Program Security				-	-				ROM	Code Pro	tect Fun	ction)		-	-		ROM	Code Pro	tect Fun	ction)
	CPU										M16C/6	0 Core									
	Basic Instructions										9	1									
CRU	Minimum Instruction Execution	50 (@2	(OMHz)	62.	5 (@16M	IHz)	50 (@:	20MHz)	62.5 (@16MHz)	50 (@20MHz)	62.5 (@16MHz)	50 (@20MHz)	62.	5 (@16M	Hz)	50	(@20MF	Hz)	62.5 (@16MHz)	50 (@20MHz)	62.5 (@16MHz)
010	Multiplier								(0.1011112)	(0200002)	16 × 1	( <i>→</i> 32							(01011112)	(02011112)	(0.1011112)
	Multiply-Accumulate Instruction										16×16 +	- 32→32									
	Barrel Shifter										-	-									
DMA	DMAC (Channels)										2	-									
	Address Space (Bytes)											-									
External Bus	External Bus Interface										-	-									
Expansion	Bus Structure										-	-									
	DRAM Controller										-	-	0								
	PLI							4	CIrcuits (	Main cloc	X, PLL, S	SUD CIOCK	, On-chip	oscillato	r)						
	Subclock										Ye	es									
Clock	RTC										_	-									
CIUCK	On-Chip Oscillator										Ye	s									
	Oscillation Stop Detection									- 1	Ye	S	2)								
	Power Save										Wait/	Stop	)								
Power Supply	Power-On Reset/POR											-									
Voltage Detection	Low Voltage Detection/LVD										-	-									
	Resolution × Channels	10-bit × 27	10-bi	t×16	10-bit × 27	10-bi	t×16		$10-bit \times 2$	7	10-bit	×16	10-bit × 27	10-bit × 16	10-bi	t×27	10-bit × 16	10-bit × 27	10-bit	×16	10-bit × 27
A/D Converter	Sample and Hold Multi-Channel Sample and Hold										Ye	es									
D/A Converter	Resolution × Channels										-	-									
	8-bit		6 (Timer A, Timer B)     8 (Timer S)																		
	16-bit		- Timer B) 8 (Timer A, Timer B) 8 (Timer S) 8 (Timer S)																		
	Input Capture		8 (Timer A, Timer B) 8 (Timer S) 8 (Timer S) 12 (Timer A Timer S)																		
Timer	PWM Output		8 (Timer A, Timer B) 8 (Timer S) 8 (Timer S) 13 (Timer A, Timer S)																		
	Real-Time Port		8 (Timer A, Timer B) 8 (Timer S) 8 (Timer S) 13 (Timer S) 																		
	Event Counter									8	(Timer A	, Timer E	3)								
	2-Phase Encoder Input								11. 777	3 (1	imer A) +	- 1 (Time	rS)	DUIT							
Watchdog Timer	3-Phase Inverter Control						1	(snared	with Time	er A4, Tin	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	mer A2,	Timer B2	, Dead II	me i ime	r)					
Trateridog Timer	Clock Sync./ Clock Async.										3 (UA	ART)									
Serial Interface	Clock Sync. Only	2 (SI/O)	1 (S	GI/O)	2 (SI/O)	1 (S	il/O)		2 (SI/O)		1 (S	I/O)	2 (SI/O)	1 (SI/O)	2 (S	I/O)	1 (SI/O)	2 (SI/O)	1 (S	/O)	2 (SI/O)
120.1	Clock Async. Only										-	-									
IEBus										2 (IV	1 (1)	ART)	(RT)								
Smart Card/SIM											1 (UA	ART)									
Synchronous Serial	Communication Unit/Special Serial I/O										1 (UA	ART)									
CAN	Channels										1										
IrDA	Message Box (Numbers)										1	6 -									
CRC Calculation	Circuit							1 (CI	RC-CCIT	T (X <sup>16</sup> + )	$(1^{12} + X^5 +$	1)/CRC-	-16 (X <sup>16</sup> -	+ X <sup>15</sup> + X <sup>2</sup>	+ 1))						
X/Y Converter											_	-	,								
	Input Only (Numbers)	Ļ,									-	-									
I/O Borto	CMOS I/O (Numbers)	71	5	5	71	5	5		71		5	5	71	55	7	1	55	71	55	5	71
I/O FOILS	High Current Drive Port											-									
	Pull-Up Resistor	71	5	5	71	5	5		71		5	5	71	55	7	1	55	71	55	5	71
External Interrup	ts Pins										1	1									
Debugging	On-Chip Debug										Ye	S							Ye	S	
Othor	BOM Correction Function			Yes	. (Addres	s match	× 2)				16	-		Yes	(Addres	s match	× 2)		Te	s	
Functions	Others						/			1	-	-			(*******		/				
Operating Freque	ency/Supply Voltage	20M	IHz/	16M	Hz/4 2 to	5.5V	201	/Hz/	16MHz/	20MHz/	16MHz/	20MHz/	16M	Hz/4 2 to	5 5V	20M	Hz/3.0 to	5.5V	16MHz/	20MHz/	16MHz/
Operating Archie	at Terresent un (°O)	3.0 to	5.5V		40 40 40	5.01	3.0 to	5.5V	4.2 to 5.5V	3.0 to 5.5V	4.2 to 5.5V	3.0 to 5.5V		40.4- 10	c.c.	2011	40 4- 01	-	4.2 to 5.5V	3.0 to 5.5V	4.2 to 5.5V
Operating Amble	ent temperature ( C)	- 40 1	10 85	-	- 40 10 12	5	- 40	10 85	- 40 10 125	- 40 10 85	- 40 10 125	- 40 10 85		40 10 12	5		- 40 10 8:	s 	- 40 10 125	- 40 10 85	- 40 10 125
		(B-A	KB-A KB-A KB-A KB-A KB-A KB-A KB-A KB-A											-8-	ę		-8-	-8-	- H)	j	4-B
Package*2		80	00 00 00 00 00 00 00 00 00 00 00 00 00											100		9644	80	190		804	
		POC		5	POC		5		POC			5	POC	POG		Š	POC	POC	DOG	5	POC
		FLC			FLC				PLC			2	PLC	FLC	Ē	2	LC	LC			PLC
		-			-				-				-				-	-			
		₽	우	노	웃	F	₽	<u>₽</u>	노					₽	₽	문	문				
		×.	1XX	XX	XX	XX	1XX	1XX	XX	0	0	0	0	X	XX	X	X	٩	٩	۵.	٩
Part No.		8T-X	8T-X	8V->	8V->	AV->	AT-X	AT-X	AV->	THE	HN	THF	ΗN	C-	C>	CT-)	CT-)	CTH	HAC	HTO	HAC
		9 0 W 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0										91F(	91FC	90FC							
		30   33   33   33   33   33   33   33										3029	3029	3029							
		ž	M30290MK M30291MK M30291MK M30291M/ M30291M/ M30290M/ M30291FF M30291FF M30291FF M30291FF M30290M/ M30290M/ M30290M/ M30291FF												ž	ž					

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

## • Specifications (M16C/10 Series)

Group				M16	C/1N						
	ROM (Bytes)	32	2K	64	IK	64K	+ 4K				
	RAM (Bytes)	1	K		3	K					
Memory	ROM Type*1			Ň			F				
	Data Flash		-	_		Yes	(4K)				
	Program Security		-	_		Yes (ID Code Check Function	, ROM Code Protect Function)				
	CPU			M16C/6	60 Core						
	Basic Instructions			9	1						
	Minimum Instruction Execution Time (ns)		62.5 (@16MHz)								
CPU	Multiplier		16×16→32								
	Multiply-Accumulate Instruction			16×16 -	+ 32→32						
	Barrel Shifter			-	_						
	DMAC (Channels)			-	_						
DMA	DTC/DMACII										
	Address Space (Bytes)	-	<u> </u>								
External Bus	External Bus Interface										
Expansion	Bus Structure										
	DRAM Controller			-	_						
	Clock Generation Circuit			3 circuits (Main clock, Sub	clock, On-chip oscillator)						
	PLL			-	-						
	Subclock			Ye	es						
OL 1	RTC			-	_						
Clock	On-Chip Oscillator			Ye	95						
	Oscillation Stop Detection			Ye	95						
	Frequency Divider			1/n (n=1, 2	2, 4, 8, 16)						
	Power Save			Wait	Stop						
Power Supply	Power-On Reset/POR			-	_						
Voltage Detection	Low Voltage Detection/LVD			-	_						
	Resolution × Channels			10-bi	t×14						
A/D Converter	Sample and Hold			Yé	28						
	Multi-Channel Sample and Hold		105								
D/A Converter	Resolution × Channels		8-bit × 1								
	8-bit			4 (Timer 1, Timer )	(, Timer Y, Timer Z)						
	16-bit			1 (Tin	ner C)						
	Input Capture	1 (Time C) -									
	Output Compare										
Timer	PWM Output		2 (Timer Y, Timer Z)								
	Real-Time Port										
	Event Counter		1 (Timer X)								
	2-Phase Encoder Input		· · · · · · · · · · · · · · · · · · ·								
	3-Phase Inverter Control										
Watchdog Timer											
	Clock Sync./ Clock Async.			2 (U/	ART)						
Serial Interface	Clock Sync, Only			· - · · ·							
	Clock Async, Only			-	_						
I <sup>2</sup> C-bus				-	_						
IEBus				-	_						
Smart Card/SIM				-	_						
Synchronous Serial	Communication Unit/Special Serial I/O			-	_						
	Channels			-	1						
CAN	Message Box (Numbers)			1	6						
IrDA				-	_						
CRC Calculation	Circuit			-	_						
X/Y Converter				-	_						
	Input Only (Numbers)			-	_						
	CMOS I/O (Numbers)			3	7						
I/O Ports	N-Channel Open Drain Port (Numbers)			-	_						
	High Current Drive Port										
	Pull-Up Resistor			3	7						
External Interrup	its Pins				3						
Debugging	On-Chip Debug	- Yes									
Function	On-Board Flash Program	- Yes									
Other	ROM Correction Function	Yes –									
Functions	Others			-	_						
Operating Freque	ency/Supply Voltage			16MHz/4	2 to 5.5V						
Operating Ambie	ent Temperature (°C)	- 40 to 125	- 40 to 85	- 40 to 125	- 40 to 85	- 40 to 125	- 40 to 85				
Package*2		PLOPOd4KB-A									
Part No.		1N2M4V-XXXFP	1N2M4T-XXXFP	1N2M8V-XXXFP	1N2M8T-XXXFP	1N2F8VFP	1N2F8TFP				
		M3C	M3C	Mac	Mac	M3C	Mac				

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

Automotive MCUs

### • Specifications (R8C/Tiny Series)

Group	•				-	B8C	/20									B8C	/21				
2																					
	ROM (Bytes)	32	2K	4	BK	64	K	96	5K	12	8K	32K	+ 2K	48K	+ 2K	64K -	+ 2K	96K	+ 2K	128K	+ 2K
	HAM (Bytes)	2	К	2.	5K	34	٢	5	К	6	К	21	٢	2.	5K	31	<	5	к	6	к
Memory	HOM lype"											-		-			(0)(0)		_		
	Data Hash							V		la Charl	Function	POM O	do Prot	ot Even	ion)	Yes (	2K)				
	Program Security							Yes	s (ID Cod	e Uneck	Function	, HUM Co	ue Prote	ect Hunct	ion)						
	CPU Regin Instructions										H8C	Core									
	Dasic Instructions	00.5	-		00.5	50	00.5	50	00.5	50	8					00.5			00.5		00.5
CPU	Minimum Instruction Execution	62.5 (@16MHz)	(@ 20	0 MH7)	62.5 (@16MH-)	50 (@20MHz)	62.5 (@16MH=)	50 (@20MH=)	62.5 (@16MHz)	50 (@20MH-)	62.5 (@16MH-)	50 (@ 20MH <del>7</del> )	62 (@16	2.5 MH-7)	50 (@20MH=)	62.5 (@16MH=)	(@20	0 MH	62.5 (@16MHz)	50 (@20MH=)	62.5 (@16MHz)
	Multiplior	(**************************************	1820		1.0 100012)	1.0 20101 12)	1.0 10/11/12)	(*************************************		(@20WIIIZ)	16 1 1	(*************************************	1010		(0201011Z)	(@.000.07)	1820		(*************************************	(0201011Z)	10101112)
	Multiply-Accumulate Instruction										16 \ 16	1 32-122									
	Clock Concration Circuit								2	circuite (I	Jain clos	+ 32-732		or)							
	PLI		2 circuits (main ciocx, Un-crip osciliator) — —																		
	Subclock																				
	BTC																				
Clock	On-Chip Oscillator							Yes	(High pre	h precision, High speed : 40MHz, Low speed : 125kHz)											
	Oscillation Stop Detection								(		<u>9</u> Y	es	, <u> </u>								
	Frequency Divider									1	/n (n=1.	2. 4. 8. 16	)								
	Power Save										Wait	/Stop	/								
Power Supply	Power-On Reset/POR										Y	es									
Voltage Detection	Low Voltage Detection/LVD	1								Yes	(Voltage	detection	n 2)								
	Resolution × Channels										10-bi	t × 12	1								
A/D Converter	Sample and Hold	İ									Y	es									
D/A Converter	Resolution × Channels										-	-									
	8-bit		3 (Timer RA, Timer RB, Timer RE)																		
	16-bit		2 (Timer RD)																		
	Input Capture									8 (s	hared wi	th Timer F	RD)								
	Output Compare									9 (share	d with Tin	ner RD, Ti	mer RE)								
Timer	PWM Output									7 (share	d with Tin	ner RB, Ti	mer RD)								
	Real-Time Port	1 (shared with Timer RA)																			
	Event Counter																				
	2-Phase Encoder Input																				
	3-Phase Inverter Control		1 (shared with Timer RD)																		
Watchdog Timer			1 (with automatic start, clock source protection function)																		
	Clock Sync./ Clock Async.										1 (UA	ART0)									
Serial Interface	Clock Sync. Only										-	_									
	Clock Async. Only										1 (UA	ART1)									
I <sup>2</sup> C-bus								1	I (Share	with Syno	chronous	Serial Co	mmunic	ation Uni	t)						
Synchronous Serial	Communication Unit/Special Serial I/O										1 (Share	with I*C)									
CAN	Channels											_									
	Message Box (Numbers)																				
	Input Only (Numbers)											3									
VO Danta	CMOS I/O (Numbers)										4	-1									
NO Ports	High Current Drive Port (Numbers)											_									
	Rull-Lip Resister											1									
External Interrup	ts Pins										4	8									
Dobugging	On-Chin Debug										~										
Function	On-Board Flash Program										V	es									
Other	BOM Correction Function										-	_									
Functions	Others																				
											ACMUN /	001411-7	1010-2								
		3.0 to 5.5V	20N 3.0 to	5.5V	3.0 to 5.5V	20WHZ/ 3.0 to 5.5V	10MHZ/ 3.0 to 5.5V	201/HZ/ 3.0 to 5.5V	3.0 to 5.5V	20MHZ/ 3.0 to 5.5V	3.0 to 5.5V	∠uwiHz/ 3.0 to 5.5V	16N 3.0 to	5.5V.	20MHZ/ 3.0 to 5.5V	3.0 to 5.5V	20N 3.0 to	1112/ 5.5V.	3.0 to 5.5V	201/IHZ/ 3.0 to 5.5V	3.0 to 5.5V
Operating Freque	ency/Supply Voltage	10MHz/	10N	1Hz/	10MHz/	10MHz/	10MHz/	10MHz/	10MHz/	10MHz/	10MHz/	10MHz/	10N	1Hz/	10MHz/	10MHz/	10N	/Hz/	10MHz/	10MHz/	10MHz/
		2.7 to 5.5V	2.7 to	5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to	5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to	5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V
Operating Ambie	ent Temperature (°C)	-40 to 125 - 40 to 85 - 40 to 125							- 40 to 125	- 40 to 85	- 40 to 125										
Package*2											PLQP00	48KB-A						-			
									*	*	:								\$	*	*
Deathla		문	L.	Ê	료	Ê.	E.	Ê	Ч	E.	Ę	Ê.	E.	윤	Ê.	료	с Ш	Ê	E E	Ë	ΕP
Fart NO.		NoK	061	r20	D7K	080	<b>78K</b>	NAU NAU	DAK	S	Ó	161	16K	17 X	17.1	18K	18,	IA	1 AK	3	Š.
		212(	212(	212(	212(	212(	2120	212(	212(	212(	212(	512.	12.	512.	12.	512	12	512	512	512.	212
		5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2	5F2
		Ĕ	Ű.	Ë	Ĕ	Ľ.	É	Ľ.	Ű.	Č.	Ľ.	Ĕ	Ω.	Ċ.	Ĕ	Ľ.	Ω.	Ľ.	l CC	Ű.	É

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

#### • Specifications (R8C/Tiny Series)

<u> </u>	```				,																
Group						R8C	/22									R80	2/23				
	ROM (Bytes)	32	К	48	K	64	К	9	5K	12	8K	32K	+ 2K	48K -	- 2K	64K	+ 2K	96K -	+ 2K	128K	( + 2K
	BAM (Bytes)	24	<	25	5K	31	<	5	к	6	ĸ		ĸ	25	к	3	ĸ	5	<	6	K
Memory	BOM Type*1									-	F						-			-	
womory	Data Elach										— i					Vaa	(0K)				
	Data Flash						-	Ve		- Charle	C.us atian		ada Deste	at Europein		res	(2K)				
	Program Security							Ye	s (ID Coa	е Спеск	Function,	ROM C	ode Prote		on)						
	CPU										R8C	Core									
	Basic Instructions										8	9									
ODU	Minimum Instruction Execution	62.5	50	62.5	50	62.5	5	50	62	.5	5	0	62.5	50	62	2.5	50	62.5	5	C	62.5
CPU	Time (ns)	(@16MHz)	(@20MHz)	(@16MHz)	(@20MHz)	(@16MHz)	(@20	MHz)	(@16	MHz)	(@20	MHz)	(@16MHz)	(@20MHz)	(@16	MHz)	(@20MHz)	(@16MHz)	(@20	MHz)	(@16MHz)
	Multiplier	1									16×1	6→32									
	Multiply-Accumulate Instruction	1									16 × 16 +	+ 32→32	>								
	Clock Generation Circuit								20	circuite (M	Aain clock	(On-ch	 n-chin oscillator)								
	BLI																				
	l LL Outralaalu																				
	SUDCIOCK		 Yes (High precision, High speed : 40MHz, Low speed : 125kHz)																		
Clock	RIC																				
	On-Chip Oscillator																				
	Oscillation Stop Detection		Y																		
	Frequency Divider		1/n (n=										6)								
	Power Save		Wait/Stop																		
Power Supply	Power-On Reset/POR	1									Ye	es									
Voltage Detection	Low Voltage Detection/LVD									Yes	(Voltage	detectio	on 2)								
	Besolution × Channels										10-bit	× 12	/								
A/D Converter	Sample and Hold										V	20									
D/A Comunitar	Deselution - Channels											55									
D/A Converter	Resolution × Channels		-																		
	8-bit		3 (Timer RA, Timer RB, Timer RE)																		
	16-bit		2 (Timer RD)																		
	Input Capture	8 (shared with Timer RD)																			
	Output Compare									9 (shared	d with Tim	ner RD, "	Timer RE)								
Timer	PWM Output									7 (shared	d with Tim	ner RB, "	Timer RD)								
	Real-Time Port	-																			
	Event Counter	1 (shared with Timer BA)																			
	2-Phase Encoder Input																				
	2-Phase Inverter Centrel		1 (shared with Timer BD)																		
Matabala a Timor	3-1 hase inventer control																				
watchdog rimer			1 (with automatic start, clock source protection function)																		
	Clock Sync./ Clock Async.										1 (UA	RT0)									
Serial Interface	Clock Sync. Only																				
	Clock Async. Only										1 (UA	RT1)									
I <sup>2</sup> C-bus									I (Share v	with Sync	hronous	Serial C	ommunic	ation Unit)							
Synchronous Serial	Communication Unit/Special Serial I/O										1 (Share	with I <sup>2</sup> C	)								
	Channels										1	1									
CAN	Message Box (Numbers)	1									1	6									
	Input Only (Numbers)										3	3									
	CMOS I/O (Numbers)										4	1									
I/O Ports	N-Channel Open Drain Port (Numbore)											_									
1/01/01/3	High Current Drive Port																				
	Bull Up Posister											1									
Extornel later	to Dino										4										
External Interrup	is Pins											5	_								
Debugging	On-Chip Debug										Ye	es									
Function	On-Board Flash Program										Ye	es									
Other	ROM Correction Function																				
Functions	Others											-									
		16MH7/	20MH7/	16MH7/	20MHz/	16MHz/3.0	201	/Hz/	161	1H7/	201/	1Hz/	16MH7/	20MHz/	161	1H <del>7</del> /	20MH7/	16MHz/	20M	Hz/	16MH7/
0	10	30 to 5.5V, 30 to 5.5V, 30 to 5.5V, 30 to 5.5V, at 55V, at 5.5V, a								3.0 to 5.5V.	3.0 to	5.5V.	3.0 to 5.5V.								
Operating Freque	ency/Supply voltage	10MHz/	10MHz/	10MHz/	10MHz/2.7	10MHz/2.7	101	/Hz/	10N	1Hz/	10N	1Hz/	10MHz/	10MHz/	10N	1Hz/	10MHz/	10MHz/	10M	Hz/	10MHz/
		2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	to 5.5V	to 5.5V	2.7 to	5.5V	2.7 to	5.5V	2.7 to	5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to	5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to	5.5V	2.7 to 5.5V
											- 40 to										
Operating Ambie	ent Temperature (°C)	- 40 to   - 40 to   - 40 to   - 40 to   - 40 to   - 40 to 85   - 40 to 125   - 40 to 85   - 40 t									125										
Pookogo*2		120	00	120	00	120							120	00			00	120			120
гаскаде -		PLQP0048KB-A																			
Part No.		1226KFP	1226JFP	1227KFP	1227JFP	1228KFP	1228JFP	122AJFP*	122AKFP**	122CKFP**	122CJFP*	1236JFP	1236KFP	1237JFP	1237KFP	1238KFP	1238JFP	123AKFP**	123AJFP*	123CJFP*	123CKFP**
		35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2	35F2

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

Automotive MCUs

#### • Specifications (R8C/Tiny Series)

<u> </u>													
Group			R80	C/26			R80	C/27		R80	C/28	R80	C/29
	ROM (Bytes)	16	SK	32	2K	16K	+ 2K	32K	+ 2K	16	δK	16K	+ 2K
	BAM (Bytes)	1	к	1	5K	1	к	1	5K		1	ĸ	
Momony	POM Tupo*1	· · ·						-					
Memory	Now Type							(0)()					(01/)
	Data Flash						Yes	(2K)			-	Yes	(2K)
	Program Security					Yes (ID Code C	Check Function	, ROM Code Pr	otect Function)	1			
	CPU						R8C	Core					
	Basic Instructions						8	19					
CPU	Minimum Instruction Execution Time (ns)	50 (@20MHz)	62.5 (@16MHz)	50 (@20MHz)	62.5 (@16MHz)	50 (@20MHz)	62.5 (@16MHz)	50 (@20MHz)	625(@	16MHz)	50 (@2	20MHz)	62.5 (@16MHz)
0.0	Multiplior	00 (0 2011112)	02.0 (0 100012)	00 (0 2011112)		00 (0200012)	161	6 200	02.0 ( 0	1011112)	00(01		
	Multiplier						1 × 01	0					
	Multiply-Accumulate Instruction						16 × 16 ·	+ 32→32					
	Clock Generation Circuit					2 circ	uits (Main cloc	k, On-chip osci	lator)				
	PLL		-										
	Subclock		-										
	BTC												
Clock	On Chin Oppillator												
	On-Chip Oscillator				10	es (High precis	ion, nigh speed	J. 40IVIEZ, LOW	speeu . 125kn	2)			
	Oscillation Stop Detection						Y	es					
	Frequency Divider						1/n (n=1, 1	2, 4, 8, 16)					
	Power Save						Wait	/Stop					
Power Supply	Power-On Reset/POR						Y	es					
Voltage Detection	Low Voltage Detection/LVD						Voc (Voltage	dotaction 2)					
Voltage Deteotion	Edw voltage Detection/EVD				10.1.		ies (voltage	uelection 2)			101		
A/D Converter	Resolution × Channels				10-bi	t × 12					10-0	lt×4	
	Sample and Hold						Y	es					
D/A Converter	Resolution × Channels						-	_					
	8-bit					3	(Timer RA, Tim	er RB. Timer R	E)				
	16-bit						1 (Tim	er BC)	/				
	Input Capture						4 (sharod wi	th Timor PC)					
	Input Capture		4 (shared with Timer RC, Timer RE)										
	Output Compare												
Timer	PWM Output					4 (	shared with Tin	ner RB, Timer F	RC)				
	Real-Time Port	1 (shared with Timer RA)											
	Event Counter												
	2-Phase Encoder Input												
	2-1 hase Encoder input												
	3-Phase Inverter Control												
Watchdog Timer	r	1 (with automatic start, clock source protection function)											
	Clock Sync./ Clock Async.		2 (UART0, UART1) 1 (UART0)										
Serial Interface	Clock Sync. Only						-	_					
	Clock Async, Only				-	_					1 (UA	ABT1)	
I <sup>2</sup> C-bus						1 (Share with	Synchronous	Serial Commu	nication Unit)			,	
Punchronous Carial	Communication Unit/Constal Corial I/O					i (onaro ma	1 (Choro	with I <sup>2</sup> C)	noution only				
Synchronous Senai	Communication Onlyspecial Senar I/O						T (Share	wiiin (C)					
CAN	Channels							_					
	Message Box (Numbers)						-	-					
	Input Only (Numbers)						:	3					
	CMOS I/O (Numbers)				2	!5					1	3	
I/O Ports	N-Channel Open Drain Port (Numbers)					-	-	_					
	High Current Daire Dart							_					
	High Current Drive Fort					-							
	Puil-Up Resistor				2	:D					1	3	
External Interrup	ts Pins							7					
Debugging	On-Chip Debug						Y	es					
Function	On-Board Flash Program						Y	es					
Other	BOM Correction Function						-	_					
Functions	Othors							_					
1 dilotiono	Others												
		20MHz/	16MHz/	20MHz/	16MHz/	20MHz/	16MHz/	20MHz/					16MHz/
Operating Freque	ency/Supply Voltage	3.0 to 5.5V,	3.0 to 5.5V,	3.0 to 5.5V,	3.0 to 5.5V,	3.0 to 5.5V,	3.0 to 5.5V,	3.0 to 5.5V,	16MHz/3.	.0 to 5.5V,	20MHz/3	.0 to 5.5V,	3.0 to 5.5V,
operating rieque	eney/ouppiy voltage	10MHz/	10MHz/	10MHz/	10MHz/	10MHz/	10MHz/	10MHz/	10MHz/2	.7 to 5.5V	10MHz/2	.7 to 5.5V	10MHz/
		2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V					2.7 to 5.5V
Operating Ambio	ent Temperature (°C)	- 40 to 85	- 40 to 125	- 40 to 85	- 40 to 125	- 40 to 85	- 40 to 125	- 40 to 85	_ 40 +	o 125	_ 40	to 85	- 40 to 125
Package *2	in temperature ( O)										4010125		
Package					PLQPU	J32GB-A					PLSPU	J2UJB-A	
		*	:	*	1	*	*	1	*	*			*
-		ř.	<u>с</u>	ř.	L L	<u>à</u>	d L	ė.	d L	с С	Ē,	Ľ.	с. С
Part No.		104	X X	3.JF	X	4.JF	X X	3.1F	×.	¥ X	416	410	X X
		26	56	26	56	27.	27.	27	27	58	58	59	50
		21	21	21	21	51	51	51	21	21	21	51	21
		35F	35F	35F	35F	35F	35F	35F	35F	35F	35F	35F	35F
		<u> </u>	L .	<u> </u>	L	<u> </u>	L	L	ш.	<u> </u>	<u> </u>	<u> </u>	L .

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

MCUs for Notebook PCs / PC Servers

### • Specifications (M16C/6K Group)

Group		M16C/6KA						
	ROM (Bytes)	128K						
	RAM (Bytes)	5K						
Memory	ROM Type <sup>*1</sup>	F						
	Data Flash	-						
	Program Security	-						
	CPU	M16C/60 Core						
	Basic Instructions	91						
CRU	Minimum Instruction Execution Time (ns)	62.5 (@16MHz)						
CFU	Multiplier	16×16→32						
	Multiply-Accumulate Instruction	16×16+32→32						
	Barrel Shifter	-						
DMA	DMAC (Channels)	-						
	Clock Generation Circuit	2 circuits (Main clock, Sub clock)						
Clock	Subclock	-						
CIUCK	Frequency Divider	1/n (n=1, 2, 4, 8, 16)						
	Power Save	Normal operating (High-speed, Medium-speed) /Wait/Stop						
	Resolution × Channels	10-bit×10						
AVD Converter	Sample and Hold	-						
D/A Converter	Resolution × Channels	-						
	8-bit	-						
Timor	16-bit	11						
TITIET	PWM Output	6						
	Event Counter	–						
Watchdog Timer		1						
	Clock Sync./ Clock Async.	1						
Serial Interface	Clock Sync. Only	2 (SI/O3, SI/O4)						
	Clock Async. Only							
I <sup>2</sup> C-bus		3						
	Input Only (Numbers)	1						
	CMOS I/O (Numbers)	129						
I/O Ports	N-Channel Open Drain Port (Numbers)	37						
	High Current Drive Port	16						
Pull-Up Resistor		104						
External Interrup	ts Pins	16						
Other	ROM Correction Function	–						
Functions	Others	PS/2 Interface × 3						
Operating Freque	ency/Supply Voltage	16MHz/3.0 to 3.6V						
Operating Ambient Temperature (°C)		- 20 to 85						
Package*2		PTQP0144LA-A						
Part No.		M306KAFCLRP						

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

USB MPUs and MCUs

## • Specifications (M16C/20 Series)

Group			M16C/24									
	ROM (Bytes)	64K	12	вК								
	RAM (Bytes)	5K	10	K								
Memory	ROM Type*1	N	Λ	F								
wichtory	Data Flash		-									
	Program Security	-	-	Yes (ID code check function, ROM code protect function)								
	CPU		M16C/60 Core									
	Basic Instructions		91									
CPU	Minimum Instruction Execution Time (ns)		62.5 (@16MHz)									
0.0	Multiplier		16×16→32									
	Multiply-Accumulate Instruction		16×16+32→32									
	Barrel Shifter											
DMA	DMAC (Channels)		4									
	Addross Space (Bytes)		114									
External Rue	External Bus Interface	Supp	ort for insertion of 1 to 3 wait states. Outputs 4 chin-select si	anals								
Expansion	Bus Structure	Data Bus Width can be selected (8/16-bit). The number of output address buses can be selected (16/20)										
	DBAM Controller	But But Multi dur bu										
	Clock Generation Circuit		3 circuits (Main clock, Sub-clock and On-chip oscillator)									
	PLL		Yes									
	Subclock		Yes									
Clock	RTC		_									
CIUCK	On-Chip Oscillator		Yes									
	Oscillation Stop Detection		Yes									
	Frequency Divider		1/n (n = 1, 2, 4, 8, 16)									
	Power Save	Normal operating	High-speed, Medium-speed, Low-speed, Low-power consu	mption) /Wait/Stop								
Power Supply	Power-On Reset/POR											
vollage Detection	Low Voltage Detection/LVD											
	Resolution × Channels		TU-DIL × 8									
A/D Converter	Multi-Channel Sample and Hold											
D/A Converter	Besolution × Channels	-										
DIA COnverter	8-bit		_									
	16-bit		5 (Timer A0, Timer A1, Timer A2, Timer A3, Timer A4)									
	Input Capture											
	Output Compare	-										
Timer	PWM Output	5 (shared with Timer A0, Timer A1, Timer A2, Timer A3, Timer A4)										
	Real-Time Port	-										
	Event Counter	5 (\$	shared with Timer A0, Timer A1, Timer A2, Timer A3, Timer	A4)								
	2-Phase Encoder Input											
Watchdog Timer	3-Filase inverter Control		1									
Tratondog Timor	Clock Sync./ Clock Async.		4 (UART0, UART1, UART2, UART3)									
Serial Interface	Clock Sync. Only		_									
	Clock Async. Only		_									
I <sup>2</sup> C-bus			4 (UART0, UART1, UART2, UART3)									
IEBus			4 (UART0, UART1, UART2, UART3)									
Smart Card/SIM			4 (UARTO, UART1, UART2, UART3)									
Synchronous Serial	Communication Unit/Special Serial I/O		2 (UART0, UART1, Serial sound interface)									
CAN	Mossage Box (Numbers)											
LISB Eunction	Message Dox (Numbers)		Ves (Full-Speed)									
IrDA	·	Tes (rui-Speed)										
CRC Calculation	Circuit		2 (CRC-CCITT, CRC16)									
X/Y Converter												
	Input Only (Numbers)	1										
	CMOS I/O (Numbers)		80									
I/O Ports	N-Channel Open Drain Port (Numbers)		2									
	High Current Drive Port		8 (20mA)									
E	Pull-Up Resistor		80 (Possible to Set Each of 4 Ports)									
External Interrup	On-Chin Dohug	i e (ivi < 3, NiNi K 1, Key input < 0)										
Function	On-Board Elash Program											
Other	BOM Correction Function		Yes (Address match)									
Functions	Others		Serial Sound Interface : 2, AND Flash Controller									
Operating Freque	ency/Supply Voltage		16MHz/3.0 to 3.6									
Operating Ambie	ent Temperature (°C)		– 20 to 85									
Package*2		PLQP0100KB-A										
Part No.		M30245M8-XXXGP	M30245MC-XXXGP	M30245FCGP								

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Q : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

TV MCUs

## • Specifications (M16C/6V Group)

Group					M16	C/6V						
	ROM (Bytes)	25	6K	38	4K	1	51	2K				
	RAM (Bytes)			10	OK			16	SK			
Memory	ROM Type*1	М	F	М	F	М	F	М	F			
,	Data Flash		1			-	1	1				
	Program Security	-	- Yes (ID code check function) - Yes (ID code check function) - Yes (ID code check function) - Yes (ID code									
	CPU		M16C/60 Core									
	Basic Instructions				ę	)1						
	Minimum Instruction Execution Time (ns)				62.5 (@	16MHz)						
CPU	Multiplier				16×1	6→32						
	Multiply-Accumulate Instruction				16×16	+ 32→32						
	Barrel Shifter					_						
	DMAC (Channels)					2						
DMA	DTC/DMACII					_						
	Address Space (Bytes)		1M									
External Bus	External Bus Interface			Support for insertion o	f 1 wait states, Output	s 4 chip-select signals	(CS0, CS1, CS2, CS3	)				
Expansion	Bus Structure		Separate bus, E	Data bus width can be	selected (8-bit/16-bit),	The number of output a	address buses can be	selected (16/20)				
	DRAM Controller					_						
	Clock Generation Circuit				3 circuits (Main clock,	Sub-clock OSD clock)						
	PLL					_						
	Subclock											
<b></b>	Real Time clock					_						
Clock	On-Chip Oscillator					_						
	Oscillation Stop Detection					_						
	Frequency Divider		1/n (n=1, 2, 4, 8, 16)									
	Power Save		Intruct 1, 2, 4, 9, 100 Normal operation (High-speed, Medium-speed, Low-speed,									
Power Supply	Power-On Reset/POR											
Voltage Detection	Low Voltage Detection/LVD					_						
	Resolution × Channels				8-b	t×6						
A/D Converter	Sample and Hold				Y	es						
	Multi-Channel Sample and Hold											
D/A Converter	Resolution × Channels		8-bit×2									
	8-bit											
	16-bit	8 (Timer A, Timer B)										
	Input Capture	-										
	Output Compare					_						
Timer	PWM Output				2 (Tir	ner A)						
	Real-Time Port											
	Event Counter	8 (Timer A, Timer B)										
	2-Phase Encoder Input											
	3-Phase Inverter Control											
Watchdog Timer			1									
	Clock Sync./ Clock Async.				2 (UART	), UART2)						
Serial Interface	Clock Sync. Only					_						
	Clock Async. Only					-						
I <sup>2</sup> C-bus					2 (Multi n	naster I <sup>2</sup> C)						
IEBus						-						
Smart Card/SIM						_						
Synchronous Serial	Communication Unit/Special Serial I/O					-						
CAN	Channels					-						
OAN	Message Box (Numbers)					-						
IrDA						_						
CRC Calculation	Circuit					-						
X/Y Converter						-						
	Input Only (Numbers)					-						
	CMOS I/O (Numbers)				7	4						
I/O Ports	N-Channel Open Drain Port (Numbers)					2						
	High Current Drive Port											
	Pull-Up Resistor	74 (Pull-up resistor can be set every four ports)										
External Interrup	its Pins					3						
Debugging	On-Chip Debug	_	Yes	-	Yes	-	Yes	-	Yes			
Function	On-Board Flash Program	_	Yes	-	Yes	-	Yes	-	Yes			
Other	ROM Correction Function	Yes (Address match × 2)	-	Yes (Address match × 2)	-	Yes (Address match × 2)	-	Yes (Address match × 2)	-			
Functions	Others			C	CD, ID1 : 2 circuits, Tri	ple-layer, 512-color OS	SD					
Operating Freque	ency/Supply Voltage				16MHz/3.	15 to 3.45V						
Operating Ambie	ent Temperature (°C)	- 20 to 70										
Package*2		PRQP0100JB-A										
Part No.		06V7MG-XXXFP	06V7FGFP	06V7MH-XXXFP	06V7FHFP	06V7MJ-XXXFP	06V7FJFP	06V7MJA-XXXFP	06V7FJAFP			
		Β	Ň	М	Ж	Β	Ň	Β	θ. M			

\*1 F : Flash memory version, L : ROM-less version, M : Mask ROM version, O : One time PROM version, Qz : QzROM version \*2 Please refer to "Package Code and Size Table" in the end of this catalog for the previous code

## **Support System**

Get the latest information on the M16C Family at the Renesas Web site.

## Renesas M16C Family Web Page http://www.renesas.com/m16c

#### A wealth of information is available, including the latest technical data necessary for system development.



#### customers to assess product functions and performance. RENESAS RENESAS were available and ferritoring in the state Evolution Software Software and Tool Propulsion in the Proceedings Software and Cotolog Development To Cotolog Latest updates Revision History Tool Selector Product Information Application No. These links display pages containing Easy to use GUI anvestment for your Development Tools. Downloads datasheets providing overviews, features, and functions of the main Renesas' IDE FAQS Technical Unda Renesas tool products. Related Ret RENESAS MILE AVAILABLE AVA Emulators On-chip debugging And Park Article poeted wi permission of Nu Horizons' "Nexus publication. Lineup: Disana sebanak Disana sebanak Disana sebanak Disanakat D T-Engine Ortaal Tour Initial Facely relationships Initial Annual Addition (parts) Initial Annual Addition (parts) Initial Annual (parts) Initial Annual (parts) Initial Annual (parts) Initial Annual (parts) Da Braddo Salivara Salivarity, 51.00 Salivarity, 51.00 Renesas' T-Engine Tour of Ukiaobous House 120 Mar 2006, Open Company Sector Control Sector Document Lipsteler | Thi Documentation This link displays a page where product documentation for Renesas tool products such as manuals can be downloaded. Information on Accessories This link displays a page with information such as patterns for connecting emulators and user systems and details of accessories used to make connections. Coding Tools | Enulation and Debugging | Q51 Middlewwwe and Driv Reference Design | Sustant Internations | C. Sochaft and Converter Renesas Partner Information This link displays a page containing overviews and contact information for Renesas partner companies. ③ Regine: 8208AL 國 · 日本 | 서운 | 上新 | 亜北 Software and Tools PRODUCTS APPLICATIONS SUPPORT Ditor a Keyword (2) Enter a Part No. (23) RENESAS This link displays a page with Perametric Search C links to a variety of development tool products such as starter kits Software and Tools and flash memory programmers. C Full Product Info Characteristics Osciliation Paramet Product Specifical Sample Codes Application Notes Decumentation Downloads FAQs Description Renesas Starter Kit for R0C/25 Renesas Starter Kit for R0C/25 Alliance Partners The alliance program provides online tools to increase the synergy between our customers, third-party partners, and Renesas.

nformation for Customers Considering Purchasing Renesas Tools

AMERICAL D 非本: 马会: 上向 · 臺北

Evaluation Software

Evaluation versions of software are

provided free of charge to enable



## Renesas Software and Tools Web Page http://www.renesas.com/tools

For customers considering purchasing Renesas tools, this Web page contains links relating to individual products, including function overviews and downloads of software evaluation versions. It is also a place where customers who already own Renesas tools can obtain the latest information, software upgrades, and more.





## **Documentation**

#### Application



## **Application Notes**

In addition to the manuals for each product, a large number of application notes are available that customers can make immediate use of in their programs.

	List of Application Note Categories	
A/D Converters	D/A Converters	Flash Memory
l <sup>2</sup> C-bus	Intelligent I/O	Interrupts
Noise	CRC	Program Security
Resets	Serial Interfaces	PWM Timers for 3-Phase Motor Drive
Timers	Watchdog Timers	DMAC
CAN	USB	External Buses
Applications	Motors	Inverter
Automotive	Development Tools	

The latest versions of Renesas documents are available for download on the following Web page. URL http://www.renesas.com/m16c

MEMO
------



## Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

- Personal properties of the purpose of any other military use. When exporting the product a variable of the solution of the purpose of any other military use. When exporting the product a variable of the solution of the purpose of any other military use. When exporting the product of the variable of the solution of the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control examples.
  9. An information included in this document, solutions, and position of control examples.
  9. An information included in this document, solutions, and position of control examples.
  9. An information included in this document is the approximation of the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control aware in the information included in this document.
  9. An information included in this document is the applicable of control examples.
  9. An information included in this document is the applicable of control examples.
  9. An information included in this document is used. Sub information included in this document, but here so and information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in this document.
  9. An information included in



#### **RENESAS SALES OFFICES**

Refer to "http://www.renesas.com/en/network" for the latest and detailed information.

Renesas Technology America, Inc. 450 Holger Way, San Jose, CA 95134-1368, U.S.A Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K. Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd. Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120 Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd. 7th Fl., North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd. 10th Fl., No.99, Fushing North Road, Taipei, Taiwan Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd. 1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632 Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd. Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd. Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia Tel: <603> 7955-9390, Fax: <603> 7955-9510

#### http://www.renesas.com