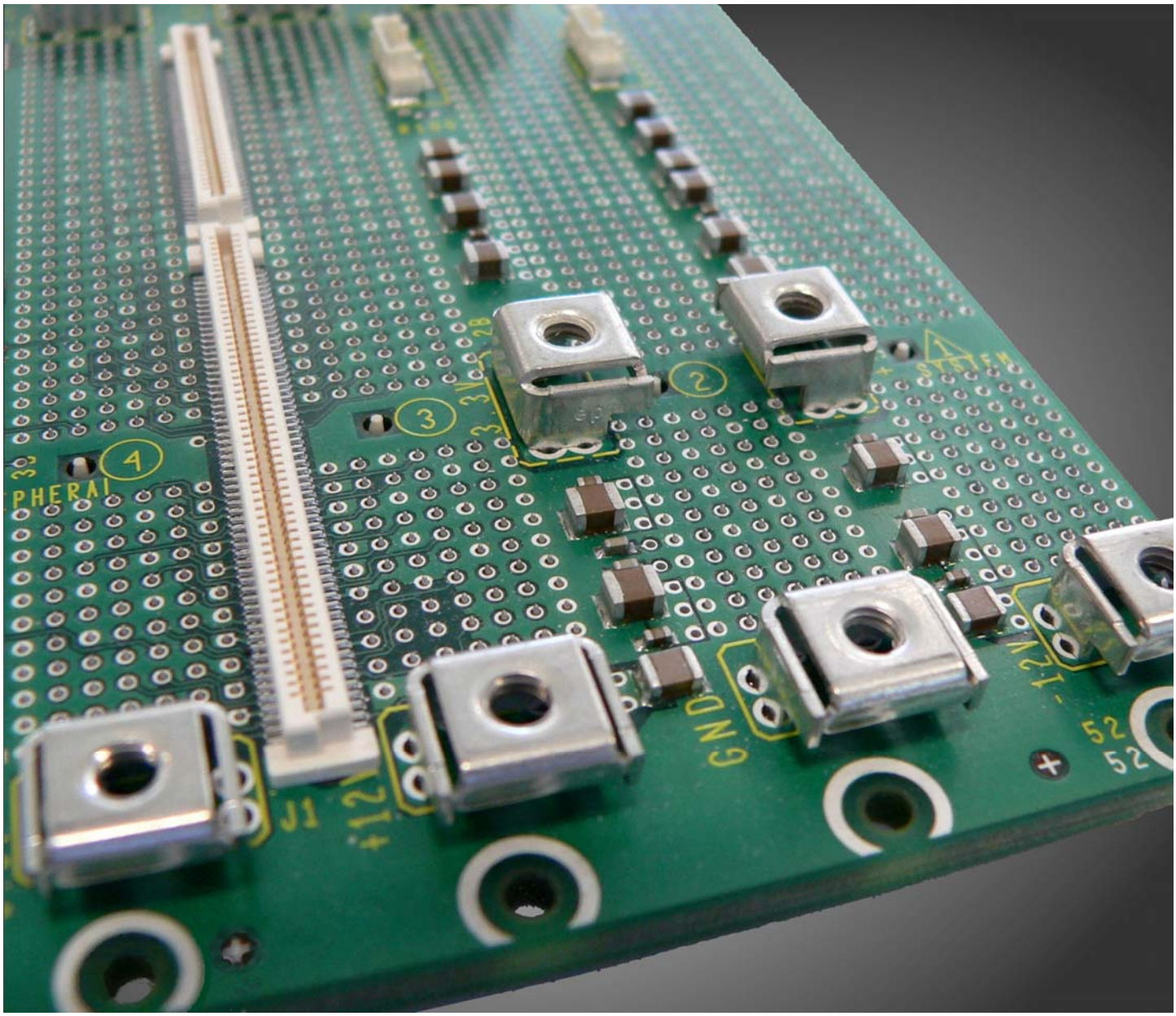
User Manual
CompactPCI Backplanes



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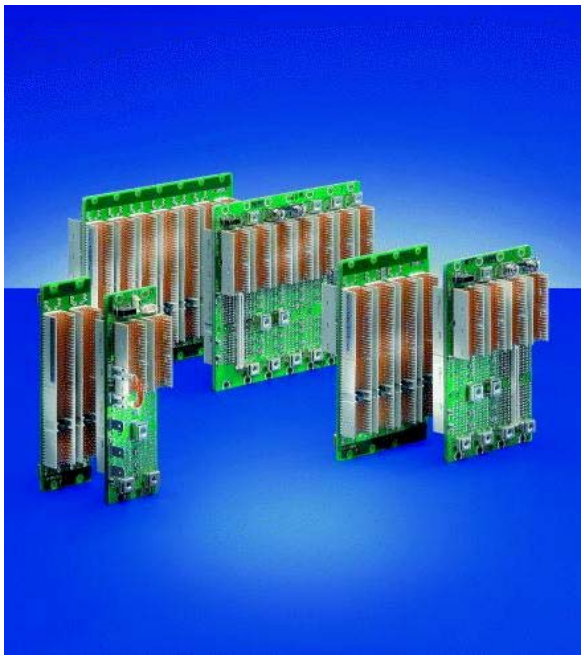


What is CompactPCI®

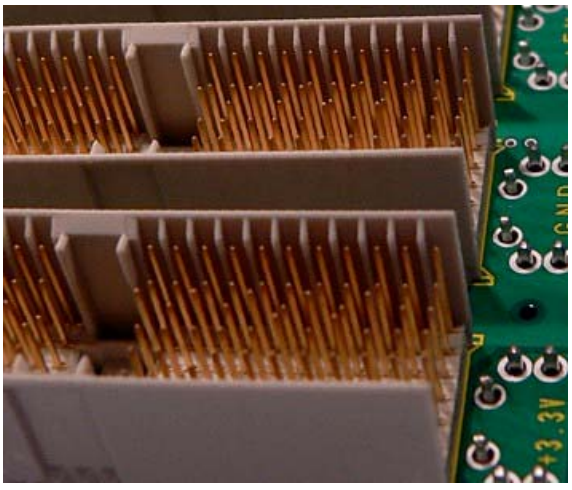
The latest specification for PCI-based industrial computers is called CompactPCI. It is electrically, a superset of desktop PCI with a different physical form factor. CompactPCI utilizes the Eurocard form factor popularized by the VME bus.

Defined for both 3U (100mm by 160 mm) and 6U (160mm by 233 mm) card sizes, CompactPCI has the following features:

- Standard Eurocard dimensions (compliant with IEEE 1101.1 mechanical standards)
- High density 2mm Pin-and-Socket connectors (IEC approved and Bellcore qualified)
- Vertical card orientation for effective cooling
- Easy card retention
- Excellent shock and vibration characteristics
- Metal front panel
- User I/O connections on front or rear of module
- Standard chassis available from many suppliers
- Uses standard PCI silicon, manufactured in large volumes
- Staged power pins for Hot Swap capability
- Eight slots in basic configuration. Easily expanded with Bridge Chips

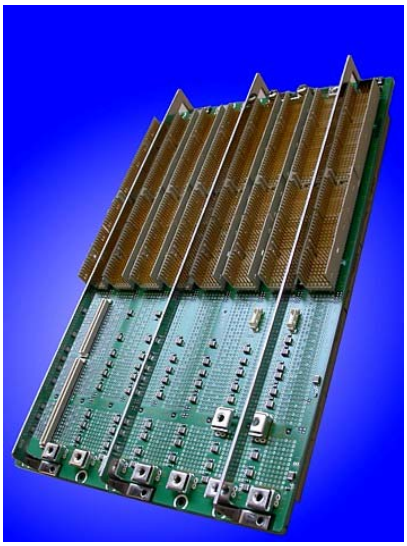
What is PICMG

PICMG (**P**CI **I**ndustrial **C**omputer **M**anufacturers **G**roup) is a consortium of over 600 companies who collaboratively develop open specifications for high performance telecommunications and industrial computing applications. The members of the consortium have a long history of developing leading edge products for these industries.



CompactPCI Connector

The CompactPCI connector is a shielded 2mm pitch, 5+2 row connector, compliant to IEC 61076-4-101. Main features of this connector are the pin stagging for hot swap and shielding for EMI/RFI protection.



Schroff CompactPCI Backplanes

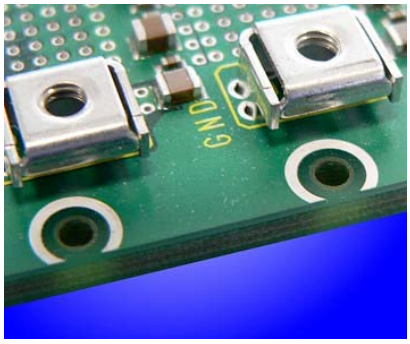
Schroff CompactPCI backplanes are fully compliant to the latest PICMG specifications.

PICMG 2.0 R 3.0	cPCI Core Specification
PICMG 2.1	cPCI Hot Swap Specification
PICMG 2.6	Bridging Specification
PICMG 2.9	System Management Bus Specification
PICMG 2.10	Keying Specification

Schroff CompactPCI backplanes are specially designed to achieve exellent power distribution, best signal integrity, virtually zero cross talk, and minimum clock skew. The SMD components used on Schroff CompactPCI backplanes lead to a much lower failure rate than conventional components.

Schroff uses ceramic capacitors on the CompactPCI backplanes to gain a better noise reduction at frequencies above 10MHz. This feature reduces the radiated and conducted noise caused by the processor and PCI clock signals. In addition, ceramic capacitors have no limitation in useful lifetime, as compared to aluminium capacitors that dry out after 5 to 10 years, and are unaware of the hazardous fire risks known from tantalum electrolytics'.

Schroff CompactPCI Backplane Features

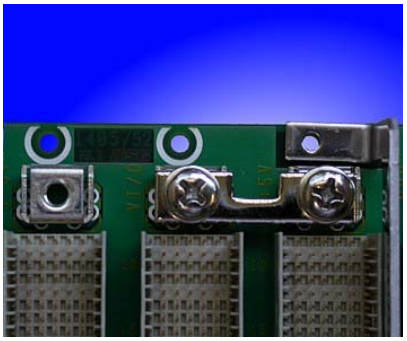


Isolated Assembling / Connection to ChassisGND

Schroff cPCI backplanes have a specially designed pattern of mounting holes to assemble the backplane isolated or connected to ChassisGND.

For isolation between BackplaneGND and ChassisGND M2.5 screws and isolating washers should be used in at least every second connector position.

If noise reduction shall be achieved by connecting DigitalGND to ChassisGND conductive spring washers are recommended instead of isolating ones.



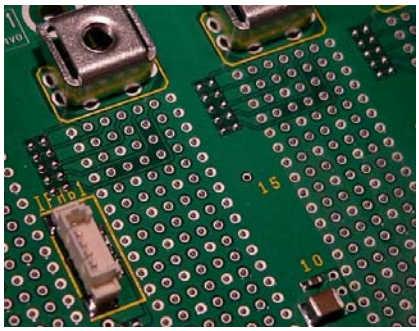
VI/O

Schroff CompactCPCI backplanes have a complete power plane for the VI/O voltage. The VI/O plane can be connected using a bridge on the power bugs to +3.3V or +5V.

By default, Schroff CompactPCI backplanes have VI/O connected to +5V with blue coding keys on P1. VI/O can also be set to 3,3V with the conversion kit **21101-658** (including 8 yellow keys and a tool) and change of the VI/O bridge position on the rear side of the backplane. Schroff CompactPCI backplanes are, on request, also avaiable with VI/O set to 3,3V.

Stiffener

The Schroff 6U CompactPCI backplanes are equiped with Stiffeners to reduce bending of the backplane during insertion and extraction of the cPCI cards to a minimum.



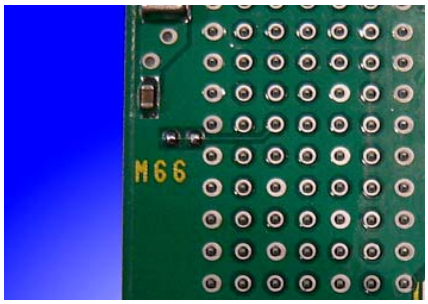
Geographical Addressing (GA)

Geographical addressing is set by default to start from number one from left (upper) position within the chassis. If more than one backplane shall be assembled, a change of geographical addresses can be made. Cut copper links in between SMD pads to open, apply a zero Ohm resistor to close. Package size shall be 0603. Position is labelled "nGA[x]" where "n" stands for slot# , and "x" for address#, see chapter „Mechanical and Electrical Interface".

Physical Slot Addresses

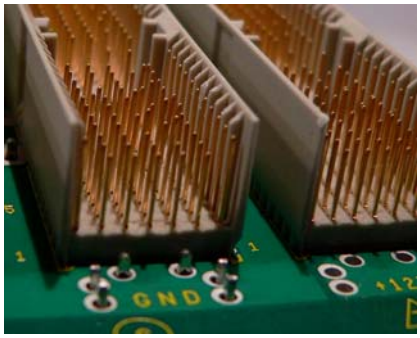
Physical Slot#	0(1)	1	2	3	4	5	6	7	8	9	10
GA[4] (J2-A22)	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
GA[3] (J2-B22)	GND	GND	GND	GND	GND	GND	GND	GND	open	open	open
GA[2] (J2-C22)	GND	GND	GND	GND	open	open	open	open	GND	GND	GND
GA[1] (J2-D22)	GND	GND	open	open	GND	GND	open	open	GND	GND	open
GA[0] (J2-E22)	GND	open	GND	open	GND	open	GND	open	GND	open	GND

Physical Slot#	11	12	13	14	15	16	17	18	19	20	21
GA[4] (J2-A22)	GND	GND	GND	GND	GND	open	open	open	open	open	open
GA[3] (J2-B22)	open	open	open	open	open	GND	GND	GND	GND	GND	GND
GA[2] (J2-C22)	GND	open	open	open	open	GND	GND	GND	GND	open	open
GA[1] (J2-D22)	open	GND	GND	open	open	GND	GND	open	open	GND	GND
GA[0] (J2-E22)	open	GND	open	GND	open	GND	open	GND	open	GND	open



66MHz Operation

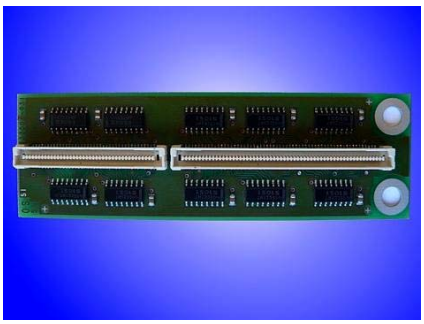
Schroff cPCI backplanes are designed in accordance with the requirements of cPCI Core Specification, Revision 3.0 (PICMG 2.0 R3.0). Up to 5 Slots 66MHz operation is possible, signal M66 is HIGH (open). Backplanes of higher slot count also fulfil the 66MHz operation requirements in terms of clock trace length and skew, but M66 is tied to GND to disable 66MHz operation by default. This link is made by a removable copper link. For test purposes, it can be opened and closed again by using a zero Ohm resistor of size 0603. For position of the link see chapter „Mechanical and Electrical Interface".



Hot Swap

Schroff cPCI backplanes fulfill the requirements for Basic Hot Swap of the Hot Swap Specification PICMG 2.1 R2.0. The signal BD_SEL# is tied to GND by a removable copper link. It can be replaced by a resistor-capacitor combination, both of package size 0603. Position is labelled "nB" where "n" stands for slot# , see chapter „Mechanical and Electrical Interface".

The P1 connector on Schroff cPCI backplanes has pin stagging needed for hot swap capabilities.



Termination

Termination on backplanes according to PICMG 2.0 R 3.0 is recommended in one case only. If, on a 8 slot backplane, strong buffers are used and only the system and the first adjacent slot are occupied and all others are empty.

Schroff has implemented a special connector on the 8 Slot cPCI backplanes, where a Termination Board can be assembled. For slot counts 4 to 7, this connector is used for assembling a cPCI Bridge, see chapter „Mechanical and Electrical Interface". Schroff is offering a 64-bit Termination Board, order code **23006-931**.

Connectors on Schroff CompactPCI Backplanes

Pin Assignment CPCI Connectors

Table 1: CompactPCI System Slot 64-Bit Connector Pin Assignment

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	SMB_SDA(11)	SMB_SCL(11)	SMB_ALERT#(11)	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND
15	GND	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)(2)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)(2)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)(2)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)(2)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	GND	V(I/O)(2)	C/BE[4]#	PAR64	GND
4	GND	V(I/O)(2)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3(3)	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2(3)	GND	CLK2	CLK3	SYSEN#(3)	GNT2#	REQ3#	GND
1(3)	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)(2),(4)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V(4)	AD[2]	GND
22	GND	AD[7]	GND	3.3V(4)	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)(2)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND(4)	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND(4)	PERR#	GND
16	GND	DEVSEL#	GND **(PCIXCAP)**	V(I/O)(2)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14	KEY AREA						
13	KEY AREA						
12	KEY AREA						
11	GND	AD[18]	AD[17]	AD[16]	GND(4)	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	GND	AD[23]	GND(4)	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)(2)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND(4)	AD[27]	GND
6	GND	REQ0#	GND	3.3V(4)	CLK0	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND(4)	GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#(13)	V(I/O)(2),(4)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V(4)	INTD#	GND
2	GND	BRSVP1A2(10)	5V	BRSVP1C2(10)	RSV(10)	RSVI(10)	GND
1	GND	5V	-12V	BRSVP1C1(10)	+12V	5V	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Table 2: CompactPCI Peripheral Slot 64-Bit Connector Pin Assignment (1)(10, 11)

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	RSV	RSV	RSV	RSV	RSV	GND
20	GND	RSV	RSV	RSV	GND	RSV	GND
19	GND	RSV	RSV	RSV	RSV	RSV	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	RSV	RSV	RSV	GND
16	GND	BRSVP2A16	BRSVP2B16	RSV	GND	BRSVP2E16	GND
15	GND	BRSVP2A15	GND	RSV	RSV	RSV	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)(2)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)(2)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)(2)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)(2)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#	GND	V(I/O)(2)	C/BE[4]#	PAR64	GND
4	GND	V(I/O)(2)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND
3(3)	GND	RSV	GND	RSV	RSV	RSV	GND
2(3)	GND	RSV	RSV	UNC(3)	RSV	RSV	GND
1(3)	GND	RSV	GND	RSV	RSV	RSV	GND
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)(2),(4)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V(4)	AD[2]	GND
22	GND	AD[7]	GND	3.3V(4)	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)(2)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND(4)	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND(4)	PERR#	GND
16	GND	DEVSEL#	GND **(PCIXCAP)**	V(I/O)(2)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#(6)	TRDY#	GND
14	KEY AREA						
13	KEY AREA						
12	KEY AREA						
11	GND	AD[18]	AD[17]	AD[16]	GND(4)	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL(6)	AD[23]	GND(4)	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)(2)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND(4)	AD[27]	GND
6	GND	REQ#	GND	3.3V(4)	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND(4)	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#(13)	V(I/O)(2),(4)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V(4)	INTD#	GND
2	GND	BRSVP1A2(10)	5V	BRSVP1C2(10	RSV(10)	RSV(10)	GND
1	GND	5V	-12V	BRSVP1C1(10	+12V	5V	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

Table 3: CompactPCI System Slot 32-Bit (Rear Panel I/O) Connector Pin Assignment

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND
20	GND	CLK5	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND
19	GND	GND	GND	SMB_SDA(11)	SMB_SCL(11)	SMB_ALERT#(11)	GND
18	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
17	GND	BP(I/O)	BP(I/O)	PRST#	REQ6#	GNT6#	GND
16	GND	BP(I/O)	BP(I/O)	DEG#	GND	BP(I/O)	GND
15	GND	BP(I/O)	BP(I/O)	FAL#	REQ5#	GNT5#	GND
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
4	GND	V(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
3(3)	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2(3)	GND	CLK2	CLK3	SYSEN#(3)	GNT2#	REQ3#	GND
1(3)	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)(2),(4)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V(4)	AD[2]	GND
22	GND	AD[7]	GND	3.3V(4)	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)(2)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND(4)	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMBSCL	IPMBSDA	GND(4)	PERR#	GND
16	GND	DEVSEL#	GND **(PCIXCAP)**	V(I/O)(2)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
14	KEY AREA						
13	KEY AREA						
12	KEY AREA						
11	GND	AD[18]	AD[17]	AD[16]	GND(4)	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	GND	AD[23]	GND(4)	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)(2)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND(4)	AD[27]	GND
6	GND	REQ0#	GND	3.3V(4)	CLK0	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND(4)	GNT0#	GND
4	GND	IPMBPWR	HEALTHY#(13)	V(I/O)(2),(4)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V(4)	INTD#	GND
2	GND	BRSVP1A2(10)	5V	BRSVP1C2(10)	RSV(10)	RSV(10)	GND
1	GND	5V	-12V	BRSVP1C1(10)	+12V	5V	GND
Pin	**Z**	**A**	**B**	**C**	**D**	**E**	**F**

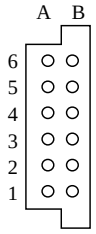
Table 4: CompactPCI Peripheral Slot 32Bit (Rear-Panel I/O) Connector Pin Assignments [1][3][8,9]

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
20	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
19	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
18	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
17	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
16	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
15	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
4	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
3	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
2	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
1	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)[2],[4]	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V[4]	AD[2]	GND
22	GND	AD[7]	GND	3.3V[4]	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)[2]	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND[4]	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND[4]	PERR#	GND
16	GND	DEVSEL#	GND **(PCIXCAP)**	V(I/O)[2]	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#[5]	TRDY#	GND
14	KEY AREA						
13	KEY AREA						
12	KEY AREA						
11	GND	AD[18]	AD[17]	AD[16]	GND[4]	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL[6]	AD[23]	GND[4]	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)[2]	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND[4]	AD[27]	GND
6	GND	REQ#	GND	3.3V[4]	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND[4]	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#[13]	V(I/O)[2],[4]	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V[4]	INTD#	GND
2	GND	BRSVP1A2[10]	5V	BRSVP1C2[10]	RSV[10]	RSV[10]	GND
1	GND	5V	-12V	BRSVP1C1[10]	+12V	5V	GND
Pin	Z	A	B	C	D	E	F

Notes for CompactPCI Pin Assignment Tables 1 through 4

1. These diagrams define the pin assignments from the front of the system chassis.
2. The V(I/O) signals are either 5 V or 3.3 V, depending on the system implementation.
3. Connector P2 pin C2 is grounded at the System Slot only. Peripheral slots leave C2 unconnected (UNC). Boards that use this signal (e.g., CPU boards that may be used in the System Slot or Peripheral Slot) shall provide a local pull-up to V(I/O). Boards designed for System Slot only use should tie this pin directly to the ground plane.
4. The following signals are long (level 3) pins in P1 for early power to hot swap boards: D3, D5, D7, D9, D11, D17, D19, D23, C4, C6, C22, C24.
5. Connector P1 pin D15 (BD_SEL#) is defined as a short length pin and is used for the final connection sequence by hot swap boards. Connector P1 pin B9 (IDSEL) is defined as a short length pin. Refer to PICMG 2.1, CompactPCI Hot Swap Specification for details.
6. These signals are defined as bussed reserve (BRSVPxxx) signals. They were defined as PCI cache signals SDONE# and SBO# (Defined in the PCI 2.1 Specification) in earlier revisions of this specification.
7. CompactPCI connector pin numbering is intentionally different from the connector manufacturer's pin numbering. This was done to allow the connectors to start at the bottom of the board and "grow" upward from J1/P1 through J5/P5.
8. BP(I/O) signals are defined as "long" tail connectors with 16.0 mm tails. Refer to IEEE 1101.11 for details. All other signals in P1 and P2 are defined to be "short" tail connectors with 4.5 mm tails.
9. BRSVPxxx signals accommodate PCI reserved signals. Bus segments shall bus these signals between connectors.
10. Usage of JTAG signals is discouraged. These signal definitions will be redefined in a future revision of the CompactPCI specification. Backplanes shall bus pins A2 (TCK), C2 (TMS) and C1 (TRST#) to all CompactPCI Slots. Pins D2 (TDO) and E2 (TDI) should be non-bussed.
11. System slot connector P2, pins C19 (SMBB_SDA), D19 (SMBB_SCL) and E19 (SMB_RSV) have been defined by the System Management Subcommittee as the appropriate rear-panel I/O pins to be used for a secondary I^2C bus local to the system board. Refer to the PICMG 2.9 System Management Specification for further information.
12. Signals IDSEL and BD_SEL# are connected to GND on the System Slot. The Dual Host Subcommittee may further define their use on the system slot.
13. P1 pin B4 is reserved for HEALTHY#. Backplane must leave this pin open and include a bypass capacitor, refer to section 3.2.10 and the CompactPCI Hot Swap Specification, PICMG 2.1 for details.

Utility-, Sense-, IPMB- Connectors

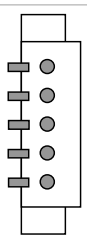


	A	B
6	nc	nc.
5	nc	-12V
4	+12V	3,3V
3	GND	+5V
2	FAL#	DEG#
1	nc	PRST#

Utility / SENSE Connector Pinout

Sense: Voltage rails +5V; 3,3V; +12V and GND of these connectors used for sense purposes. They should be connected to the backplane.
Some Power Supplies need at least a connection to GND, otherwise the outputs overrun.
FAL#: Signal driven by intelligent PSU's, at least one output has failed (is out of range).
DEG#: Signal driven by intelligent PSU's, PSU indicates that the supply is beginning to derate its power output.

Cable assy **23204-115** (350mm)
23204-116 (600mm)



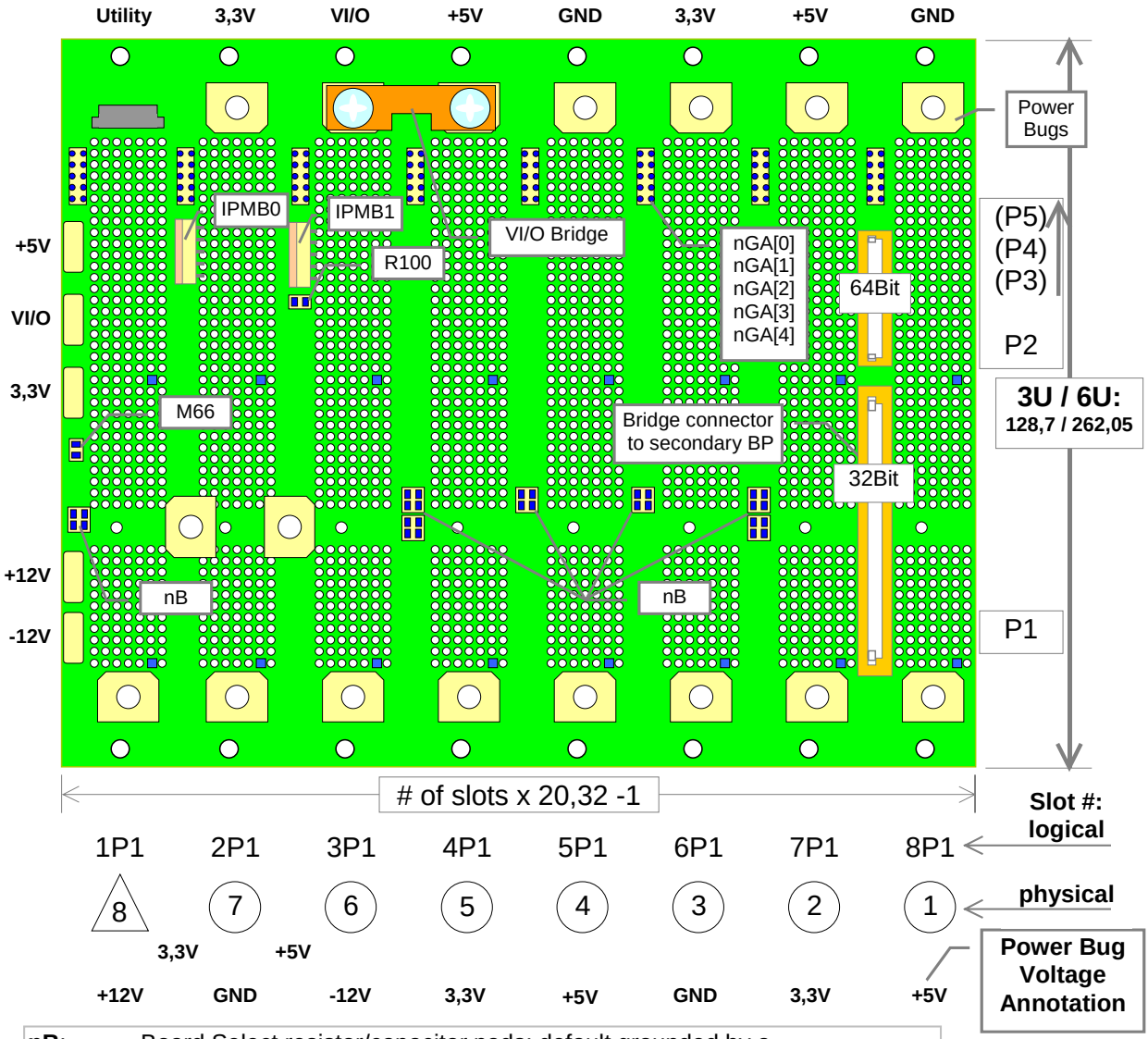
Pin	Signal
1	SCL
2	GND
3	SDA
4	Vsm
5	nc

IPMB Connector (Top view on connector)

Vsm (Power) can be connected to +5V by using zero Ohm resistor of size 0603 (R100).
Cable assy **23204-113** (750mm)

Mechanical and Electrical Interface

Schroff CPCI Backplane, Rear view, system slot right



nB: Board Select resistor/capacitor pads; default grounded by a removable copper link in outer layer;
n: slot number;

M66: 66MHz enabling line can be grounded using a 0603 zero Ohm resistor; default is grounded for backplanes comprised of more than 5 slots

Faston Blades on left hand side only available on Backplanes < 4 Slots:

- 3 Slot BPs: VI/O Power Bug on Top is replaced by 3,3V
  VI/O is set by a cable bridge between Fastons
  +/- 12V Fastons not available
- 1&2 Slot BPs: Faston available as shown
  no Power Bug on Top, replaced by IPMB0/1 connector

System Slot left Backplanes
placement of components and Power Bug annotation is mirrored

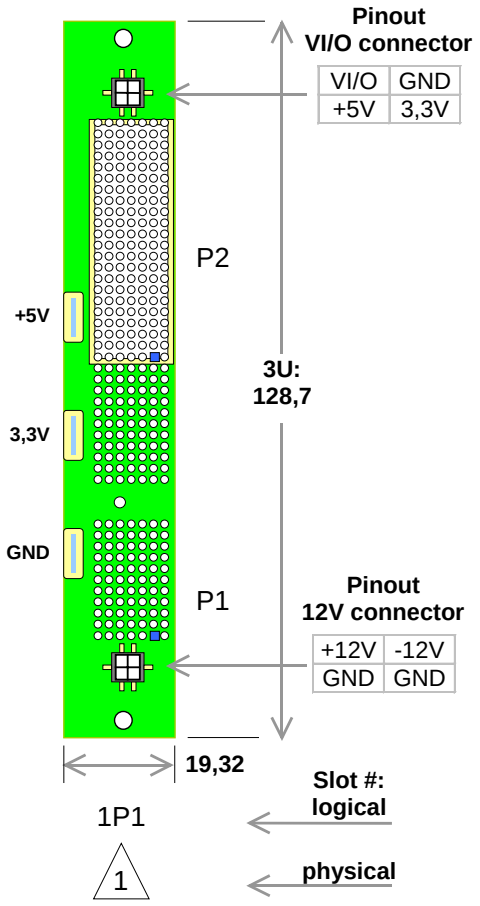
Schroff 1-Slot 3U cPCI Backplane, 23006-811

Purpose

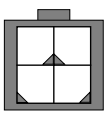
The 1 Slot Backplane provides power to a cPCI CPU Board. There are no bussed signals, connector P2 is compatible to the 32Bit System Slot pinout and comprises Rear I/O functionality

Mechanical and Electrical Interface

Rear view



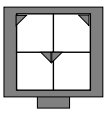
VI/O connector
top view on connector



VI/O	GND
+5V	3,3V

b/p connector: Molex # 43045-0418
free connector: Molex # 43025-0400
crimp contact: Molex # 43030-0007
(AWG 20-24, tin plated, Bag)

12V connector
top view on connector



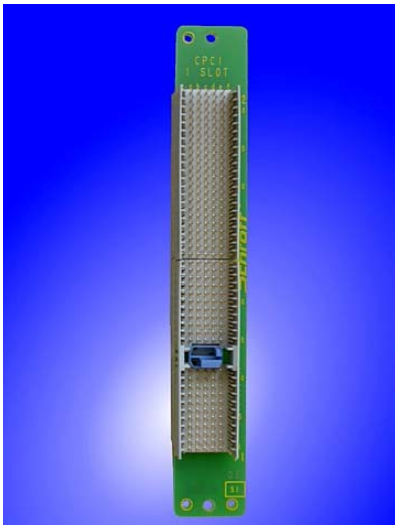
+12V	-12V
GND	GND

b/p connector: Molex # 43045-0418
free connector: Molex # 43025-0400
crimp contact: Molex # 43030-0007
(AWG 20-24, tin plated, Bag)

Power connectors
+5V, 3,3V & GND

6,3mm Faston blades,

fit with every 6,3mm Faston, available from different manufacturers



Schroff CompactPCI Backplanes for Special Applications

I/O Board

1 Slot backplane 3U for upper position in a 6U environment. Backplane includes connectors P4 and P5 with long pins and shrouds. Used if 3U backplane should be installed with 6U Boards. The I/O Board connects P4 and P5 from front to rear I/O board.

Order Code 23090-719

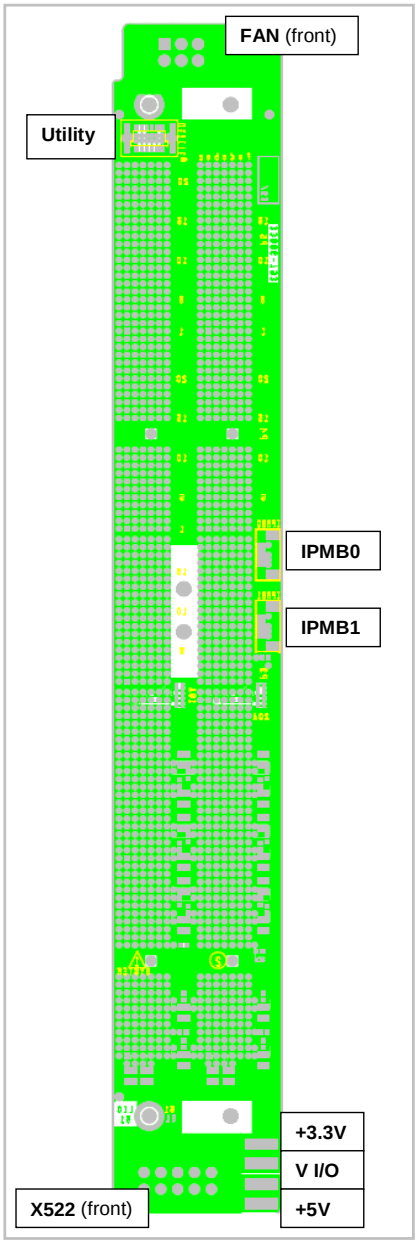
cPCI Backplane for 1U Vertical System (ATX)

Schroff has designed a special cPCI backplane that fit into a 1U system with vertical card cage. This backplane combines the 6U cPCI backplane, 64-bit cPCI bus, with 2 slot and Molex connectors for power supply (ATX) and fans.

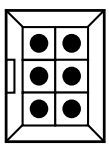
Features

- System slot left
- Placement of power connectors underneath the P1 connector row to reduce voltage drop to a minimum.
- Connectors for IPMB on board.
- Power bugs to connect VI/O to +5V or +3,3V

Order Code 23006-793, 2 Slot, 2 Minifit connectors.

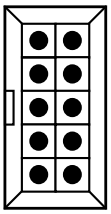


Fan Connector

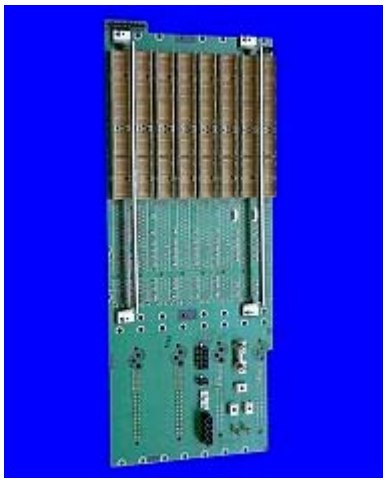


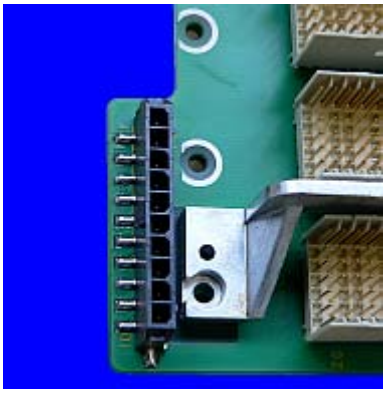
1	+5V
2	+12V
3	+12V
4	GND
5	GND
6	GND

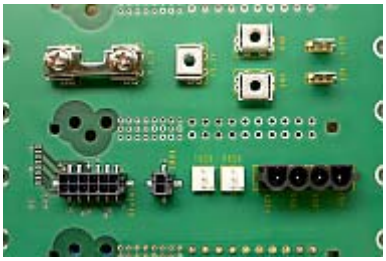
X522 Connector



1	+5V
2	GND
3	+3.3V
4	GND
5	+12V
6	+5V
7	GND
8	+3.3V
9	GND
10	-12V







cPCI Backplanes with P47 Connectors for 1 to 4U Vertical Systems

Schroff has designed special cPCI backplanes that fit into 1 to 4U systems with vertical card cage. These backplanes combine the 6U cPCI backplane, 64-bit cPCI bus, 2 to 8 slots and the P47 connectors for power supplies. Backplanes with 2 and 8 Slots are stock items, 4 and 6 slot on request.

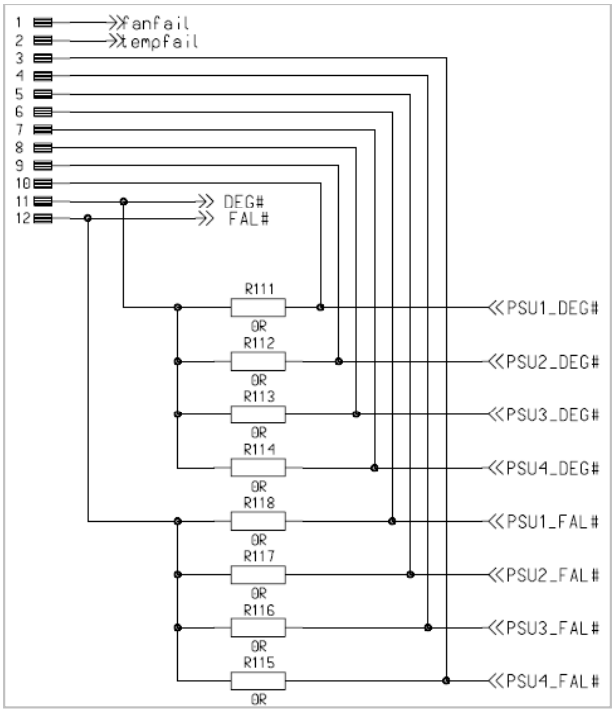
Features

- System slot left
- Placement of power connectors underneath the P1 connector row to reduce voltage drop to a minimum.
- Starting from 4 Slot backplane, two P47 connectors assembled.
- Redundant and parallel operation of power supplies possible.
- Connectors for IPMB, Utility, Disk- Drive, PSU-Status, fantray, temperature sensors, and Inhibit on board.
- Power bugs for every voltage present as optional power input or output (max. 30A per voltage).

Order Code

23006-794	2 Slot, 1 P47 connector
23006-795	4 Slot, 2 P47 connectors
23006-796	6 Slot, 2 P47 connectors, 3 connectors on request
23006-797	8 Slot, 2 P47 connectors, 3 or 4 connectors on request

Status



Fan

1	+12V
2	+12V
3	GND
4	GND
5	+5V
6	fanfail
7	tempfail
8	GND
9	Signal 1
10	Signal 2

Sig1

1	nc
2	GND
3	Signal 1

Sig2

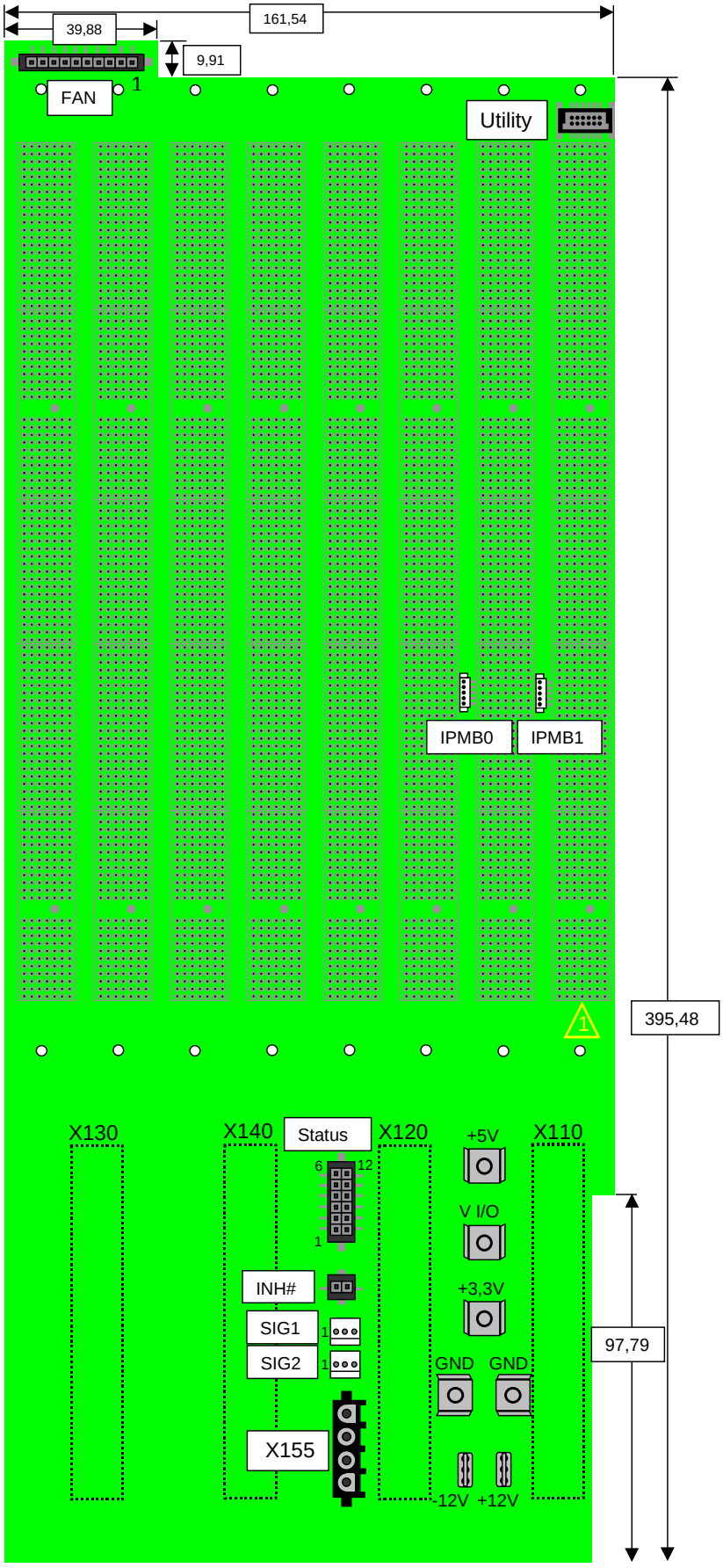
1	nc
2	GND
3	Signal 2

INH#

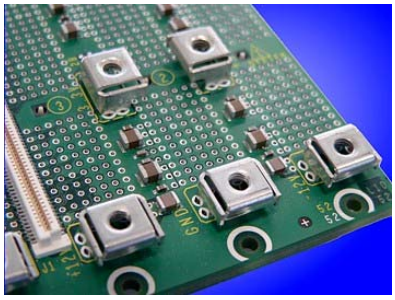
1	INH#
2	GND

X155

1	+5V
2	GND
3	GND
4	+12V


39,88
161,54
9,91
FAN
1
Utility
IPMB0
IPMB1
395,48
X130
X140
Status
X120
X110
+5V
6
12
1
V I/O
INH#
+3,3V
SIG1
SIG2
GND
GND
97,79
X155
-12V
+12V

Modular Power Concept



Power Bugs

Schroff cPCI backplanes are populated with specially designed power bugs. The power cables can be connected to the power bugs with cable lugs fastened with M4 screws. Each power bug can handle 30 Amps.

Schroff has designed various cables and power boards to be assigned to these power bugs. They provide interfaces for many different PSU types.

ATX Cable

Assembled on the power bugs of the CompactPCI backplanes, the ATX cable provides the mating connector for an ATX power supply.

Order Code 23204-121
ATX(M) to Ring Term 250mm

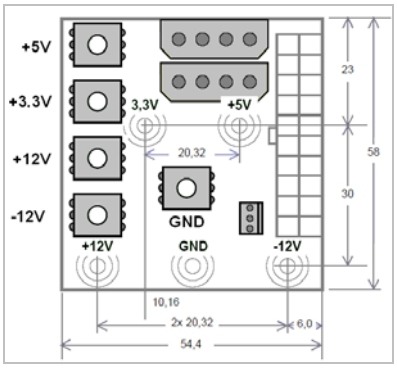
ATX Connector Pinout

+3.3V	11	1	+3.3V
-12V	12	2	+3.3V
GND	13	3	GND
INH#	14	4	+5V
GND	15	5	GND
GND	16	6	+5V
GND	17	7	GND
nc	18	8	FAL#
+5V	19	9	nc
+5V	20	11	+12V

pinout: top view on connector free connector: Molex # 39-01-2205 crimp terminal: Molex # 39-00-0039 (AWG 18-24, Bag)

CPCI Signal INH# uses a pin defined within the ATX spec as PS-ON; both (INH#, PS-ON) used to drive the PSU ON/OFF;

Logic Level is reversed; to drive PSU on, drive INH#: HIGH (PCMG 2.11 PSU's) PS-ON: LOW (ATX PSU's)

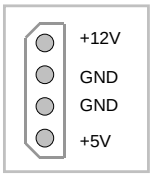


ATX Piggy Back

The Power Piggyback board can be used if ATX PSU's shall be connected to a Backplane. In this case the signal "INH#" at connector X15 shall be jumpered to GND that the ATX-PSU power up. Connector X15 is jumpered for ATX PSU's by default. If other PSU's like CPCI PSU's (acc. to PICMG 2.11) shall be used, than the jumper should be removed.

Oder Code 23098-100

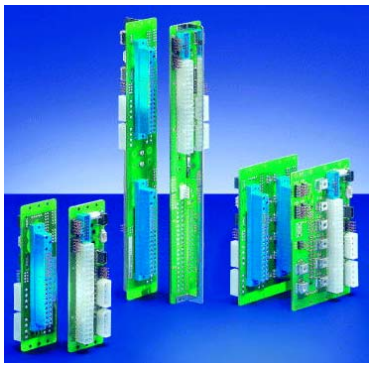
Disk Drive Power Connector (X5, X6)

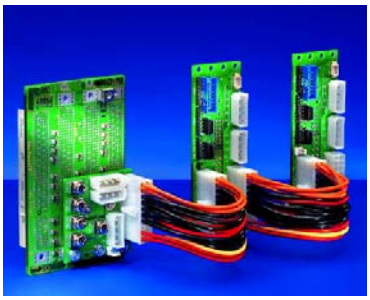


board connector: Molex # 15-24-4049
free connector: Molex # 15-24-3053
(IDC, AWG 16)

Connector X15

1: INH#
2: GND
3: FAL#





Power Backplane with P47 Connector

According to

PICMG 2.9	System Management Spezifikation
PICMG 2.11	Compact PCI Power Interface Spezifikation

Power backplane to support pluggable PSUs with P47 connector. Power backplane has 8/16HP width and can be assembled anywhere in the system. The power backplane can easily be connected electrically to the cPCI backplane by using the cables supplied with the power board. Power input to the power backplane with crimp contacts plugged directly into the P47 connectors. Parallel operation of 2 PSUs possible by connecting the current share bus on both power boards. 3U power backplane 8HP assembled with one P47 connector, 3U backplane 16HP with 2 P47, the 6U power backplane with 1 or 2 P47 connectors.

Order Code

23098-105	1 PSU Slot (8HP), 3U Board, connector for 1 PSU
23098-115	2 PSU Slots (16HP), 3U Board, connectors for 2 PSU´s
23098-116	1 PSU Slot, 6U Board (8HP), 1 PSU connector for one 6U PSU
23098-117	1 PSU Slot, 6U Board (8HP), 2 PSU connectors for two 3U PSU's

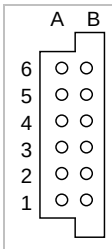
Sense Option

Sensing can be accomplished by three different options:

- using the Utility/Sense connector; all voltages are sensed (X7/8)
- using the Inhibit/Sense connector, the main voltages (+5V, 3,3V GND) can be connected to backplanes not assembled with the Utility connector by easy wiring (X25)
- only GND-Sense is connected to GND at the Power Board for minimum requirements of some PSU'S (Jumper X24)

GND-Sense Jumper (X24)

Some PSUs may require at least that sense return (GND Sense) is connected to GND to avoid output voltages out of range. For easy implementation, X24 can be shorted to connect GND Sense to GND of the power board



	A	B
6	nc	INH#
5	nc	-12V
4	+12V	3,3V
3	GND	+5V
2	DEG#	FAL#
1	nc	nc

Utility / SENSE Connector Pinout (X7, X8)

Sense pins referred to voltages +5V; 3,3V; +12V and GND of these connector are used for sense purposes. They should be connected to the backplane. The -12V pin is connected to the -12V power rail.
Some power supplies need at least a connection between GND_Sense and GND, otherwise the outputs overrun.

FAL#: Signal driven by intelligent PSUs, at least one output has failed (is out of range)
DEG#: Signal driven by intelligent PSUs, PSU indicates that the supply is beginning to derate its power output
INH#: Signal to turn the PSU outputs "on/off"; "open" or "HIGH": "on" / "LOW": "off"

cable assy **23204-115** (350mm)
cable assy **23204-116** (600mm)

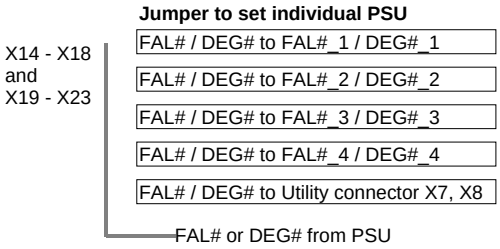
Pin Assignment X9

1. Part type: header with or w/o housing and latches, grid: 100mil
   recommendation for mating connector: any IDC connector for ribbon cable of a pitch of 50 mil (acc. to DIN 41651)
2. FAL#_n, DEG#_n: n is the number of an individual PSU
3. To set the PSU signal FAL# or respectively DEG# to an individual line use jumper according the schematic given in Figure 3.

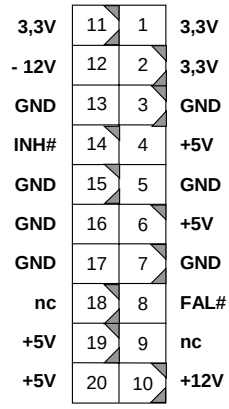
1	FAL#_1
2	FAL#_2
3	FAL#_3
4	FAL#_4
5	DEG#_1
6	DEG#_2
7	DEG#_3
8	DEG#_4
9	+3.3V share
10	+5V share
11	+12V share
12	GND
13	nc
14	nc

Setting individual FAL# & DEG# Signal

using Jumper array X14 - X18 for FAL#
using Jumper array X19 – X23 for DEG#



ATX Power Connector (X3, X4)



pinout: top view on connector

free connector: Molex # 39-01-2205
crimp terminal: Molex # 39-00-0039
(AWG 18-24, Bag)

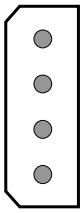
CPCI Signal INH# uses a pin defined within the ATX spec as PS-ON;
both (INH#, PS-ON) used to drive the PSU ON/OFF;
Logic Level is reversed; to drive PSU on, drive
INH#: HIGH (PCMG 2.11 PSU's)
PS-ON: LOW (ATX PSU's)

Pin Assignment Positronic P47 (X1)

Pin#	Signal Name	Description
1	V1	V1 Output (+5V)
2	V1	V1 Output (+5V)
3	V1	V1 Output (+5V)
4	V1	V1 Output (+5V)
5	RTN	V1 and V2 Return (GND)
5	RTN	V1 and V2 Return (GND)
7	RTN	V1 and V2 Return (GND)
8	RTN	V1 and V2 Return (GND)
9	RTN	V1 and V2 Return (GND)
10	RTN	V1 and V2 Return (GND)
11	RTN	V1 and V2 Return (GND)
12	RTN	V1 and V2 Return (GND)
13	V2	V2 Output (3,3V)
14	V2	V2 Output (3,3V)
15	V2	V2 Output (3,3V)
16	V2	V2 Output (3,3V)
17	V2	V2 Output (3,3V)
18	V2	V2 Output (3,3V)
19	RTN	V3 Return (GND)
20	V3	V3 Output (+12V)
21	V4	V4 Output (-12V)
22	RTN	Signal Return (GND)
23	RESERVED	Reserved
24	RTN V4	V4 Return (GND)
25	GA0	Geographic Address Bit 0
26	RESERVED	Reserved
27	EN#	Enable (set to GND)
28	GA1	Geographic Address Bit 1
29	V1ADJ	V1 Adjust
30	V1 SENSE	V1 Remote Sense
31	GA2	Geographic Address Bit 2
32	V2ADJ	V2 Adjust
33	V2 SENSE	V2 Remote Sense
34	S RTN	Sense Return
35	V1 SHARE	V1 Current Share
36	V3 SENSE	V3 Remote Sense
37	IPMB_SCL	System Management Bus
38	DEG#	Degrade Signal
39	INH#	Inhibit
40	IPMB_SDA	System Management Bus
41	V2 SHARE	V2 Current Share
42	FAL#	Fail Signal
43	IPMB_PWR	System Management Bus
44	V3 SHARE	V3 Current Share
45	CGND	Chassis Ground (safety ground)
46	ACN/+DC IN	AC Input – Neutral; +DC Input
47	ACL/-DC	IN AC Input – Line; =-DC Input

Disk Drive Power Connector (X5, X6)

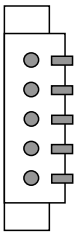
top view on connector



board connector: Molex # 15-24-4049
free connector: Molex # 15-24-3053
(IDC, AWG 16)

IPMB Connector (X2)

top view on connector

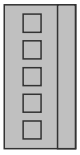


Pin	Signal
1	SCL
2	GND
3	SDA
4	Vsm
5	nc

cable 750mm: **23204 - 113**
free connector: Molex # 51021-0500
crimp contact: Molex # 50079-8100

Remote Connector (X25)

top view on connector



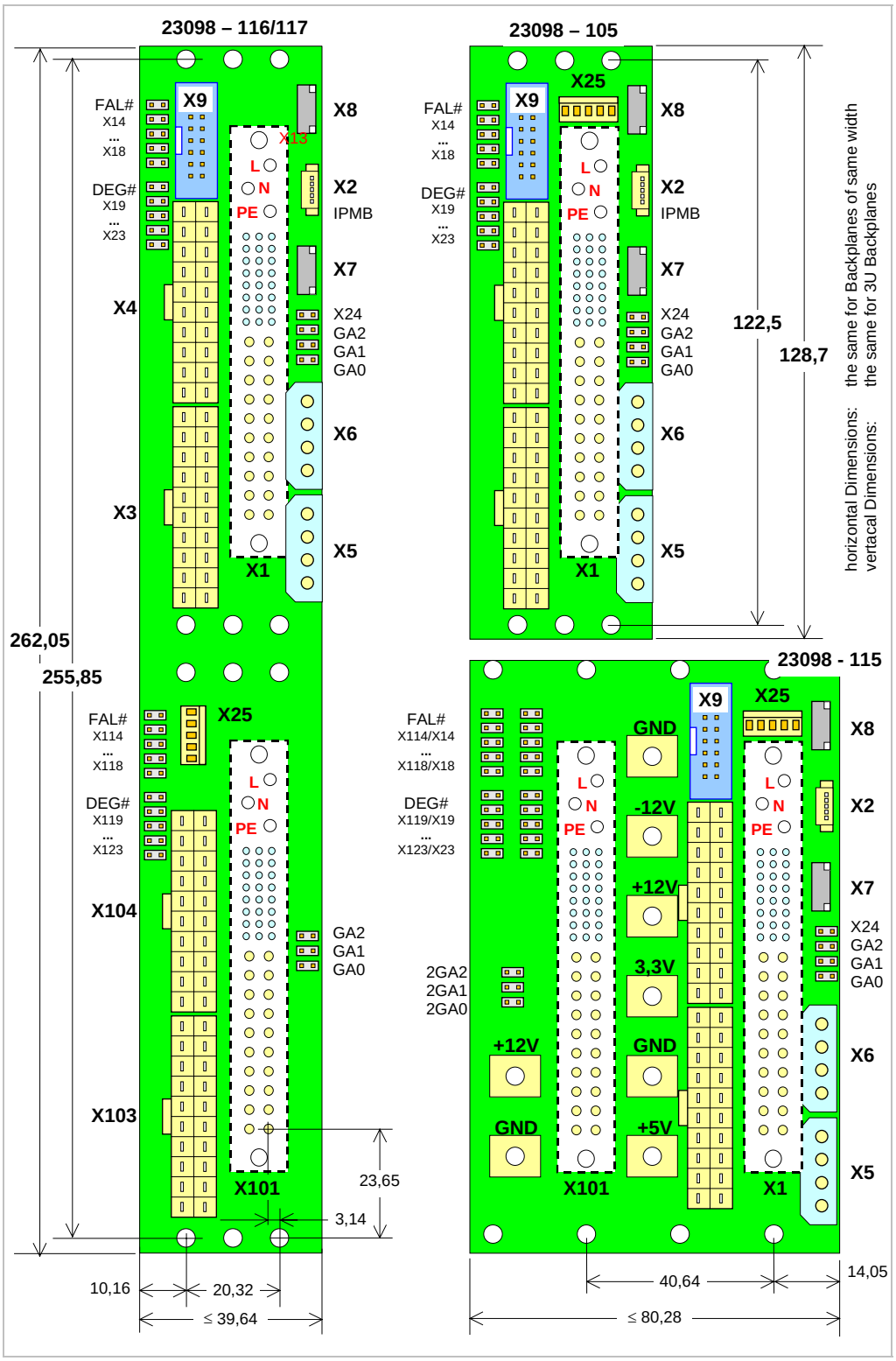
Pin	Signal
5	INH#
4	GND
3	+5V Sense
2	3,3V Sense
1	Sense Return (GND)

cable 750mm: **23204 - 114**
free connector: Tyco# 643814-5

Start-up of the Board

The cable tie of the power mains has to be opened and the crimp contacts have to be pushed into the dedicated connector chambers of X1;
Corresponding cable colours: brown: L (line); blue: N (neutral); green/yellow: PE (protective earth).
Cable length: 500mm, other end can be fitted with Faston crimp contacts (included in delivery).

Power Backplanes, view from rear, X1 is assembled from front



Available Backplanes and Accessories

CompactPCI Backplanes 3U, 32-bit, System Slot left

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-811	1	yes	+5V	33 / 66 MHz

CompactPCI Backplanes 3U, 64-bit, System Slot left

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-811	1	yes	+5V	33 / 66 MHz
23006-733	3	no	+5V	33 / 66 MHz
23006-734	4	no	+5V	33 / 66 MHz
23006-736	6	no	+5V	33 MHz
23006-738	8	no	+5V	33MHz

CompactPCI Backplanes 6U, 64-bit, System Slot left

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-765	5	yes	+5V	33 / 66 MHz
23006-768	8	yes	+5V	33 MHz

CompactPCI Backplanes 3U, 32-bit, System Slot right

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-811	1	yes	+5V	33 / 66 MHz
23006-812	2	yes	+5V	33 / 66 MHz
23006-813	3	yes	+5V	33 / 66 MHz
23006-814	4	yes	+5V	33 / 66 MHZ
23006-815	5	yes	+5V	33 / 66 MHz
23006-816	6	yes	+5V	33 MHz
23006-817	7	yes	+5V	33 MHz
23006-818	8	yes	+5V	33 MHz

CompactPCI Backplanes 3U, 32-bit, System Slot right, Secondary

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-824	4	yes	+5V	33 / 66 MHz
23006-827	7	yes	+5V	33 MHz

CompactPCI Backplanes 3U, 64-bit, System Slot right

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-811	1	yes	+5V	33 / 66 MHz
23006-833	3	no	+5V	33 / 66 MHz
23006-834	4	no	+5V	33 / 66 MHz
23006-835	5	no	+5V	33 / 66 MHz
23006-836	6	no	+5V	33 MHz
23006-837	7	no	+5V	33 MHz
23006-838	8	no	+5V	33MHz

CompactPCI Backplanes 3U, 64-bit, System Slot right, Secondary

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-854	4	no	+5V	33 / 66 MHz
23006-857	7	no	+5V	33 MHz

CompactPCI Backplanes 6U, 64-bit, System Slot right

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-862	2	Yes	+5V	33 / 66 MHz
23006-863	3	Yes	+5V	33 / 66 MHz
23006-864	4	Yes	+5V	33 / 66 MHz
23006-865	5	Yes	+5V	33 / 66 MHz
23006-866	6	Yes	+5V	33 MHz
23006-867	7	Yes	+5V	33 MHz
23006-868	8	Yes	+5V	33 MHz

CompactPCI Backplanes 6U, 64-bit, System Slot right, Secondary

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency
23006-884	4	Yes	+5V	33 / 66 MHz
23006-887	7	Yes	+5V	33 MHz

CompactPCI Backplanes „Special“ 6U, 64-bit, System Slot left

Article Number	Slot Count	Rear I/O	V I/O	Bus frequency	Power input
23006-792	2	Yes	+5V	33 / 66 MHz	1 x ATX
23006-794	2	Yes	+5V	33 / 66 MHz	1 x P47
23006-795 (3)	4	Yes	+5V	33 / 66 MHz	2 x P47
23006-796 (3)	6	Yes	+5V	33 MHz	2 x P47 (1)
23006-797	8	Yes	+5V	33 MHz	2 x P47 (2)

(1): 3 P47 connectors on request; (2) 3 or 4 P47 connectors on request; (3) Backplanes available on request

CompactPCI Bridges

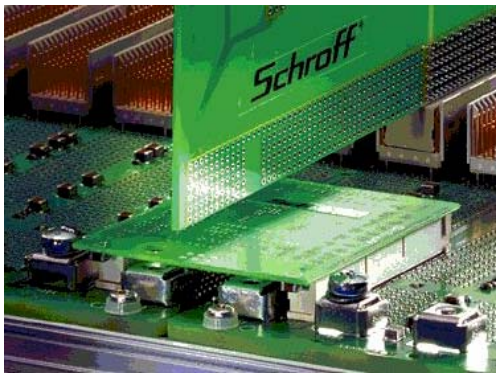
Article Number	Bus width / Orientation	Bus frequency	Description
23006-920	32-bit / right to left	33 / 66 MHz	Low profile
23006-922	64-bit / right to left	33 / 66 MHz	Low profile

Power Cable, Power Piggy, Power Backplanes

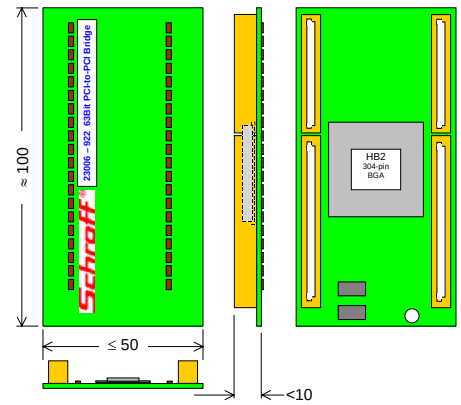
Article Number	Description
23204-121	Cable ATX(M) to Ring Terminals, 250mm length
23098-100	ATX Power Piggy
23098-105	Power Backplane 3U 8HP with 1 P47 connector
23098-115	Power Backplane 3U 16HP with 2 P47 connectors
23098-116	Power Backplane 6U 8HP with 1 P47 connector, upper position
23098-117	Power Backplane 6U 8HP with 2 P47 connectors, upper and lower position

Accessories

Article Number	Description
23204-110	Cable P47 Input Mains, 500mm length
23204-112	Cable ATX (F) to ring terminals, 250mm length
23204-113	Cable IPMB, 750mm length
23204-114	Cable Sense-Remote, 5-Way, 750mm length
23204-115	Cable Utility-Sense, 12-Way, 350mm length
23204-116	Cable Utility-Sense, 12-Way, 600mm length
23204-117	Cable Current Share, 14-Way, 100mm length
23204-134	Cable Remote AMP-MTA, 3-Way, 800mm length
21101-658	CPCI Conversion Kit, 8 yellow Coding keys plus tool, to set VI/O to 3,3V

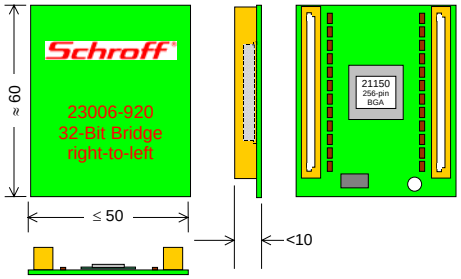


CPCI Rear Brick Bridge
64Bit, right-to-left



part#: **23006 - 922**

CPCI Rear Brick Bridge
32Bit, right-to-left



part#: **23006 - 920**

CompactPCI Bridge

CompactPCI has been designed to accommodate up to 8 modules on a bus segment. Installing a bridge module on a bus segment consumes one of the loads on the segment but creates a new bus segment with up to 7 additional modules. The bridge module handles all communication between the bus segments.

With the rear palette bridges from Schroff no valuable front slot is wasted. Due to the very low height of 10mm, even no rear I/O slot is wasted.

Schroff offers a 32-bit and a 64-bit rear palette bridge, both for system slot right backplanes. Both are based on the Intel 21154 PCI-to-PCI bridge Chip.

The maximum power consumption of this bridge module is 0.75W at +5V and 2.2 W at +3.3V. GND and the power supplies (+5V, +3.3V, +/-12V) are connected from the primary PCI bus to the secondary PCI bus. V(I/O) may be +3.3V or +5V on either side of the bridge. The bridge will automatically detect the bus voltage and adjust its I/O levels accordingly.

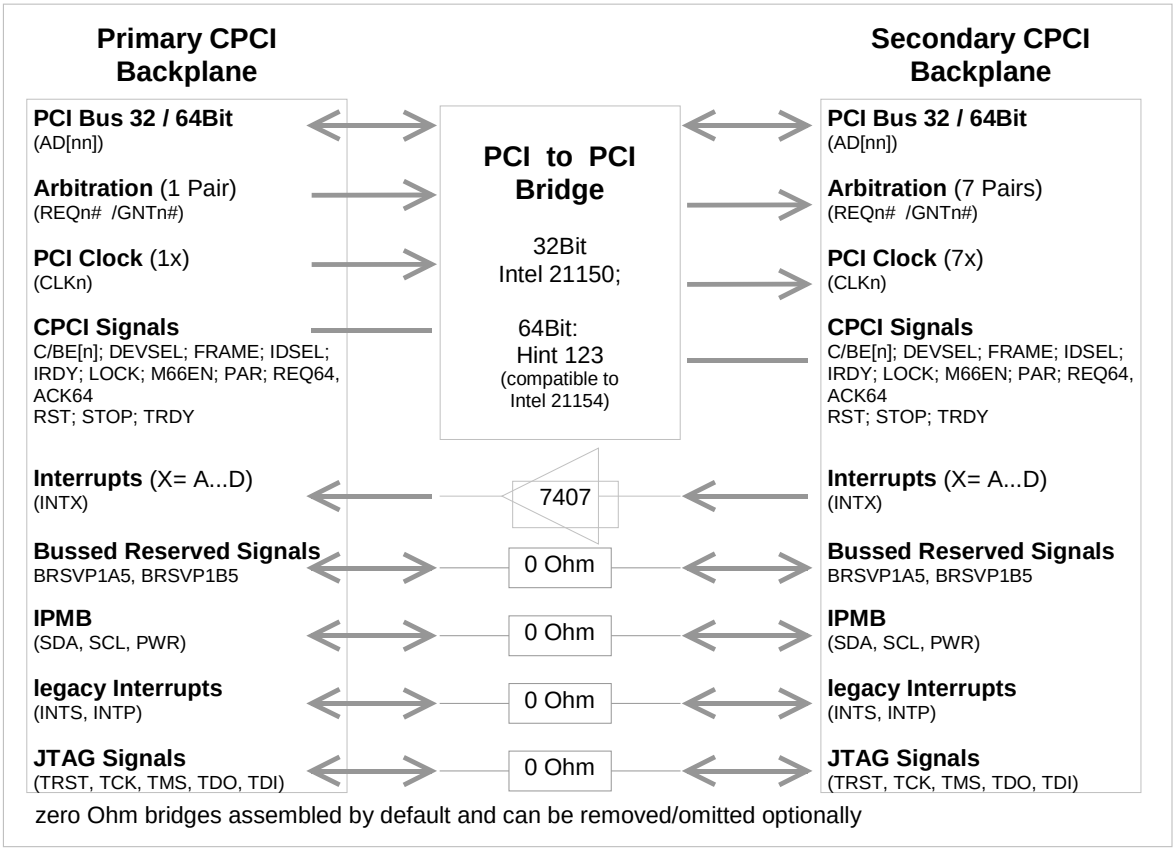
Power Supply of Backplanes: Both backplanes connected by the bridge are to be powered individually. The bridge is not to be used for bridging power. The bridge does not isolate the power rails of both backplanes. GND is connected by a sufficient number of pins in the connector to ensure signal integrity and a common GND potential on both backplanes.

VI/O There is no need to choose the VI/O voltage for the bridge. The bridge automatically takes the VI/O voltage of the primary and secondary side. Both backplanes can be set to different VI/O voltages, e.g. +5V on the primary side and 3,3V on the secondary side.

M66MHz Operation The bridge chips are capable of operating at 66MHz. The Bridges can operate with 33 MHz or 66MHz on primary and secondary side. It´s also possible to have the primary side operate at 66 MHz and the secondary at 33 MHz.

Mechanical Mounting Both backplanes should only be attached to the horizontal rails, but not fixed. The mounting screws of the backplane are not to be tightened until the bridge is plugged and fully seated!

Block Wiring Diagram



zero Ohm bridges assembled by default and can be removed/omitted optionally

Possible Bridge Configurations

3U, 32-bit, Systemslot right

Number of Slots	Configuration	Bus frequency	Articles needed
8	4 + 4 Slot	33 / 66 MHz or mixed	23006-814 + 23006-824 + 23006-920
9	5 + 4 Slot	33 / 66 MHz or mixed	23006-815 + 23006-824 + 23006-920
10	6 + 4 Slot	33 MHz	23006-816 + 23006-824 + 23006-920
11	7 + 4 Slot	33 MHz	23006-817 + 23006-824 + 23006-920
11	4 + 7 Slot	33 MHz or mixed	23006-814 + 23006-827 + 23006-920
12	5 + 7 Slot	33 MHz or mixed	23006-815 + 23006-827 + 23006-920
13	6 + 7 Slot	33 MHz	23006-816 + 23006-827 + 23006-920
14	7 + 7 Slot	33 MHz	23006-817 + 23006-827 + 23006-920
15	4 + 7 + 4 Slot	33 MHz or mixed	23006-814 + 23006-827 + 23006-824(1) + 2x 23006-920
16	5 + 7 + 4 Slot	33 MHz or mixed	23006-815 + 23006-827 + 23006-824(1) + 2x 23006-920
17	6 + 7 + 4 Slot	33 MHz	23006-816 + 23006-827 + 23006-824(1) + 2x 23006-920
18	7 + 7 + 4 Slot	33 MHz	23006-817 + 23006-827 + 23006-824(1) + 2x 23006-920
18	4 + 7 + 7 Slot	33 MHz or mixed	23006-814 + 2x 23006-827(1) + 2x 23006-920
19	5 + 7 + 7 Slot	33 MHz or mixed	23006-815 + 2x 23006-827(1) + 2x 23006-920
20	6 + 7 + 7 Slot	33 MHz	23006-816 + 2x 23006-827(1) + 2x 23006-920
21	7 + 7 + 7 Slot	33 MHz	23006-817 + 2x 23006-827(1) + 2x 23006-920

(1) If the backplane is used as tertiary backplane, the geographical address has to be changed. Please refer to chapter „Schroff CPCI Backplanes“, „Geographical addressing“.

3U, 64-bit, Systemslot right

Number of Slots	Configuration	Bus frequency	Articles needed
8	4 + 4 Slot	33 / 66 MHz or mixed	23006-834 + 23006-854 + 23006-922
9	5 + 4 Slot	33 / 66 MHz or mixed	23006-835 + 23006-854 + 23006-922
10	6 + 4 Slot	33 MHz	23006-836 + 23006-854 + 23006-922
11	7 + 4 Slot	33 MHz	23006-837 + 23006-854 + 23006-922
11	4 + 7 Slot	33 MHz or mixed	23006-834 + 23006-857 + 23006-922
12	5 + 7 Slot	33 MHz or mixed	23006-835 + 23006-857 + 23006-922
12	4 + 4 + 4 Slot	33 / 66 MHz or mixed	23006-834 + 2x 23006-854(1) + 2x 23006-922
13	6 + 7 Slot	33 MHz	23006-836 + 23006-857 + 23006-922
13	5 + 4 + 4 Slot	33 / 66 MHz or mixed	23006-835 + 2x 23006-854(1) + 2x 23006-922
14	7 + 7 Slot	33 MHz	23006-837 + 23006-857 + 23006-922
15	7 + 4 + 4 Slot	33 MHz	23006-837 + 2x 23006-854(1) + 2x 23006-922
15	4 + 4 + 7 Slot	33 MHz or mixed	23006-834 + 23006-854 + 23006-857(1) + 2x 23006-922
16	5 + 7 + 4 Slot	33 MHz or mixed	23006-835 + 23006-857 + 23006-854(1) + 2x 23006-922
16	5 + 4 + 7 Slot	33 MHz or mixed	23006-835 + 23006-854 + 23006-857(1) + 2x 23006-922
17	6 + 7 + 4 Slot	33 MHz	23006-836 + 23006-857 + 23006-854(1) + 2x 23006-922
18	7 + 7 + 4 Slot	33 MHz	23006-837 + 23006-857 + 23006-854(1) + 2x 23006-922
18	4 + 7 + 7 Slot	33 MHz or mixed	23006-834 + 2x 23006-857(1) + 2x 23006-922
19	5 + 7 + 7 Slot	33 MHz or mixed	23006-835 + 2x 23006-857(1) + 2x 23006-922
20	6 + 7 + 7 Slot	33 MHz	23006-836 + 2x 23006-857(1) + 2x 23006-922
21	7 + 7 + 7 Slot	33 MHz	23006-837 + 2x 23006-857(1) + 2x 23006-922

(1) If the backplane is used as tertiary backplane, the geographical address has to be changed. Please refer to chapter „Schroff CPCI Backplanes“, „Geographical addressing“.

6U, 64-bit, Systemslot right

Number of Slots	Configuration	Bus frequency	Articles needed
8	4 + 4 Slot	33 / 66 MHz or mixed	23006-864 + 23006-884 + 23006-922
9	5 + 4 Slot	33 / 66 MHz or mixed	23006-865 + 23006-884 + 23006-922
10	6 + 4 Slot	33 MHz	23006-866 + 23006-884 + 23006-922
11	7 + 4 Slot	33 MHz	23006-867 + 23006-884 + 23006-922
11	4 + 7 Slot	33 MHz or mixed	23006-864 + 23006-887 + 23006-922
12	5 + 7 Slot	33 MHz or mixed	23006-865 + 23006-887 + 23006-922
13	6 + 7 Slot	33 MHz	23006-866 + 23006-887 + 23006-922
14	7 + 7 Slot	33 MHz	23006-867 + 23006-887 + 23006-922
16	5 + 7 + 4 Slot	33 MHz or mixed	23006-865 + 23006-887 + 23006-884(1) + 2x 23006-922
17	6 + 7 + 4 Slot	33 MHz	23006-866 + 23006-887 + 23006-884(1) + 2x 23006-922
18	7 + 7 + 4 Slot	33 MHz	23006-867 + 23006-887 + 23006-884(1) + 2x 23006-922
18	4 + 7 + 7 Slot	33 MHz or mixed	23006-864 + 2x 23006-887(1) + 2x 23006-922
19	5 + 7 + 7 Slot	33 MHz or mixed	23006-865 + 2x 23006-887(1) + 2x 23006-922
20	6 + 7 + 7 Slot	33 MHz	23006-866 + 2x 23006-887(1) + 2x 23006-922
21	7 + 7 + 7 Slot	33 MHz	23006-867 + 2x 23006-887(1) + 2x 23006-922

(1) If the backplane is used as tertiary backplane, the geographical address has to be changed. Please refer to chapter „Schroff CPCI Backplanes“, „Geographical addressing“.

Mechanical and Climatic Parameters

	Backplanes	Bridges
Operating Temperature	-40°C - +85°C (-55°C - +125°C on request)	0 - +85°C (-40°C - +85°C on request)
Storage Temperature	-55°C - +105°C (-55°C - +155°C on request)	- 45°C - +70°C
Humidity	max 95%, not condensing (Conformal Coating on request)	
Flammability PCB, Connectors Ceramic caps	 UL 94 V-0 fire-proof	
Connectors Performance level per IEC 61076-4-101 Mechanical Durability (Mating Cycles) Total Insertion and Extraction Force (mating)	IEC 61076-4-101 (HardMetric 2mm Grid) level 2 (level 1 on request) >250 cycles (> 500 cycles on request) < 0,75 N / Pin	
Vibration acc. DIN 41640 Part 15	10Hz – 500Hz (5Hz – 2000Hz on request) 5g rms (20g rms on request)	
Shock (10 pulses each direction x,y,z)	10g, 6ms	
Low Pressure / Altitude (max Board voltage per single isolation gap doesn't exceed 12V)	no restrictions	
Construction	10 - Layer Stripline	
Dimensions (mm) Width (pl. see Dwg.) Height 3U / 6U Thickness	 20,32mm x #Slots-1mm 128,7mm / 262,05mm 3,2mm +/- 0,2mm	 50mm 100mm (64-bit), 60mm (32-bit) 10mm

Electrical Parameters

Specifications	PICMG 2.0 R3.0 CPCI Core Specification PICMG 2.1 CPCI Hot Swap Specification PICMG 2.6 Bridging Specification PICMG 2.9 System Management Bus Spec. PICMG 2.10 Keying Specification
Service Life: MTBF acc. to MIL HDBK 217F, cond.: 25°C, ground, benign 6U 8-Slot	more than 600.000h
Characteristic Impedance PCI traces Clock traces Clock trace length	65 Ω ± 10 % 65 Ω ± 10 % 160 +/- 1,0mm; acc. to 66MHz spec for all backplanes
Ohmic Resistance of Signal Tracks PCI traces	< 95mΩ/Slot
Hot Swap	supported
Termination (only 8 Slot Backplanes)	Schottky diodes (on request), plugable termination board
Power input	Power bugs for wiring or special Adapter Board to use an ATX cable; this board can act as a power distribution star point within the Systems
max. Current carrying Capacity 5V/GND 3,3V/GND	8 A per Slot 10 A per Slot
max. Voltage Drop between any two points on the backplane on +5V or +3,3V	< 40mV
VI/O bridging (default)	+5V (default), blue key; 3,3V optional (yellow key) field changeable, using M4 screws and a bus bar (fixed during bp assy by using a Power Bug cable using Faston crimp contacts on request)
Clock frequency	33 MHz, 66 MHz up to 5 Slots; on higher Slot number M66EN can by enabled for test purposes (cut a copper link on rear)
PCI Bus Width	32bit; 64bit, check part#
Data Transfer Rate (peak) 33 MHz 66 MHz	132 Mbyte/s (32 bit) / 264 Mbyte/s (64 bit) 264 Mbyte/s (32 bit) / 528 Mbyte/s (64 bit)
Bridging of Backplanes	backplane of slot numbers equal or higher than 4 up to 7 Slots can be bridged, see chapter Possible bridge configurations