MIC1232

5V Voltage Supervisor with Manual Reset, Watchdog Timer, and Dual Reset Outputs

Features

- Low-Current Version of DS1232, MAX1232, TC1232, CAT1232
- Low Current: 18 µA (typ.), 40 µA (max.)
- Selectable Threshold (TOL): 5% or 10% of 5V
- Selectable Watchdog Timer (TD): 150 ms, 600 ms, 1.2s
- Power OK/Reset Time Delay: 250 ms (min.)
- Debounced Pushbutton Reset Input (/PBRST)
- Dual Complementary Reset Outputs
  - Active-Low, Open-Drain Reset Output
  - Active-High, Push-Pull Reset Output
- Available in 8-lead SOIC and 8-Lead PDIP Packages
- –40°C to +85°C Temperature Range
- Pin-for-Pin Compatible with MIC1832, DS1832, CAT1832

Applications

- Automotive Systems
- Intelligent Systems
- Critical Microprocessor Power Monitoring
- Battery Powered Computers
- Controllers

General Description

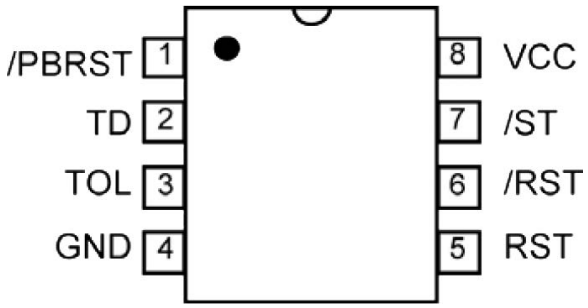
The MIC1232 is a low-current microprocessor supervisor for monitoring 5V systems. The device features logic selectable (TOL) reset thresholds of 5% or 10% of 5V; a pushbutton reset input (/PBRST); a watchdog timer with three-state selectable (TD) timeout periods of 150 ms, 600 ms, or 1.2s; a fixed reset timeout period of 250 ms (min.); and active-low open-drain reset (/RST) and active-high push-pull reset (RST) outputs. The /RST output maintains a valid reset condition for V_{CC} as low as 1.4V.

The MIC1232 asserts a reset condition if the supply voltage drops below the reset threshold, the pushbutton reset is asserted low, or the watchdog timer does not see a high-to-low transition on the watchdog timer input within the watchdog timer period. A reset condition is held for the reset timeout period of 250 ms (min.) after the pushbutton input is released or after the supply voltage increases above the reset threshold voltage.

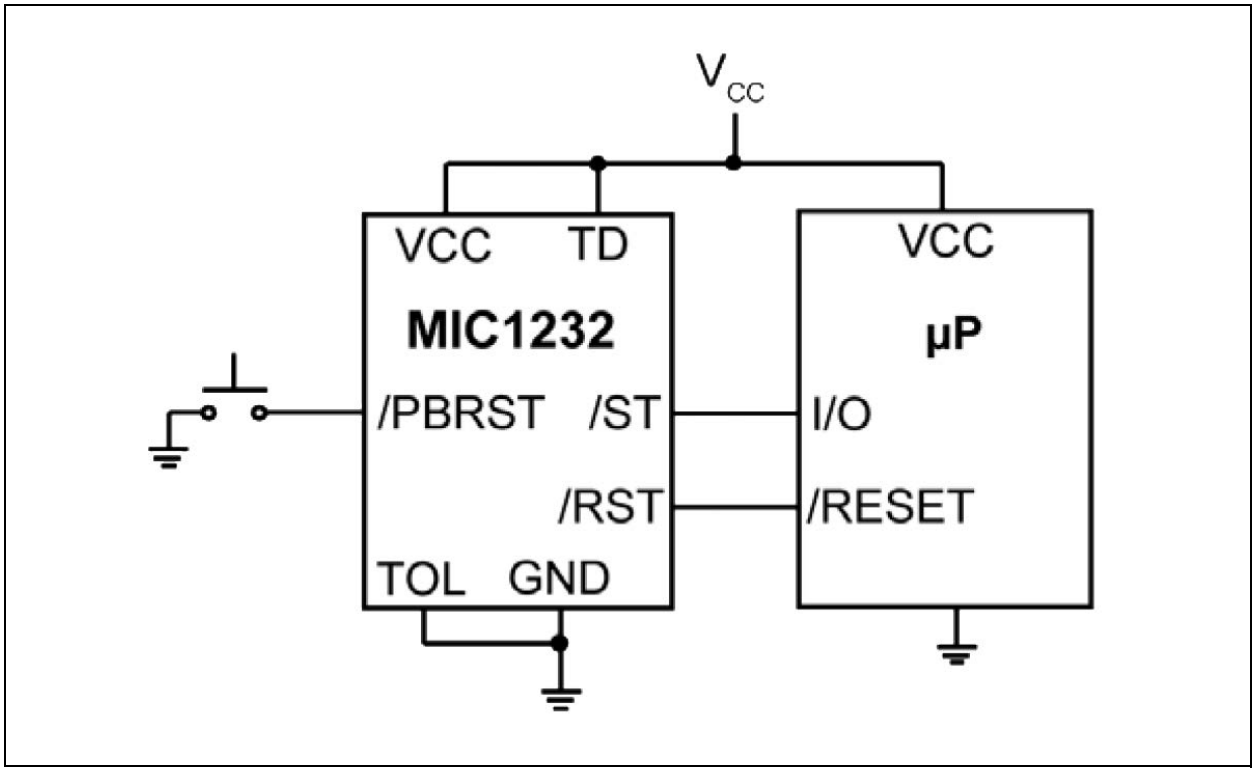
The MIC1232 is a drop-in replacement for the DS1232, MAX1232, and TC1232. It consumes a low 18 µA (typ.) of supply current, 40 µA (max.). This is one-tenth the max current of the DS1232, and one-quarter the max current of the MAX1232 and TC1232. It operates over the –40°C to +85°C temperature range and is available in the 8-lead SOIC and PDIP packages.

Package Types

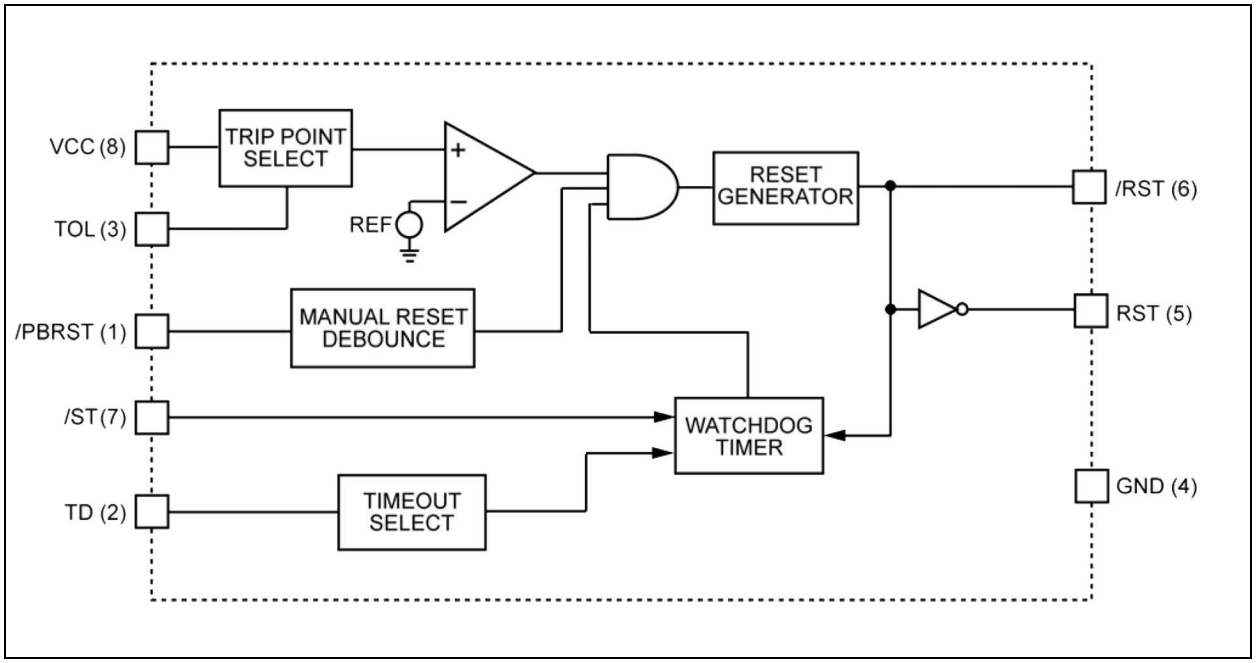
MIC1232
8-Lead SOIC (M) or
8-Lead PDIP (N)



Typical Application Circuits



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Terminal Voltage

V_{CC} ..... −0.3V to +6.0V
All other inputs ..... −0.3V to (V_{CC} + 0.3V)

Input Current

V_{CC} ..... 250 mA
GND, all other inputs ..... 25 mA
ESD Rating ..... Note 1

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100 pF.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V to 5.5V; T_A = Operating Temperature Range; **bold** values indicate –40°C ≤ T_A ≤ +85°C, unless noted.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range	V_{CC}	4.5	—	5.5	V	—
Supply Current	I_{CC}	—	18	**40**	µA	Note 1
/ST and /PBRST Input Levels	V_{IH}	**2.0**	—	**V_{CC} + 0.3**	V	Note 2
	V_{IL}	**–0.3**	—	**0.8**	V	—
Input Leakage	I_{IL}	—	—	**±1**	µA	—
Output Source Current, RST	I_{SOURCE}	**1.0**	10	—	mA	V_{OH} = 2.4V
Output Sink Current, /RST. RST	I_{OSK}	**2.0**	10	—	mA	V_{OL} = 0.4V
VCC 5% Trip Point (Reset Threshold Voltage)	V_{CCTP}	**4.5**	4.62	**4.74**	V	TOL = GND
VCC 10% Trip Point (Reset Threshold Voltage)	V_{CCTP}	**4.25**	4.37	**4.49**	V	TOL = V_{CC}
Input Capacitance, /ST, TOL	C_{IN}	—	—	5	pF	Note 3
Output Capacitance, /RST, RST	C_{OUT}	—	—	7	pF	Note 3

Note 1: I_{CC} is measured with outputs open and inputs within 0.5V of supply rails.
2: /PBRST has an internal pull-up resistor to V_{CC} (typ. 40 kΩ).
3: Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

V_{IN} = 4.5V to 5.5V; T_A = Operating Temperature Range; bold values indicate –40°C≤ T_A ≤ +85°C, unless noted.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
/PBRST Min. Pulse Width	t_{PB}	**20**	—	—	ms	/PBRST = V_{IL} (Note 1)
/PBRST Delay	t_{PBD}	**1**	4	**20**	ms	—
Reset Active Time	t_{RST}	**250**	610	**1000**	ms	—
/ST Pulse Width	t_{ST}	**20**	—	—	ns	—
/ST Timeout Period	t_{TD}	**62.5**	150	**250**	ms	TD = 0V
		250	600	**1000**	ms	TD = Open
		500	1200	**2000**	ms	TD = V_{CC}
VCC Fall Time	t_F	**10**	—	—	µs	—
VCC Rise Time	t_R	**0**	—	—	ns	—
VCC Detect to /RST Low and RST High	t_{RPD}	—	50	**150**	µs	V_{CC} Falling (Note 2)
VCC Detect to /RST Low and RST Low	t_{RPD}	**250**	610	**1000**	ms	V_{CC} Falling (Note 3)

Note 1: /PBRST must be held low for a minimum of 20ms to guarantee a reset.

2: V_{CC} falling at 1.66mV/µs.

3: /RST has an open drain output

TEMPERATURE SPECIFICATIONS

Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range (Note 1)	T_J	–40	—	+85	°C	—
Lead Temperature	—	—	—	+300	°C	Soldering, 10 seconds
Storage Temperature	T_S	–65	—	+150	°C	—

Note 1: The device is not guaranteed to function outside its operating ratings.

Timing Diagrams

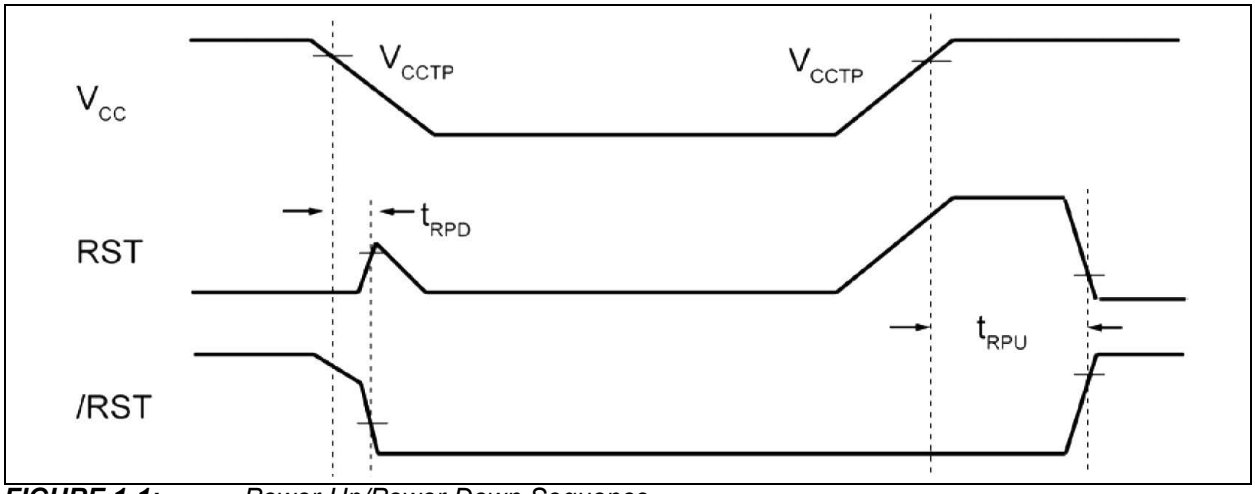


FIGURE 1-1: *Power-Up/Power-Down Sequence.*

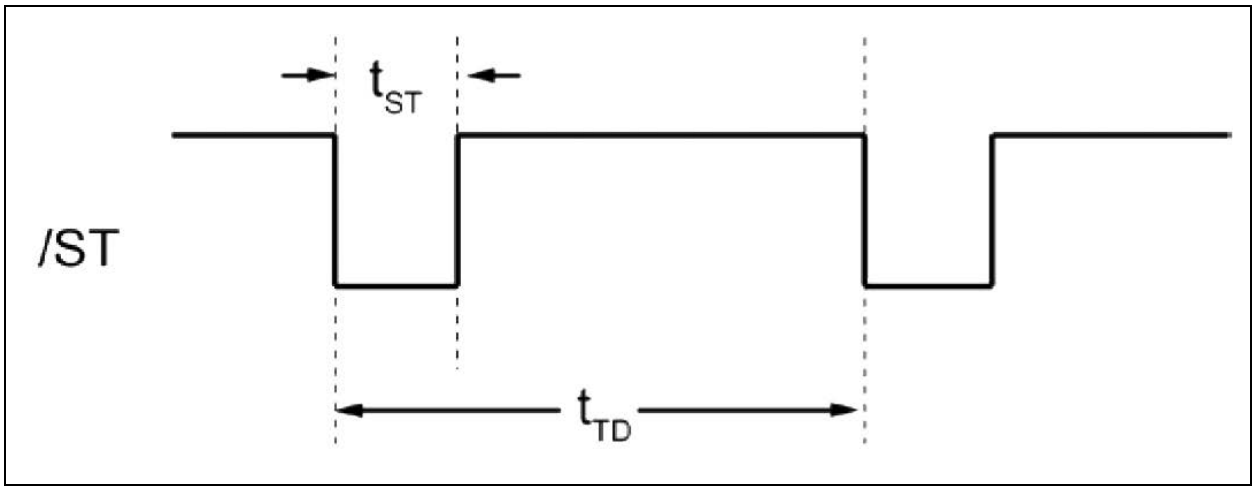


FIGURE 1-2: *Watchdog Input.*

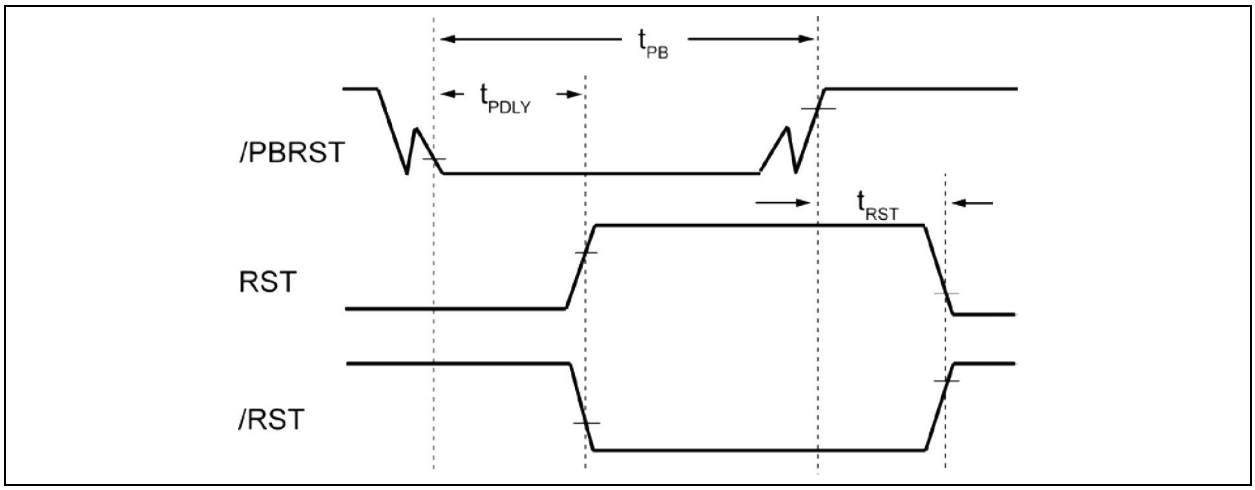


FIGURE 1-3: *Pushbutton Reset.*

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	/PBRST	Pushbutton Reset input: This input is debounced and can be driven with external logic signals or by using a mechanical pushbutton to actively force a reset. All pulses less than 1ms in duration on the /PBRST pin are ignored; any pulse with a duration of 20ms or greater is guaranteed to cause a reset.
2	TD	Time Delay input: This input selects the timebase used by the watchdog timer. When TD = 0V, the watchdog timeout period is set to a nominal value of 150ms. When TD = open, the watchdog timeout period is set to a nominal value of 600ms. When TD = VCC, the watchdog period is 1.2s nominally.
3	TOL	Tolerance Select input: This input selects whether 5% or 10% of VCC is used as the reset threshold voltage. When TOL = 0V, the 5% tolerance level is selected and when TOL = VCC, a 10% tolerance level is selected.
4	GND	IC ground pin, 0V reference.
5	RST	RST is asserted high if either VCC goes below the reset threshold, the watchdog times out, or /PBRST is pulled low for a minimum of 20ms. RST remains asserted for one reset timeout period after VCC exceeds the reset threshold, after the watchdog times out, or after /PBRST goes high.
6	/RST	/RST is asserted low if either VCC goes below the reset threshold, the watchdog times out, or /PBRST is pulled low for a minimum of 20ms. /RST remains asserted for one reset timeout period after VCC exceeds the reset threshold, after the watchdog times out, or after /PBRST goes high. Open-drain output.
7	/ST	Input to watchdog timer. If /ST does not see a transition from high to low within the watchdog timeout period, RST and /RST will be asserted.
8	VCC	Primary supply input, +5V.

3.0 APPLICATION INFORMATION

3.1 Power Monitor

The /RST and RST pins are asserted whenever V_{CC} falls below the reset threshold voltage determined by the TOL pin. A 5% tolerance level (4.62V reset threshold voltage) can be selected by connecting the TOL pin to ground. A 10% tolerance level can be selected by connecting the TOL pin to the VCC pin. The reset pins will remain asserted for a period of 250ms after V_{CC} has risen above the reset threshold voltage. The reset function ensures that the microprocessor is properly reset and powers up into a known condition after a power failure. /RST will remain valid with V_{CC} as low as 1.4V.

3.2 Watchdog Timer

The microprocessor can be monitored by connecting the /ST pin (watchdog input) to a bus line or I/O line. If a high-to-low does not occur on the /ST pin within the watchdog timeout period determined by the TD pin (see the Electrical Characteristics Table), the /RST and the RST will remain asserted for 250 ms. A minimum pulse of 20 ns or any transition high-to-low on the /ST pin resets the watchdog timer. The watchdog timer is reset if /ST sees a valid transition within the watchdog timeout period.

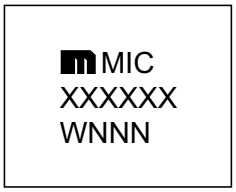
3.3 Pushbutton Reset Input

The /PBRST input can be driven with a manual pushbutton switch or with external logic signals. The input is internally debounced and requires an active low signal to force the reset outputs into their active states. The /PBRST input recognizes any pulse that is 20 ms or longer in duration and ignores all pulses that are less than 1 ms in duration.

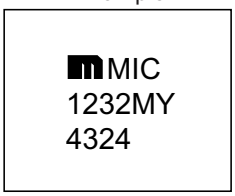
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

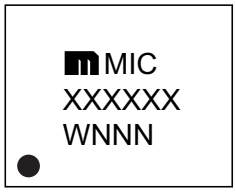
8-Lead SOIC*



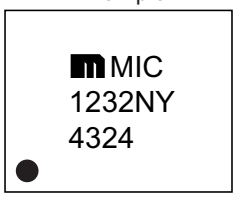
Example



8-Lead PDIP*



Example

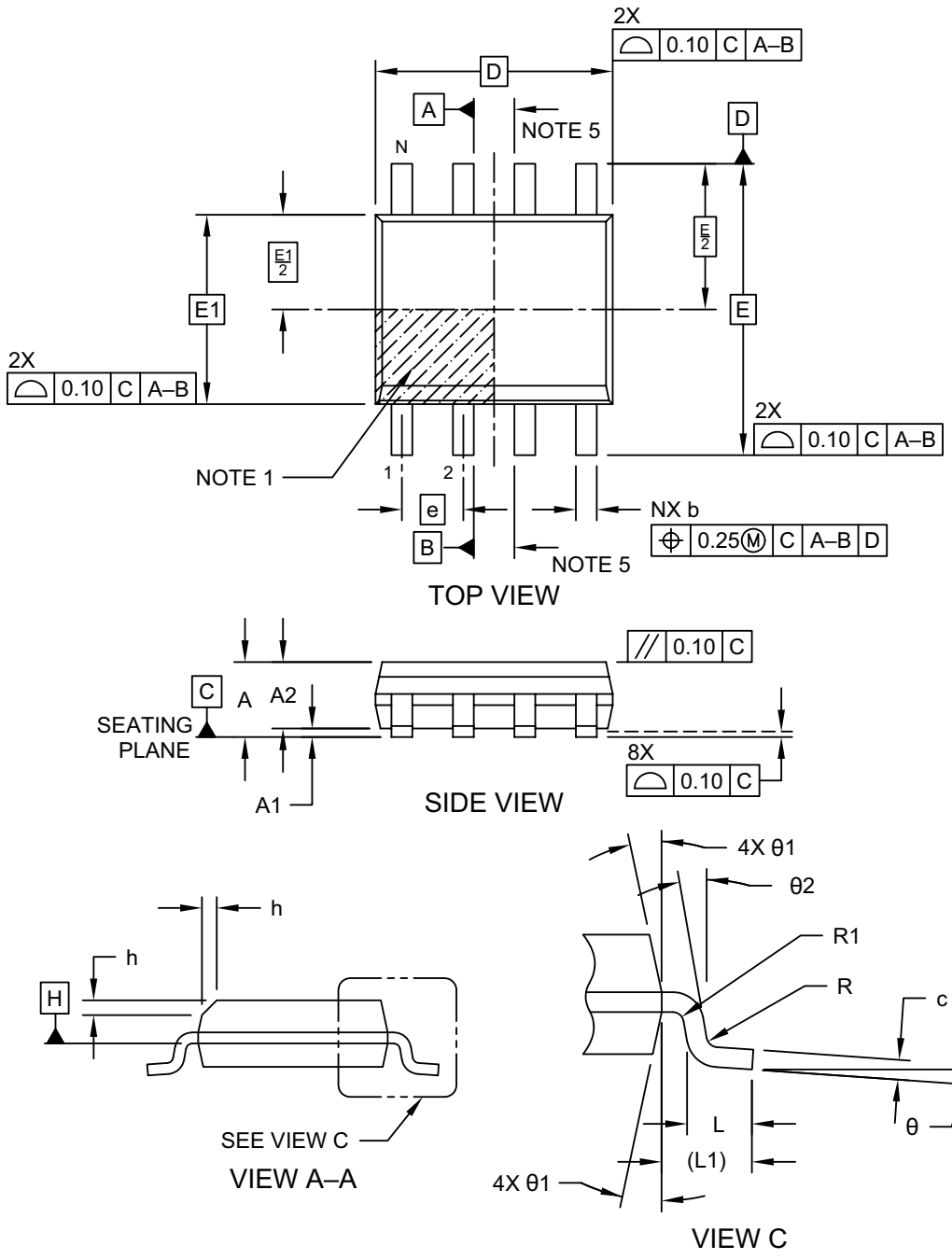


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (¯) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N.

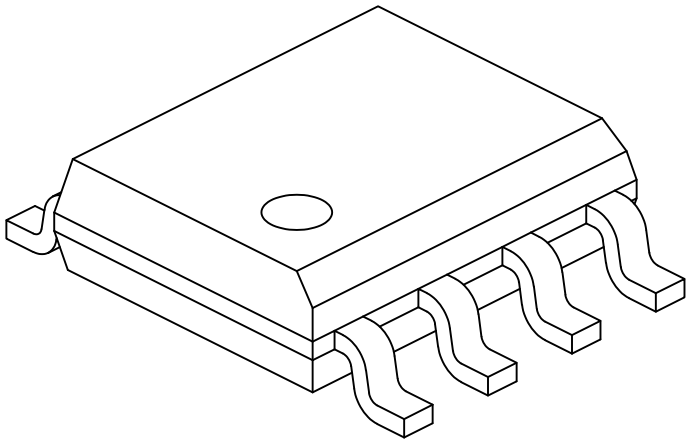
8-Lead 3.9 mm SOIC Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



8-Lead 3.9 mm SOIC Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



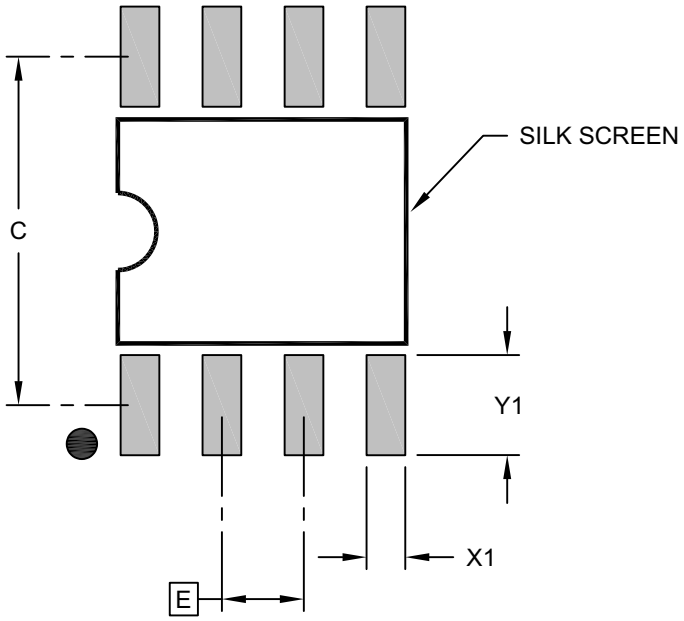
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	8°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

8-Lead 3.9 mm SOIC Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

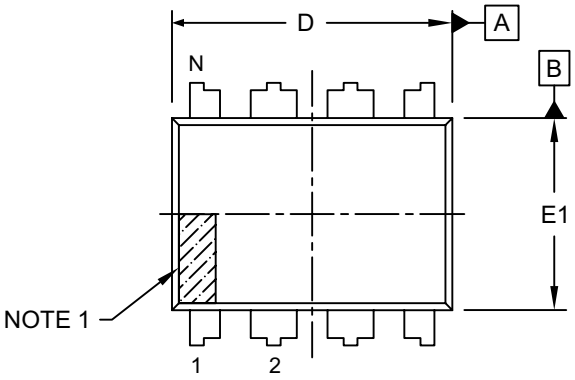
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

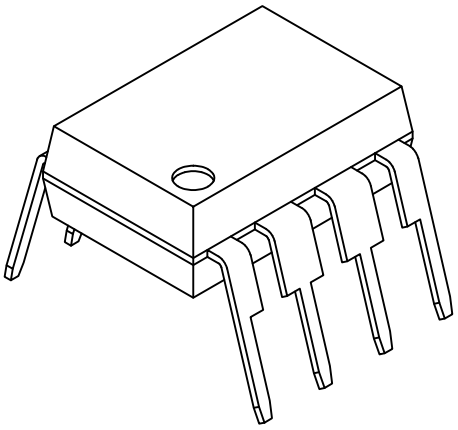
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

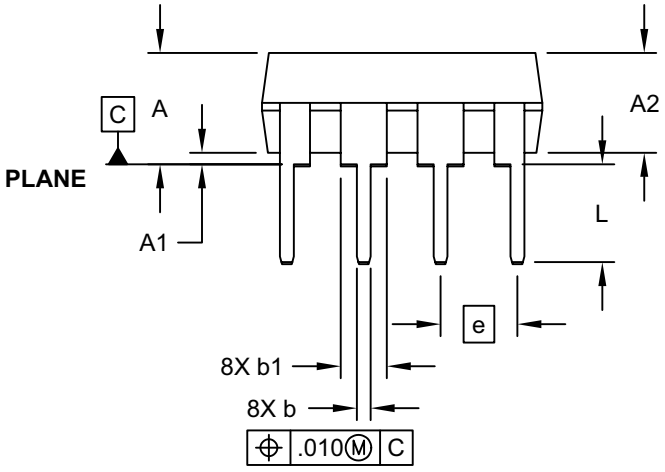
8-Lead 0.300 in PDIP Package Outline and Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

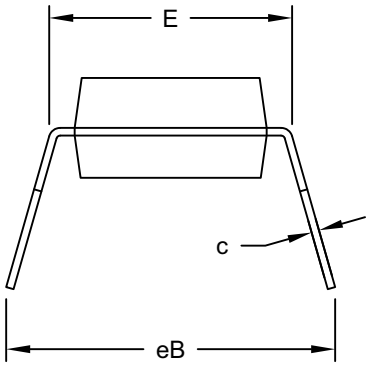


TOP VIEW





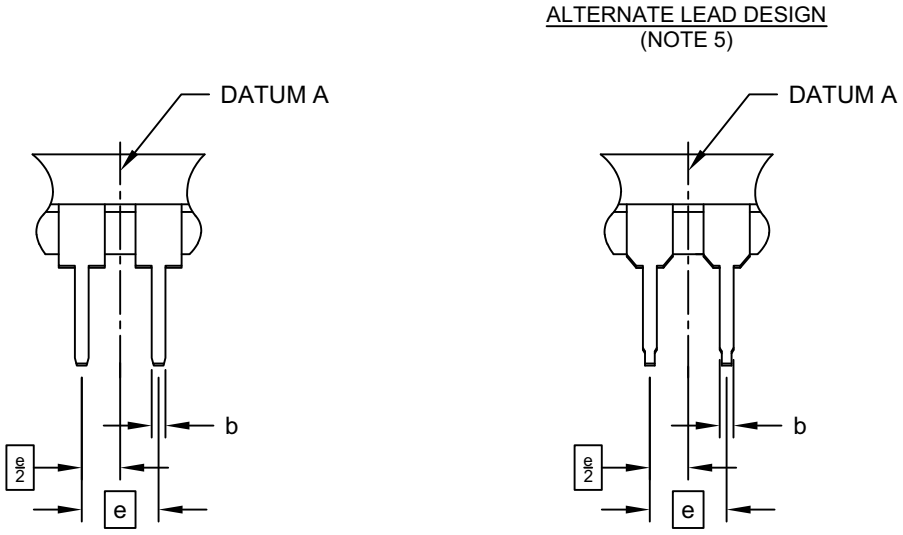
SIDE VIEW



END VIEW

8-Lead 0.300 in PDIP Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2022)

- Converted Micrel document MIC1232 to Microchip data sheet DS20006726A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	X	X	-XX
Device	Package	Junction Temp. Range	Media Type

Device:	MIC1232:	5V Voltage Supervisor with Manual Reset, Watchdog Timer and Dual Reset Outputs
Package:	M =	8-Lead SOIC
	N =	8-Lead PDIP
Junction Temperature Range:	Y =	–40°C to +185°C
Media Type:	<blank>=	95/Tube (M option only)
	<blank>=	50/Tube (N option only)
	TR =	2500/Reel (M option only)

Examples:

a) MIC1232MY: MIC1232, –40°C to +185°C Temp. Range, 8-Lead SOIC, 95/Tube

b) MIC1232NY: MIC1232, –40°C to +185°C Temp. Range, 8-Lead PDIP, 50/Tube

c) MIC1232MY-TR: MIC1232, –40°C to +185°C Temp. Range, 8-Lead SOIC, 2500/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

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