RELIABILITY REPORT

FOR

MAX3668EHJ

PLASTIC ENCAPSULATED DEVICES

April 21, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3668 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3668 is a complete, +3.3V laser driver with automatic power control (APC) circuitry for SDH/SONET applications up to 622Mbps. It accepts differential PECL inputs, provides bias and modulation currents, and operates over a temperature range from -40°C to +85°C.

An APC feedback loop is incorporated to maintain a constant average optical power over temperature and lifetime. The wide modulation current range from 5mA to 75mA and bias current of 1mA to 80mA are easy to program, making this product ideal for use in various SDH/SONET applications.

The MAX3668 also provides enable control and a failure-monitor output to indicate when the APC loop is unable to maintain the average optical power. The MAX3668 is available in a 5mm 32-pin TQFP package as well as in dice.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{CC}	-0.5V to +7.0V
Current into BIAS	-20mA to +150mA
Current into OUT+, OUT-	-20mA to +100mA
Current into MD	-5mA to +5mA
Voltage at DATA+,DATA-,CLK+,CLK-,ENABLE, /FAIL	-0.5V to (VCC +0.5V)
Voltage at CAPC, MODSET, BIASMAX, APCSET	-0.5V to +3.0V
Voltage at OUT+,OUT-	+1.5V to (VCC + 1.5V)
Voltage at BIAS	+1.0V to (VCC + 0.5V)
Storage Temp.	-65°C to +165°C
Operating Junction Temperature Range	-55°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +85°C)	
32-Pin TQFP	929mW
Derates above +85°C	
32-Pin TQFP	14.3mW/°C

II. Manufacturing Information

A. Description/Function:	+3.3V, 622Mbps SDH/SONET Laser Driver with APC
B. Process:	GST2 (High-Speed Double Poly-Silicon Bipolar Process)
C. Number of Device Transistors:	1525
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malyasia or Philippines
F. Date of Initial Production:	January, 1999

III. Packaging Information

A. Package Type:	**32-Pin TQFP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-7001-0333
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 3

IV. Die Information

A. Dimensions:	70 x 83 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.4 microns (as drawn)
F. Minimum Metal Spacing:	1.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 60 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 9.19 \times 10^{-9}$ $\lambda = 9.19$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-B3A**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF22-1 die type has been found to have all pins able to withstand a transient pulse of ±500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA.

Table 1
Reliability Evaluation Test Results

MAX3668EHJ

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		60	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

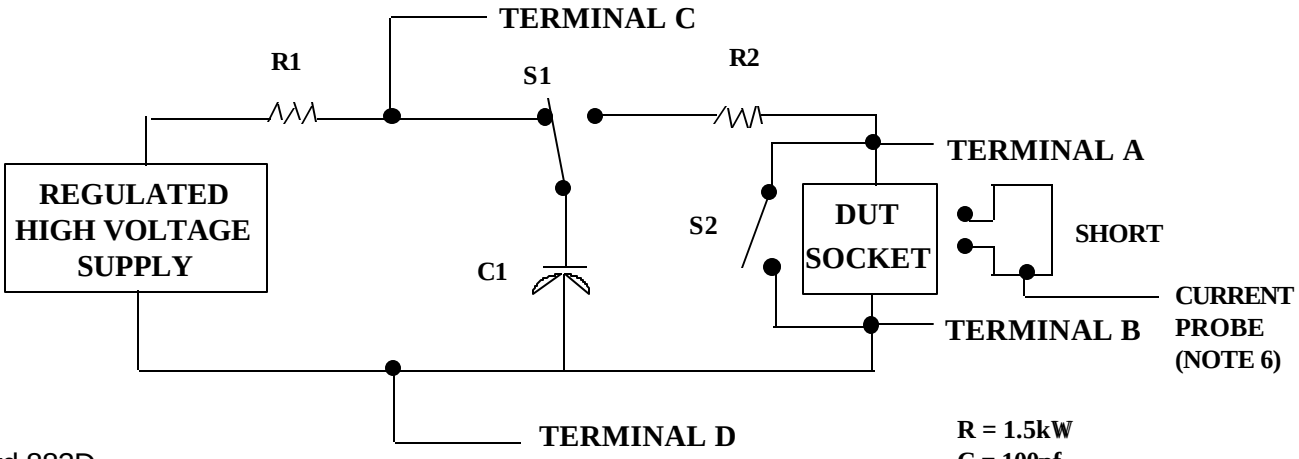
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

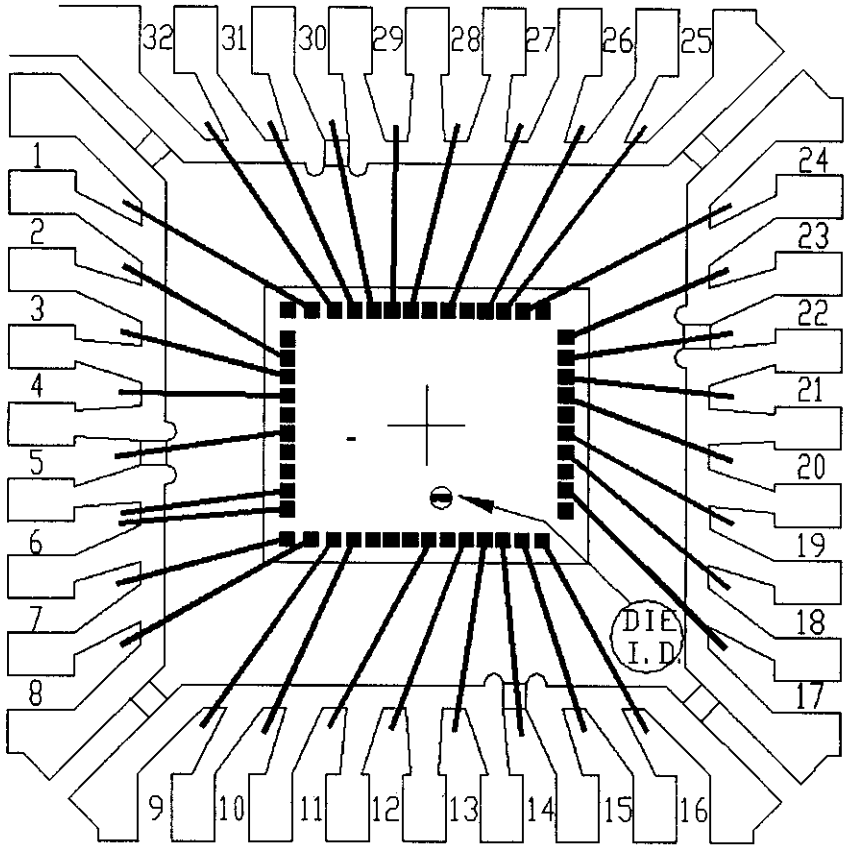
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: H32-2F		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 133×133	PKG. DESIGN			BUILDSHEET NUMBER: 05-7001-0333 / REV.: B