NP501-00029-0v01-E

FRAM
MB85RC1MT

The MB85RC1MT is a 1M bits FRAM LSI with serial interface (I^2C), using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
Since the FRAM is able to write with high-speed operation even though it is a nonvolatile memory, the MB85RC1MT is suitable for the log management and the storage of the resume data, etc.

PRELIMINARY

■ FEATURES

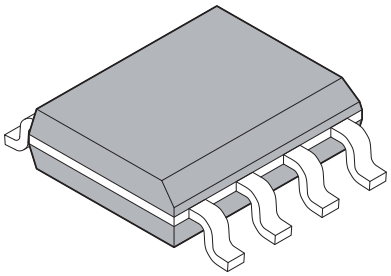
- **Bit configuration** : 131,072 words×8 bits
- **Two-wire serial interfac** : Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- **Operating frequency** : 3.4 MHz (Max @HIGH SPEED MODE)
  1 MHz (Max @FAST MODE PLUS)
- **Read/write endurance** : 10^{13} times / 16 bits
- **Data retention** : 10 years (+85 °C)
- **Operating power supply voltage** : 1.8V to 3.6V
- **Low power consumption** : Operating power supply current 1.2 mA (Max @3.4 MHz)
  Standby current 15 µA (Typ)
  Sleep current 4 µA (Typ)
- **Operation ambient temperature range** : -40 °C to +85 °C
- **Package** : 8-pin plastic SOP (FPT-8P-M02)
  RoHS compliant

■ ORDERING INFORMATION

Product name	Package	Shipping form	Minimum shipping quantity
MB85RC1MTPNF-G-JNE1	8-pin plastic SOP (FPT-8P-M02) 3.90mm×5.05mm, 1.27mm pitch	Tube	—*
MB85RC1MTPNF-G-JNERE1		Embossed Carrier tape	1500

*: Please contact our sales office about minimum shipping quantity.

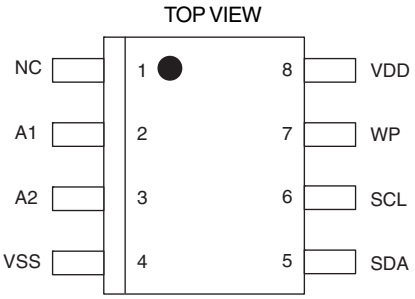
■ OUTLINE OF PACKAGE



8-pin plastic SOP
(FPT-8P-M02)

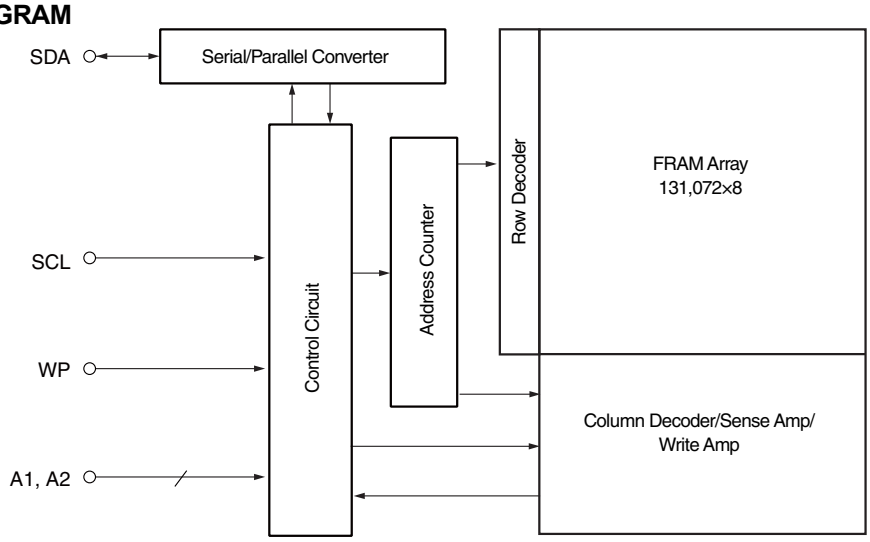
Copyright©2014 FUJITSU SEMICONDUCTOR LIMITED All rights reserved

■ PIN ASSIGNMENT



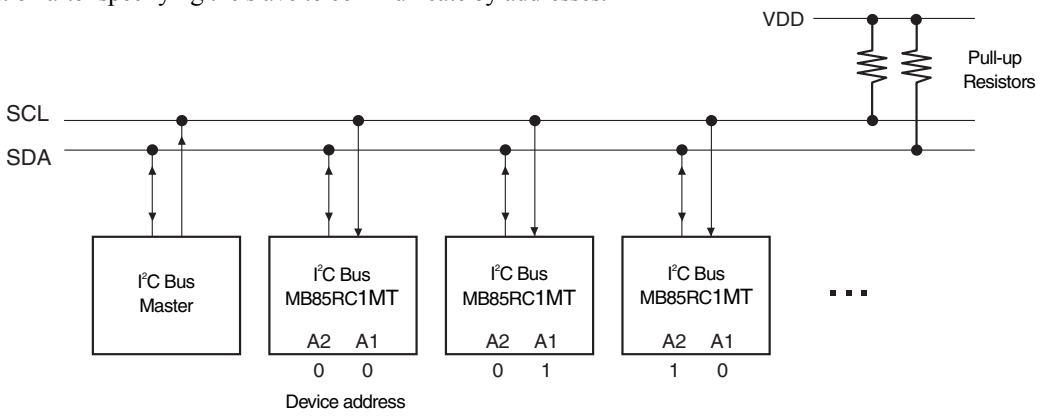
Pin Number	Pin Name	Functional Description
1	NC	No Connect pin
2,3	A1,A2	Device Address pins The MB85RC1MT can be connected to the same data bus up to 4 devices. Device addresses are used in order to identify each of these devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A1and A2 pins are internally pulled-down and recognized as the "L" level.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output timing serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When the Write Protect pin is the “H” level, the writing operation is disabled. When the Write Protect pin is the “L” level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The write protect pin is internally pulled down to VSS pin, and that is recognized as the “L” level (write enabled) when the pin is the open state.
8	VDD	Supply Voltage pin

■ BLOCK DIAGRAM



■ I²C

The MB85RC1MT has the two-wire serial interface; the I²C bus, and operates as a slave device. The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, the I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.



Copyright©2014 FUJITSU SEMICONDUCTOR LIMITED All rights reserved