

# MOSFET – N-Channel Shielded Gate POWERTRENCH®

150 V, 2.8 A, 128 mΩ

## FDT86244

### Description

This N-Channel MOSFET is produced using Fairchild onsemi advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for  $R_{DS(on)}$ , switching performance and ruggedness.

### Features

- Shielded Gate MOSFET Technology
- Max  $R_{DS(on)}$  = 128 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 2.8\text{ A}$
- Max  $R_{DS(on)}$  = 178 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 2.4\text{ A}$
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- These Devices are Pb-Free and are RoHS Compliant

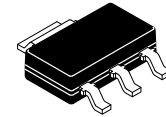
### Typical Applications

- Load Switch
- Primary Switch

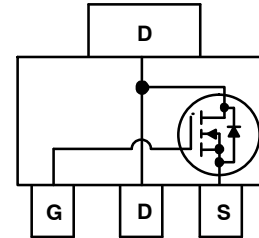
### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	20	V
$I_D$	Drain Current –Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	2.8	A
	–Pulsed	12	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	12	mJ
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.2	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

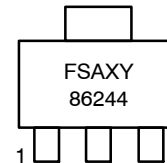
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



SOT-223  
CASE 318H



### MARKING DIAGRAM



Z = Assembly Plan Code  
XY = Date Code (Year & week)  
86244 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
FDT86244	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

**THERMAL CHARACTERISTICS**

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{V}$	150	-	-	V
$\frac{\Delta BV_{DSS(th)}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	-	104	-	mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120 \text{V}, V_{GS} = 0 \text{V}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{V}, V_{DS} = 0 \text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	-	-10	-	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{V}, I_D = 2.8 \text{A}$	-	106	128	m $\Omega$
		$V_{GS} = 6 \text{V}, I_D = 2.4 \text{A}$	-	127	178	
		$V_{GS} = 10 \text{V}, I_D = 2.8 \text{A}, T_J = 125^\circ\text{C}$	-	196	237	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{V}, I_D = 2.8 \text{A}$	-	12	-	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 75 \text{V}, V_{GS} = 0 \text{V}, f = 1 \text{MHz}$	-	295	395	pF
$C_{oss}$	Output Capacitance		-	33	45	pF
$C_{riss}$	Reverse Transfer Capacitance		-	2.4	5	pF
$R_g$	Gate Resistance		-	1	-	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75 \text{V}, I_D = 2.8 \text{A}, V_{GS} = 10 \text{V}, R_{GEN} = 6 \Omega$	-	5.3	11	ns
$t_r$	Rise Time		-	1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time		-	9.8	20	ns
$t_f$	Fall Time		-	2.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{V to } 10 \text{V}, V_{GS} = 0 \text{V to } 5 \text{V}$	-	4.9	7	nC
$Q_{g(TOT)}$	Total Gate Charge		-	2.8	4	nC
$Q_{gs}$	Total Gate Charge	$V_{DD} = 75 \text{V}, I_D = 2.8 \text{A}$	-	1.4	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	1.3	-	nC

# FDT86244

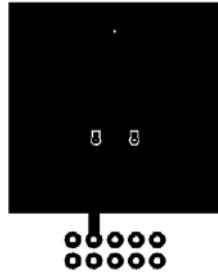
## ELECTRICAL CHARACTERISTICS (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Drain-Source Diode Characteristics</b>						
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2.8\text{ A}$ (Note 2)	-	0.82	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = 2.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	48	77	ns
$Q_{rr}$	Reverse Recovery Charge		-	44	70	nC

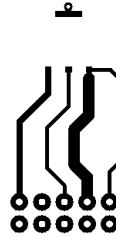
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 55 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 118 °C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test : Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%
- Starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 1\text{ mH}$ ,  $I_{AS} = 5\text{ A}$ ,  $V_{DD} = 135\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

TYPICAL CHARACTERISTICS  $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED

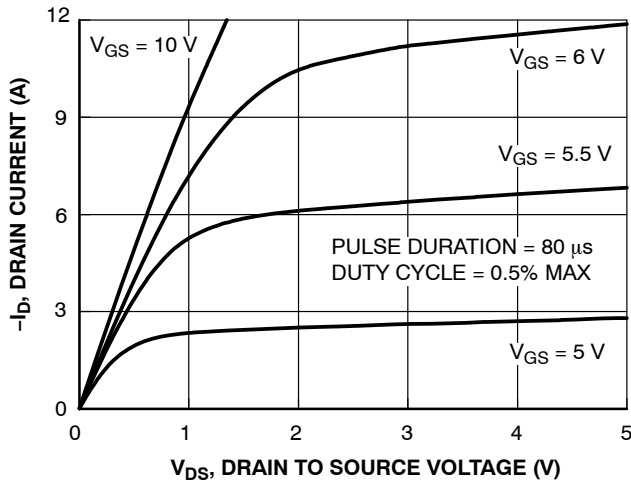


Figure 1. On-Region Characteristics

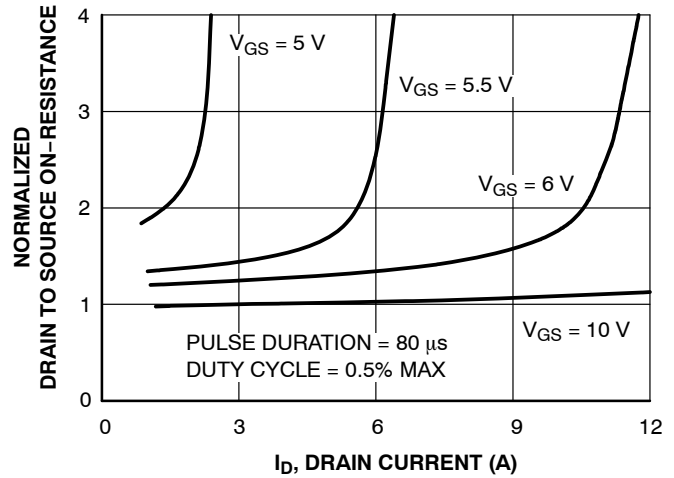


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

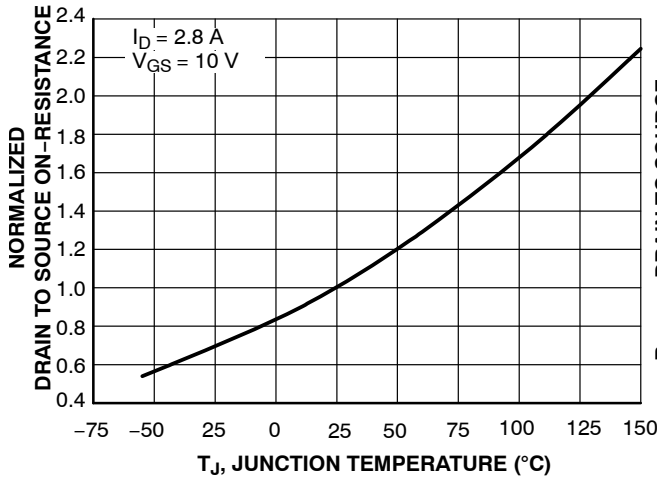


Figure 3. Normalized On Resistance vs Junction Temperature

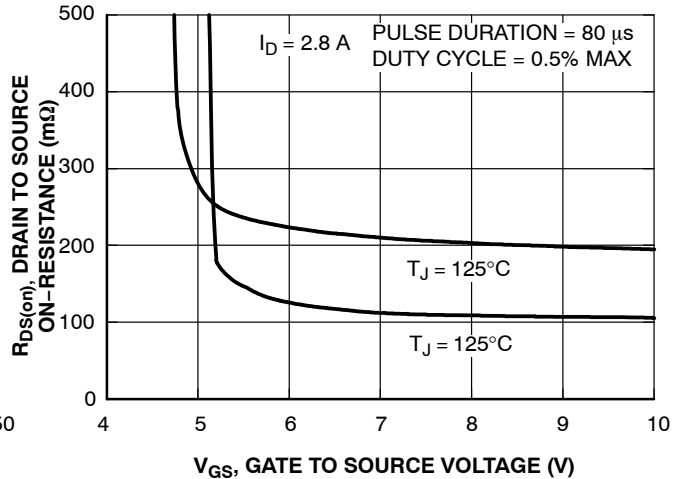


Figure 4. On-Resistance vs Gate to Source Voltage

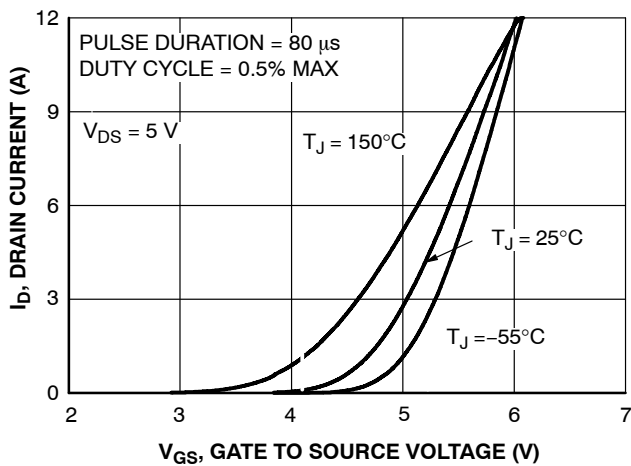


Figure 5. Transfer Characteristics

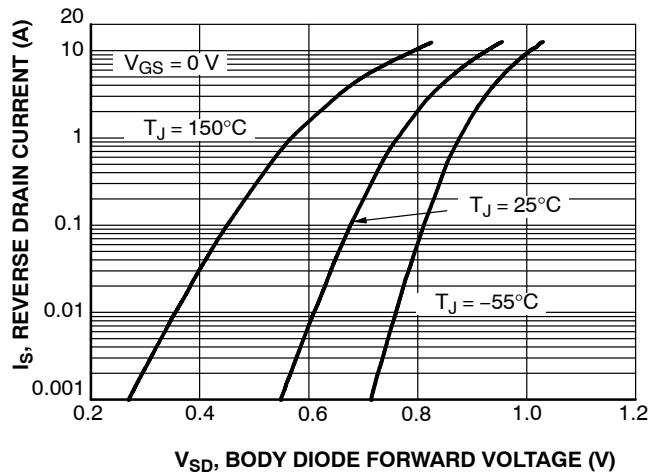


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (CONTINUED)  $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED

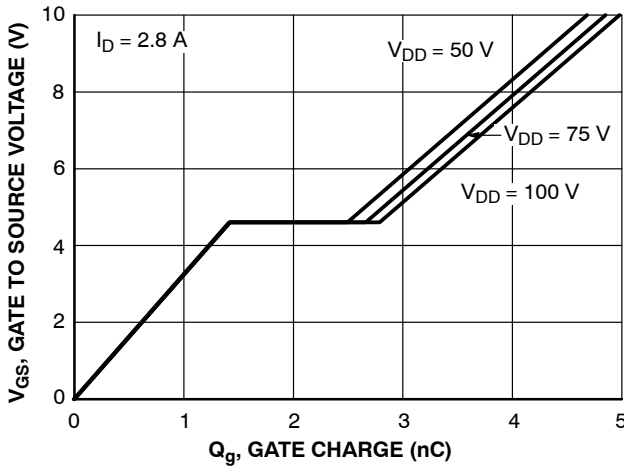


Figure 7. Gate Charge Characteristics

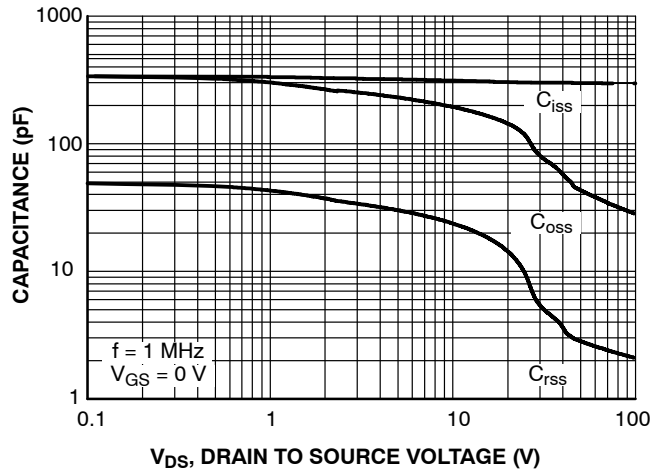


Figure 8. Capacitance vs Drain to Source Voltage

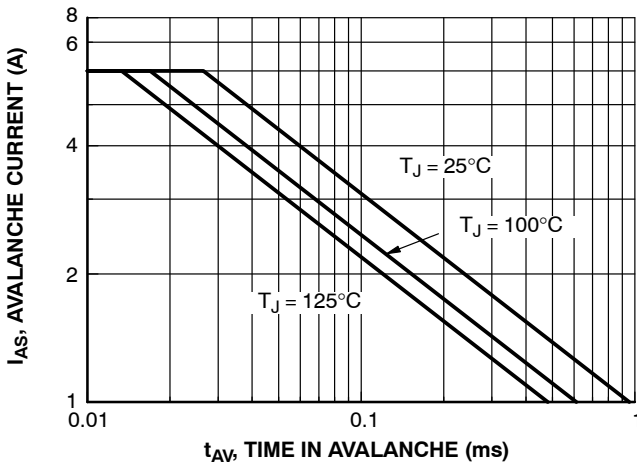


Figure 9. Unclamped Inductive Switching Capability

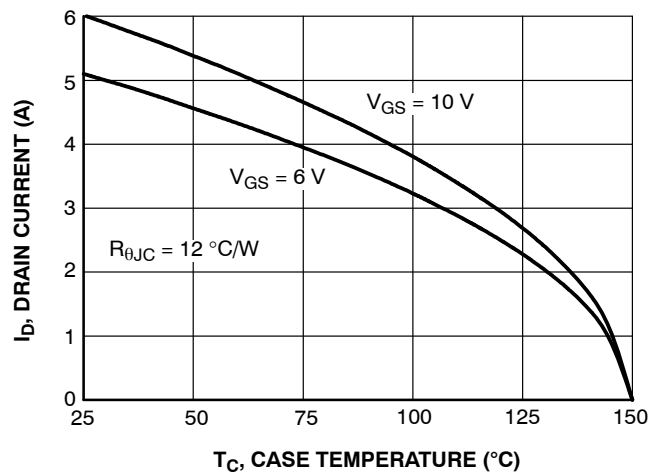


Figure 10. Maximum Continuous Drain Current vs Case Temperature

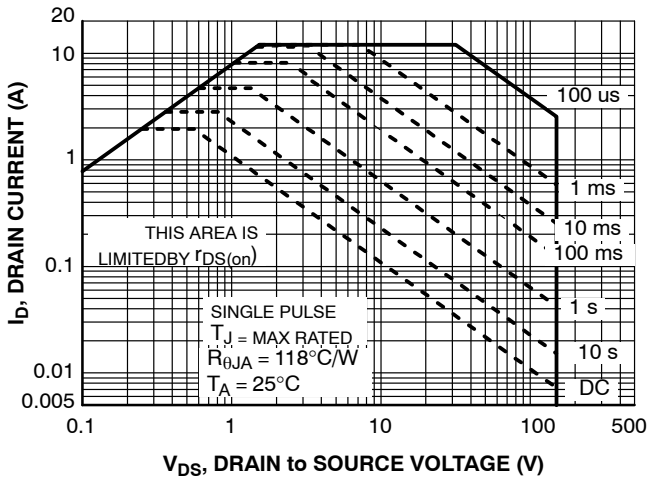


Figure 11. Forward Bias Safe Operating Area

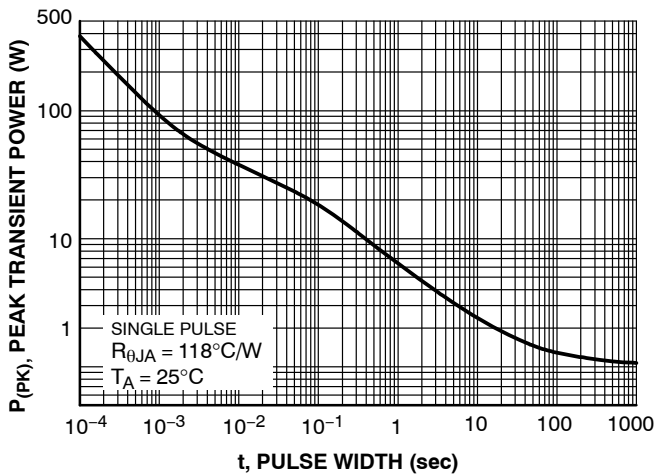


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)  $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED

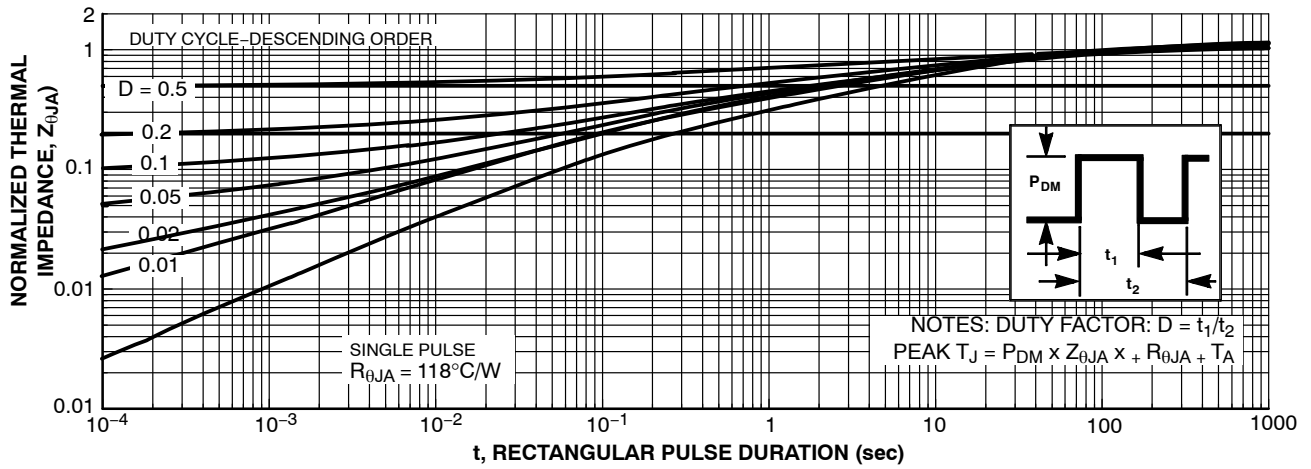
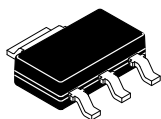


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

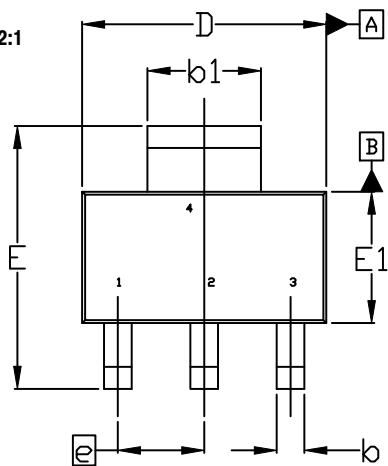
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**SOT-223**  
CASE 318H  
ISSUE B

DATE 13 MAY 2020

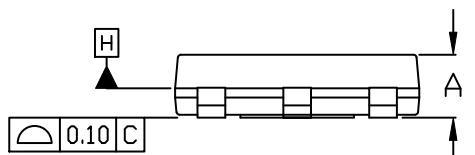
SCALE 2:1



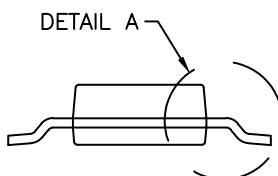
TOP VIEW

$\Phi 0.10 \text{ (M)}$  C A B

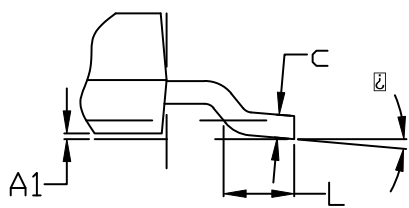
NOTE 7



SIDE VIEW



END VIEW

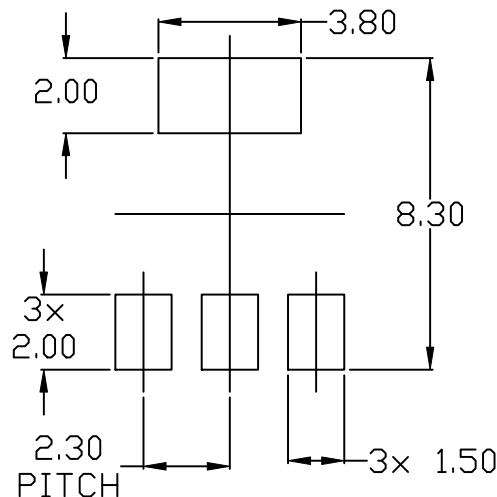


DETAIL A

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

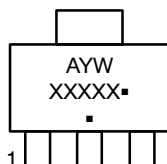
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
$\square$	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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