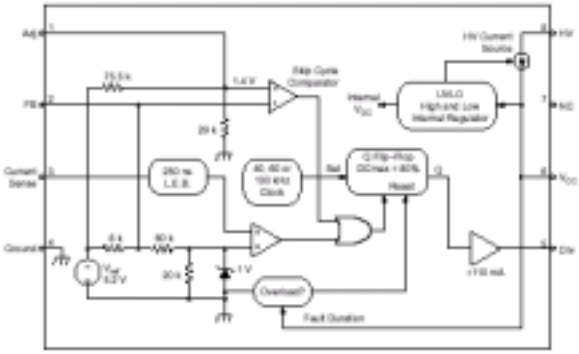
NCP1200PAK/D
Rev. 0, May-2001

NCP1200 Literature Pack

ON Semiconductor™

NCP1200

PWM Current Mode Controller



Description

- Self-supplied from the DC rail (up to 450V)
- Drives external MOSFET
- Low standby power
- Short circuit protected
- Meets next IEA recommendations: P_{IN} < 500mW
- Internally fixed frequency at 40kHz, 60kHz and 100kHz

Applications

- Off-line power supplies
- AC-DC adapters & battery chargers
- Auxiliary power supplies

Features

- Current mode control
- Self-supplied from the DC rail (lower cost)
- Built-in frequency jitter
- Peak current reduction at no load
- Low standby power <0.5mW
- Higher integration than UC384*x*
- Drives external MOSFET

Benefits

- Easier to stabilize and fast response
- Eliminates need for auxiliary winding
- Reduce EMI
- Reduces acoustic noise under open circuit conditions
- Meets European low power directives
- Low external parts count
- Offer increase flexibility of design to maximize thermal performance and scale power requirements

Ordering Information

Device	Package	Shipping
NCP1200P40	PDIP-8	50 per rail
NCP1200D40R2	SO-8	2500 per reel
NCP1200P60	PDIP-8	50 per rail
NCP1200D60R2	SO-8	2500 per reel
NCP1200P100	PDIP-8	50 per rail
NCP1200D100R2	SO-8	2500 per reel

Additional Information

- Visit us at **onsemi.com/ncp1200**
  - Datasheet
  - Case outline
  - App note AND8023/D
- Transient and averaged SPICE models available

For details, contact your sales representative, local distributor, or visit

www.onsemi.com

ON Semiconductor

NCP1200

PWM Current-Mode Controller for Low-Power Universal Off-Line Supplies

Housed in SO–8 or DIP–8 package, the NCP1200 represents a major leap toward ultra–compact Switch–Mode Power Supplies. Thanks to a novel concept, the circuit allows the implementation of a complete off–line battery charger or a standby SMPS with few external components. Furthermore, an integrated output short–circuit protection lets the designer build an extremely low–cost AC/DC wall adapter associated with a simplified feedback scheme.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz, the controller drives low gate–charge switching devices like an IGBT or a MOSFET thus requiring a very small operating power. Thanks to current–mode control, the NCP1200 drastically simplifies the design of reliable and cheap off–line converters with extremely low acoustic generation and **inherent pulse–by–pulse control**.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the skip cycle mode and provides excellent efficiency at light loads. Because this occurs at low peak current, no acoustic noise takes place.

Finally, the IC is self–supplied from the DC rail, eliminating the need of an auxiliary winding. This feature ensures operation in presence of low output voltage or shorts.

High Efficiency

Features

Allows Smaller, Lower Cost Transformer

- **No Auxiliary Winding Operation**
- Internal Output Short–Circuit Protection

Meet Next IEA Requirements

- **Extremely Low No–Load Standby Power**

Stable and Fast Response

- **Current–Mode with Skip–Cycle Capability**
- Internal Leading Edge Blanking
- 110 mA Peak Current Source/Sink Capability
- Internally Fixed Frequency at 40 kHz, 60 kHz and 100 kHz
- Direct Optocoupler Connection

For Lower EMI

- **Built–in Frequency Jittering**
- **SPICE Models Available** for TRANsient and AC Analysis
- Internal Temperature Shutdown

Fast, Easy Design

Typical Applications

- AC/DC Adapters
- Off–line Battery Chargers
- Auxiliary/Ancillary Power Supplies (USB, Appliances, TVs, etc.)

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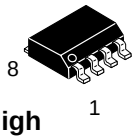
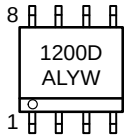
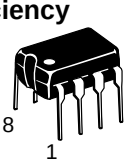
MARKING DIAGRAMS

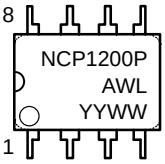


SO–8
D SUFFIX
CASE 751



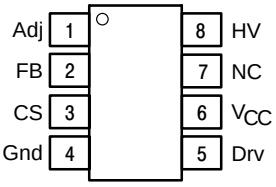


DIP–8
P SUFFIX
CASE 626



A = Assembly Location
L = Wafer Lot
Y, YY = Year
W, WW = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on the complete version of this data sheet.

March, 2001 – Rev. 4

NCP1200

PWM Current-Mode Controller for Low-Power Universal Off-Line Supplies

Housed in SO–8 or DIP–8 package, the NCP1200 represents a major leap toward ultra–compact Switch–Mode Power Supplies. Thanks to a novel concept, the circuit allows the implementation of a complete offline battery charger or a standby SMPS with few external components. Furthermore, an integrated output short–circuit protection lets the designer build an extremely low–cost AC/DC wall adapter associated with a simplified feedback scheme.

With an internal structure operating at a fixed 40 kHz, 60 kHz or 100 kHz, the controller drives low gate–charge switching devices like an IGBT or a MOSFET thus requiring a very small operating power. Thanks to current–mode control, the NCP1200 drastically simplifies the design of reliable and cheap offline converters with extremely low acoustic generation and inherent pulse–by–pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the skip cycle mode and provides excellent efficiency at light loads. Because this occurs at low peak current, no acoustic noise takes place.

Finally, the IC is self–supplied from the DC rail, eliminating the need of an auxiliary winding. This feature ensures operation in presence of low output voltage or shorts.

Features

- No Auxiliary Winding Operation
- Internal Output Short–Circuit Protection
- Extremely Low No–Load Standby Power
- Current–Mode with Skip–Cycle Capability
- Internal Leading Edge Blanking
- 110 mA Peak Current Source/Sink Capability
- Internally Fixed Frequency at 40 kHz, 60 kHz and 100 kHz
- Direct Optocoupler Connection
- Built–in Frequency Jittering for Lower EMI
- SPICE Models Available for TRANsient and AC Analysis
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- AC/DC Adapters
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- Auxiliary/Ancillary Power Supplies (USB, Appliances, TVs, etc.)

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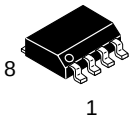
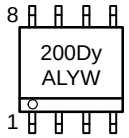
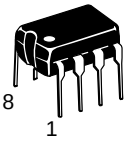
MARKING DIAGRAMS

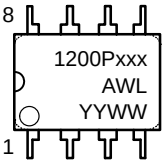


SO–8
D SUFFIX
CASE 751



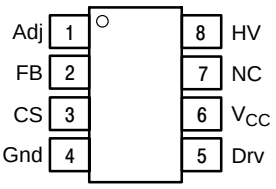


DIP–8
P SUFFIX
CASE 626



xxx = Device Code: 40, 60 or 100
y = Device Code:
4 for 40
6 for 60
1 for 100
A = Assembly Location
L = Wafer Lot
Y, YY = Year
W, WW = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

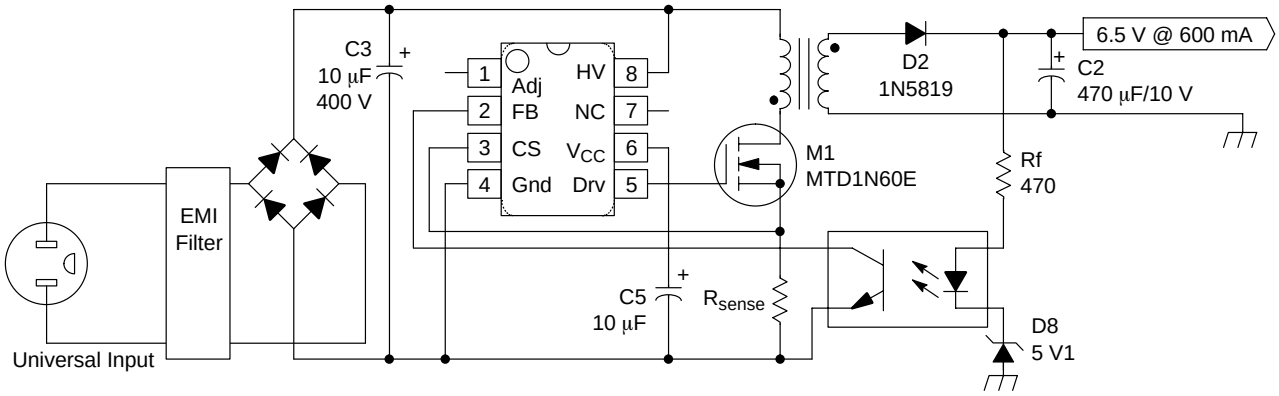


Figure 1. Typical Application

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	Adj	Adjust the skipping peak current	This pin lets you adjust the level at which the cycle skipping process takes place
2	FB	Sets the peak current setpoint	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand
3	CS	Current sense input	This pin senses the primary current and routes it to the internal comparator via an L.E.B
4	Gnd	The IC ground	
5	Drv	Driving pulses	The driver's output to an external MOSFET
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 10 μF
7	NC	No Connection	This un–connected pin ensures adequate creepage distance
8	HV	Generates the V_{CC} from the line	Connected to the high–voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor

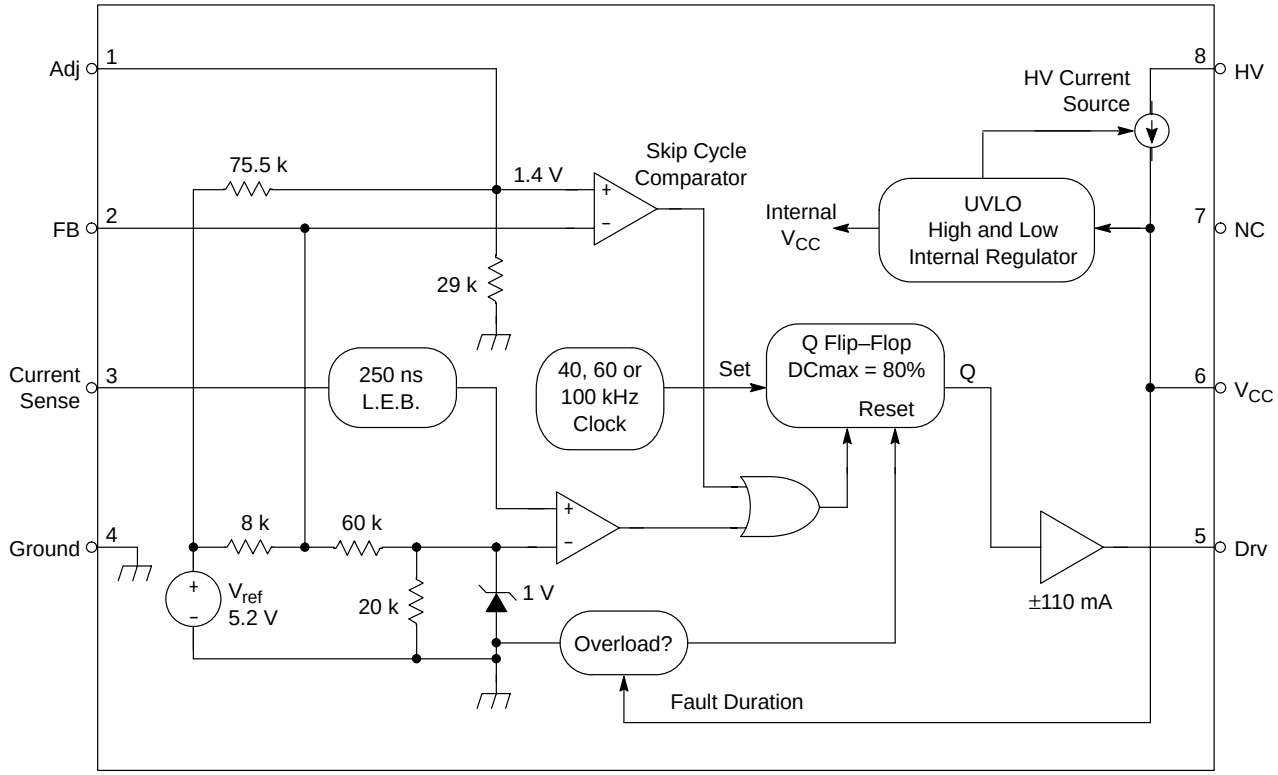


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC}	16	V
Thermal Resistance Junction–to–Air, PDIP8 version Thermal Resistance Junction–to–Air, SOIC version	$R_{\theta JA}$ $R_{\theta JA}$	100 178	°C/W
Maximum Junction Temperature Typical Temperature Shutdown	T_{Jmax} –	150 140	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C
ESD Capability, HBM model (All pins except V_{CC} and HV)	–	2.0	kV
ESD Capability, Machine model	–	200	V
Maximum Voltage on pin 8 (HV), pin 6 (V_{CC}) grounded	–	450	V
Maximum Voltage on pin 8 (HV), pin 6 (V_{CC}) decoupled to ground with 10 μF	–	500	V

ELECTRICAL CHARACTERISTICS (For typical values T_J = +25°C, for min/max values T_J = –25°C to +125°C, Max T_J = 150°C, V_{CC}= 11 V unless otherwise noted)

Rating	Pin	Symbol	Min	Typ	Max	Unit
DYNAMIC SELF–SUPPLY (All frequency versions, otherwise noted)						
V_{CC} increasing level at which the current source turns–off	6	V_{CCOFF}	10.3	11.4	12.5	V
V_{CC} decreasing level at which the current source turns–on	6	V_{CCON}	8.8	9.8	11	V
V_{CC} decreasing level at which the latch–off phase ends	6	$V_{CClatch}$	–	6.3	–	V
Internal IC Consumption, no output load on pin 6	6	I_{CC1}	–	710	880 Note 1	μA
Internal IC Consumption, 1 nF output load on pin 6, F_{SW} = 40 kHz	6	I_{CC2}	–	1.2	1.4 Note 2	mA
Internal IC Consumption, 1 nF output load on pin 6, F_{SW} = 60 kHz	6	I_{CC2}	–	1.4	1.6 Note 2	mA
Internal IC Consumption, 1 nF output load on pin 6, F_{SW} = 100 kHz	6	I_{CC2}	–	1.9	2.2 Note 2	mA
Internal IC Consumption, latch–off phase	6	I_{CC3}	–	350	–	μA
INTERNAL CURRENT SOURCE						
High–voltage current source, V_{CC} = 10 V	8	I_{C1}	2.8	4.0	–	mA
High–voltage current source, V_{CC} = 0	8	I_{C2}	–	4.9	–	mA
DRIVE OUTPUT						
Output voltage rise–time @ CL = 1 nF, 10–90% of output signal	5	T_r	–	67	–	ns
Output voltage fall–time @ CL = 1 nF, 10–90% of output signal	5	T_f	–	28	–	ns
Source resistance (drive = 0, Vgate = V_{CCHMAX} – 1 V)	5	R_{OH}	27	40	61	Ω
Sink resistance (drive = 11 V, Vgate = 1 V)	5	R_{OL}	5	12	20	Ω
CURRENT COMPARATOR (Pin 5 un–loaded)						
Input Bias Current @ 1 V input level on pin 3	3	I_{IB}	–	0.02	–	μA
Maximum internal current setpoint	3	I_{Limit}	0.8	0.9	1.0	V
Default internal current setpoint for skip cycle operation	3	I_{Lskip}	–	350	–	mV
Propagation delay from current detection to gate OFF state	3	T_{DEL}	–	100	160	ns
Leading Edge Blanking Duration	3	T_{LEB}	–	230	–	ns
INTERNAL OSCILLATOR (V_{CC} = 11 V, pin 5 loaded by 1 kΩ)						
Oscillation frequency, 40 kHz version	–	f_{OSC}	36	42	48	kHz
Oscillation frequency, 60 kHz version	–	f_{OSC}	52	61	70	kHz
Oscillation frequency, 100 kHz version	–	f_{OSC}	86	103	116	kHz
Built–in frequency jittering, F_{SW} = 40 kHz	–	f_{jitter}	–	300	–	Hz/V
Built–in frequency jittering, F_{SW} = 60 kHz	–	f_{jitter}	–	450	–	Hz/V
Built–in frequency jittering, F_{SW} = 100 kHz	–	f_{jitter}	–	620	–	Hz/V
Maximum duty–cycle	–	Dmax	74	80	87	%
FEEDBACK SECTION (Vcc = 11 V, pin 5 loaded by 1 kΩ)						
Internal pull–up resistor	2	Rup	–	8.0	–	kΩ
Pin 3 to current setpoint division ratio	–	Iratio	–	4.0	–	–
SKIP CYCLE GENERATION						
Default skip mode level	1	Vskip	1.1	1.4	1.6	V
Pin 1 internal output impedance	1	Zout	–	25	–	kΩ

1. Max value @ T_J = –25°C.
2. Max value @ T_J = 25°C, please see characterization curves.

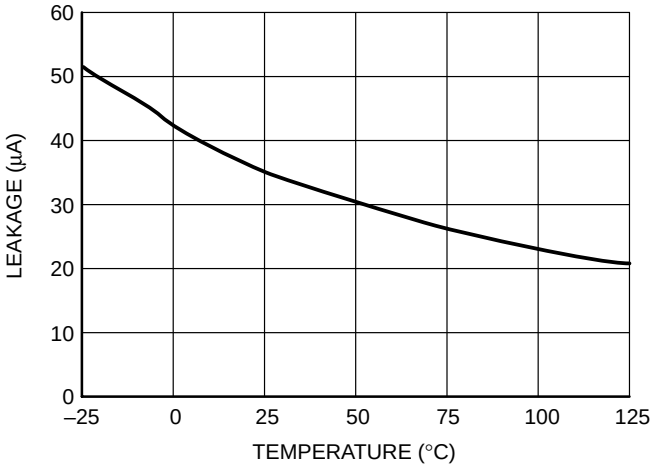


Figure 3. HV Pin Leakage Current vs. Temperature

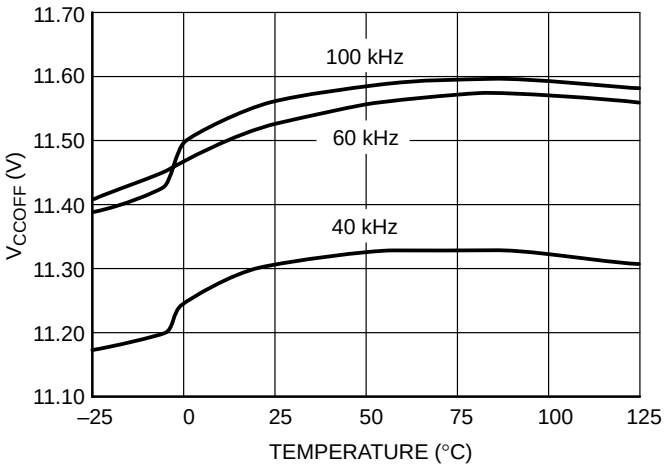


Figure 4. V_{CC} OFF vs. Temperature

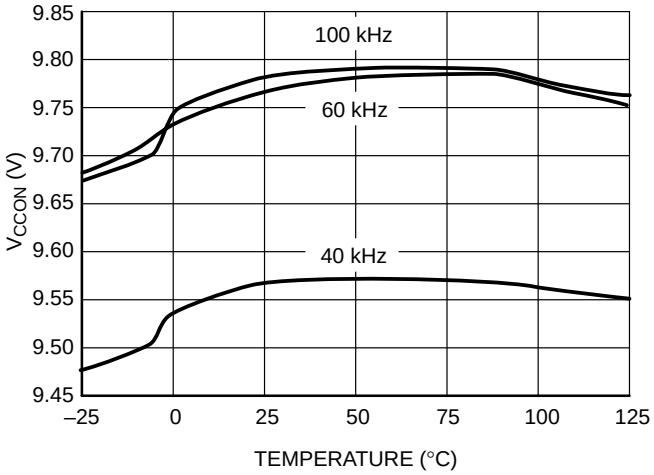


Figure 5. V_{CC} ON vs. Temperature

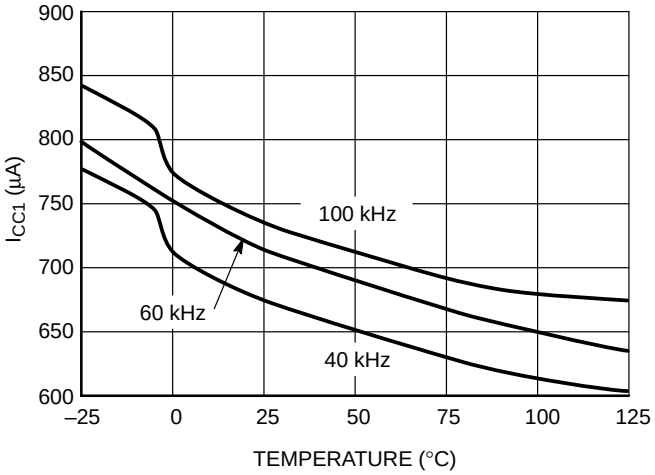


Figure 6. I_{CC1} vs. Temperature

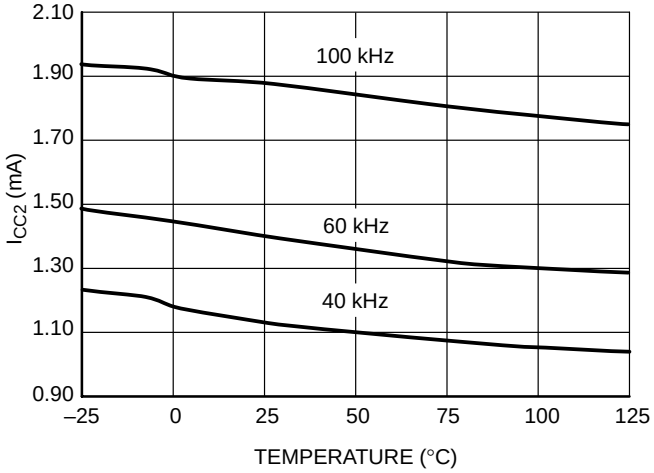


Figure 7. I_{CC2} vs. Temperature

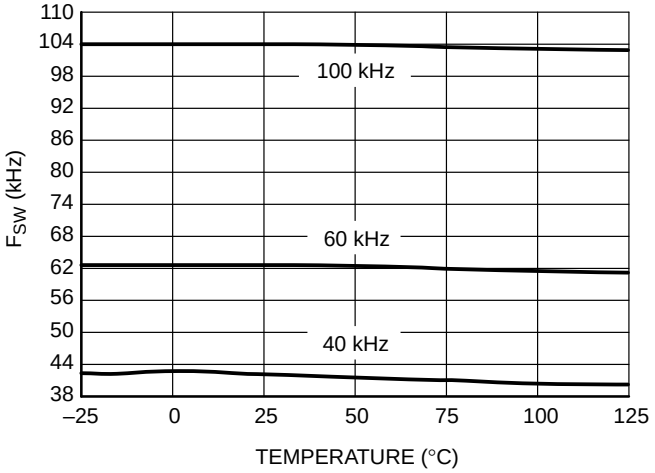


Figure 8. Switching Frequency vs. T_J

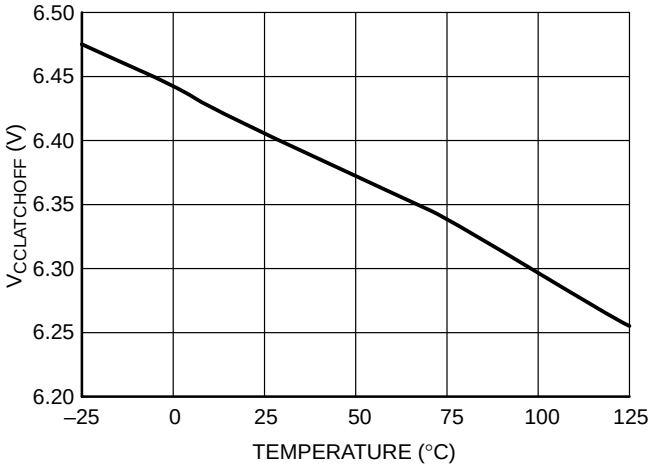


Figure 9. V_{CC} Latchoff vs. Temperature

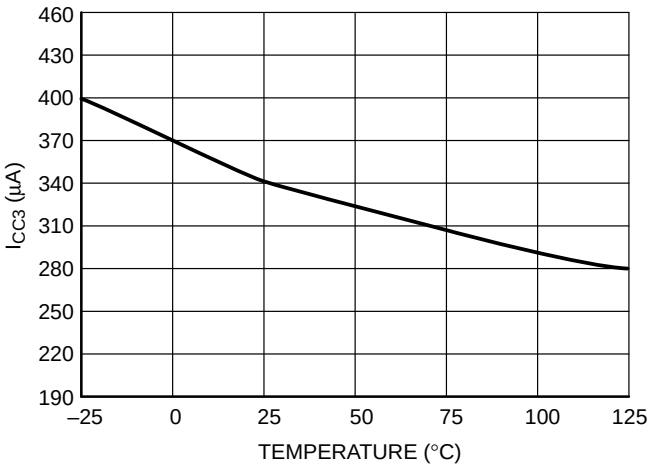


Figure 10. I_{CC3} vs. Temperature

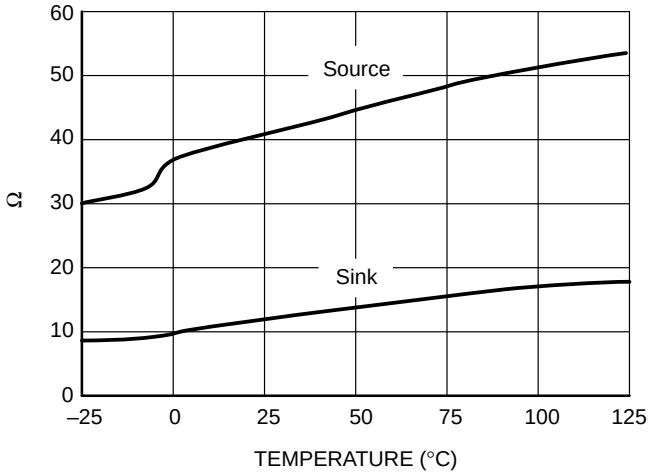


Figure 11. DRV Source/Sink Resistances

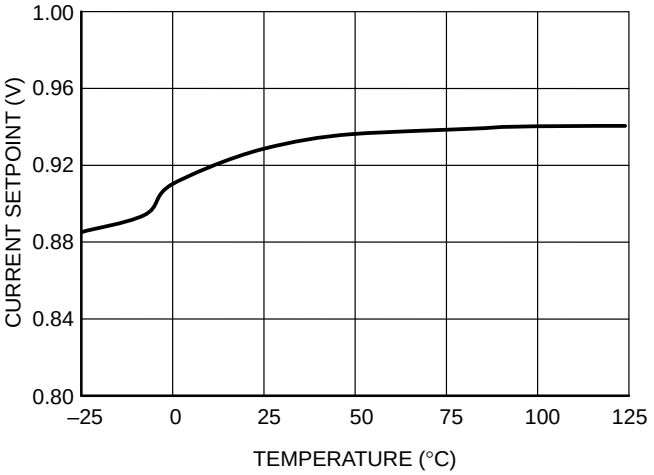


Figure 12. Current Sense Limit vs. Temperature

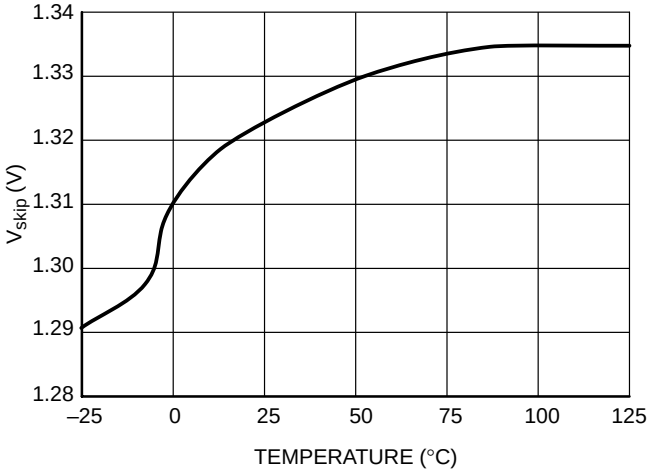


Figure 13. V_{skip} vs. Temperature

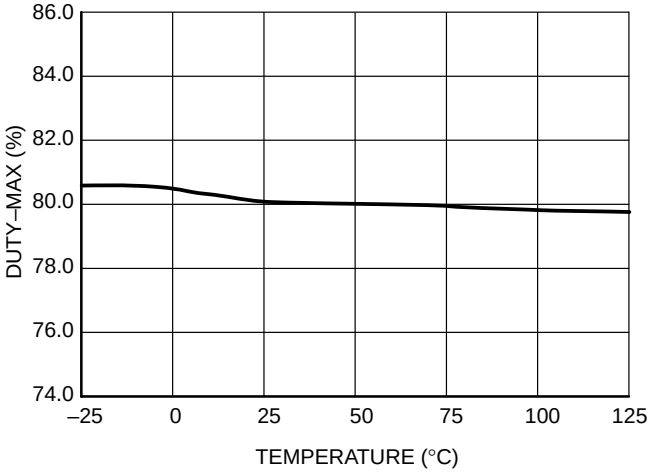


Figure 14. Max Duty–Cycle vs. Temperature

APPLICATIONS INFORMATION

INTRODUCTION

The NCP1200 implements a standard current mode architecture where the switch–off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part–count is the key parameter, particularly in low–cost AC/DC adapters, auxiliary supplies etc. Thanks to its high–performance High–Voltage technology, the NCP1200 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low–pass filter and self–supply. This later point emphasizes the fact that ON Semiconductor's NCP1200 does NOT need an auxiliary winding to operate: the product is naturally supplied from the high–voltage rail and delivers a V_{CC} to the IC. This system is called the Dynamic Self–Supply (DSS).

Dynamic Self–Supply

The DSS principle is based on the charge/discharge of the V_{CC} bulk capacitor from a low level up to a higher level. We can easily describe the current source operation with a bunch of simple logical equations:

POWER–ON: IF $V_{CC} < V_{CCOFF}$ THEN Current Source is ON, no output pulses

IF V_{CC} decreasing > V_{CCON} THEN Current Source is OFF, output is pulsing

IF V_{CC} increasing < V_{CCOFF} THEN Current Source is ON, output is pulsing

Typical values are: V_{CCOFF} = 11.4 V, V_{CCON} = 9.8 V

To better understand the operational principle, Figure 15's sketch offers the necessary light:

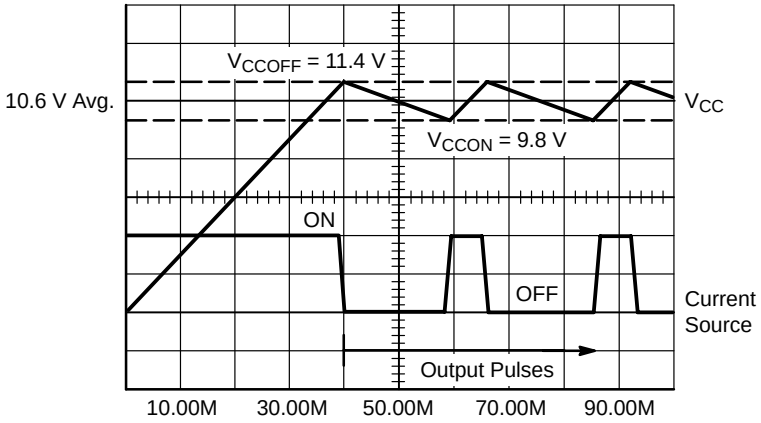


Figure 15. The Charge/Discharge Cycle Over a 10 μF V_{CC} Capacitor

The DSS behavior actually depends on the internal IC consumption and the MOSFET's gate charge, Qg. If we select a MOSFET like the MTD1N60E, Qg equals 11 nC (max). With a maximum switching frequency of 48 kHz (for the P40 version), the average power necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is:

$$Fsw \cdot Qg \cdot V_{CC} \qquad \text{with}$$

Fsw = maximum switching frequency

Qg = MOSFET's gate charge

$V_{CC} = V_{GS}$ level applied to the gate

To obtain the final driver contribution to the IC consumption, simply divide this result by V_{CC}: Idriver = $Fsw \cdot Qg$ = 530 μA. The total standby power consumption at no–load will therefore heavily rely on the internal IC consumption plus the above driving current (altered by the driver's efficiency). Suppose that the IC is supplied from a 400 V DC line. To fully supply the integrated circuit, let's imagine the 4 mA source is ON during 8 ms and OFF during 50 ms. The IC power contribution is therefore: 400 V . 4 mA . 0.16 = 256 mW. If for design reasons this contribution is still too high, several solutions exist to diminish it:

1. Use a MOSFET with lower gate charge Qg
2. Connect pin through a diode (1N4007 typically) to one of the mains input. The average value on pin 8 becomes $\frac{2 * V_{mains\ PEAK}}{\pi}$. Our power contribution example drops to: 160 mW.

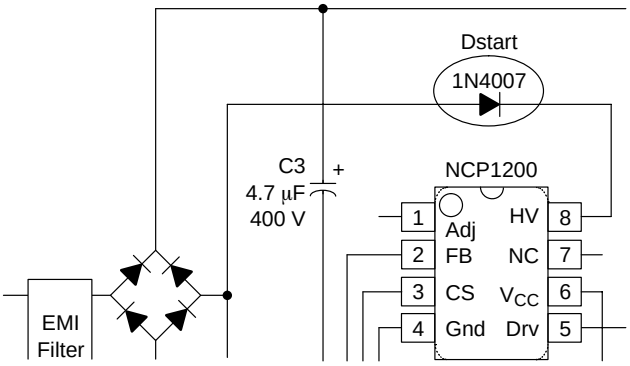


Figure 16. A simple diode naturally reduces the average voltage on pin 8

3. Permanently force the V_{CC} level above V_{CCH} with an auxiliary winding. It will automatically disconnect the internal start–up source and the IC will be fully self–supplied from this winding. Again, the total power drawn from the mains will significantly decrease. Make sure the auxiliary voltage never exceeds the 16 V limit.

Skipping Cycle Mode

The NCP1200 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so–called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 18). Suppose we have the following component values:

Lp, primary inductance = 1 mH

F_{SW}, switching frequency = 48 kHz

Ip skip = 300 mA (or 350 mV / Rsense)

The theoretical power transfer is therefore:

$$\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw = 2.2\ W$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 2.2 . 0.1 = 220 mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

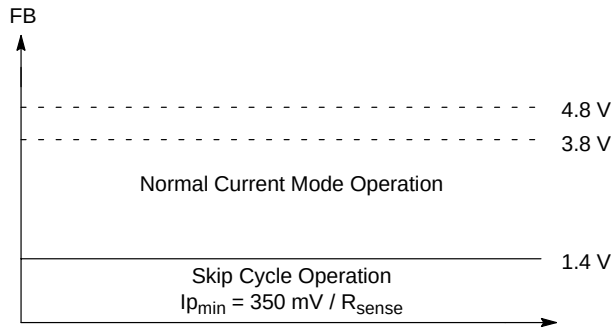


Figure 17. Feedback Voltage Variations

When FB is above the skip cycle threshold (1.4 V by default), the peak current cannot exceed 1 V/Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1 / 4 (Figure 19). The user still has the flexibility to alter this 1.4 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level.

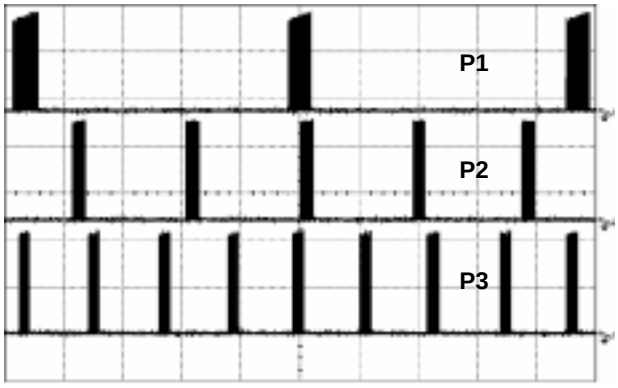


Figure 18. Output pulses at various power levels (X = 5 μs/div) P1<P2<P3

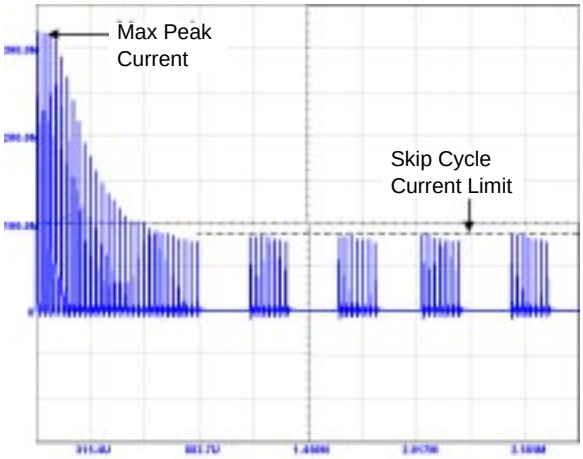


Figure 19. The skip cycle takes place at low peak currents which guarantees noise free operation

Power Dissipation

The NCP1200 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the NCP1200 current consumption. The total power dissipation can be evaluated using: $(V_{HVDC} - 11\ V) \cdot ICC2$. If we operate the device on a 250 VAC rail, the maximum rectified voltage can go up to 350 VDC. As a result, the worse case dissipation occurs on the 100 kHz version which will dissipate 340 **.** 1.8 mA@Tj = –25°C = 612 mW (however this 1.8 mA number will drop at higher operating temperatures). A DIP8 package offers a junction–to–ambient thermal resistance of $R_{\theta J-A}$ 100°C/W. The maximum power dissipation can thus be computed knowing the maximum operating ambient temperature (e.g. 70°C) together with the maximum allowable junction temperature (125°C): $Pmax = \frac{T_{Jmax} - T_{Amax}}{R_{R\theta J-A}}$ = 550 mW. As we can see, we do not reach the worse consumption budget imposed by the 100 kHz version. Two solutions exist to cure this trouble. The first one consists in adding some copper area around the NCP1200 DIP8 footprint. By adding a min–pad area of 80 mm^2 of 35 μ copper (1 oz.) $R_{\theta J-A}$ drops to about 75°C/W which allows the use of the 100 kHz version. The other solutions are:

1. Add a series diode with pin 8 (as suggested in the above lines) to drop the maximum input voltage down to 222 V ((2 × 350)/pi) and thus dissipate less than 400 mW
2. Implement a self–supply through an auxiliary winding to permanently disconnect the self–supply.

SO–8 package offers a worse $R_{\theta J-A}$ compared to that of the DIP8 package: 178°C/W. Again, adding some copper area around the PCB footprint will help decrease this number: 12 mm x 12 mm to drop $R_{\theta J-A}$ down to 100°C/W with 35 μ copper thickness (1 oz.) or 6.5 mm x 6.5 mm with 70 μ copper thickness (2 oz.). As one can see, we do not recommend using the SO–8 package for the 100 kHz version with DSS active as the IC may not be able to sustain the power (except if you have the adequate place on your PCB). However, using the solution of the series diode or the self–supply through the auxiliary winding does not cause any problem with this frequency version. These options are thoroughly described in the AND8023/D.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short–circuit protection. A short–circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the FB pin level is pulled up to 4.1 V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken optocoupler. To account for this situation, the NCP1200 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty–cycle. The system recovers when the fault condition disappears.

During the start–up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time–out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the V_{CCOFF} level (typically 11.4 V) the device internally watches for an overload current situation. If this condition is still present when V_{CCON} is reached, the controller stops the driving pulses, prevents the self–supply current source to restart and puts all the circuitry in standby, consuming as little as 350 μA typical (I_{CC3} parameter). As a result, the V_{CC} level slowly discharges toward 0. When this level crosses 6.3 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 11.4 V and again delivers output pulses at the $UVLO_H$ crossing point. If the fault condition has been removed before $UVLO_L$ approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 20 shows the evolution of the signals in presence of a fault.

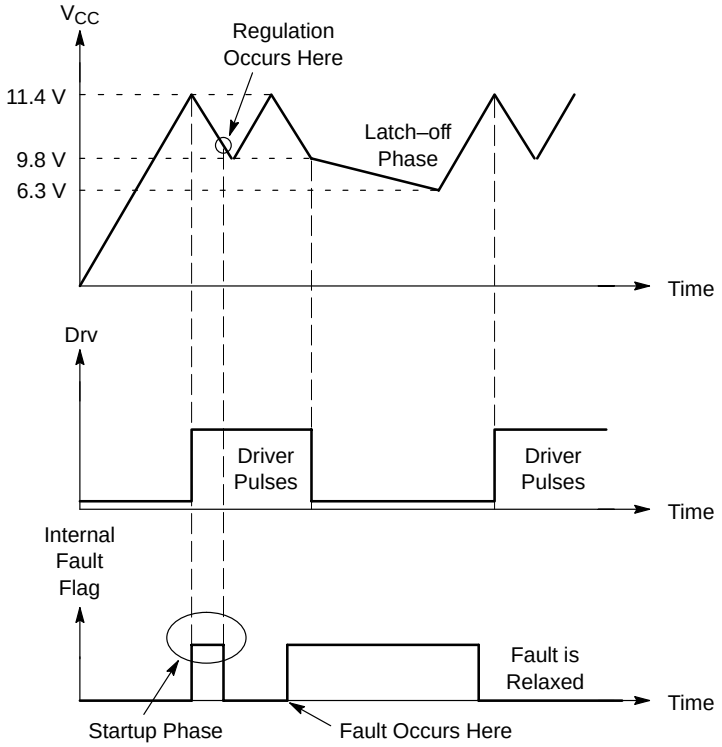


Figure 20. If the fault is relaxed during the V_{CC} natural fall down sequence, the IC automatically resumes. If the fault persists when V_{CC} reached $UVLO_L$, then the controller cuts everything off until recovery.

Calculating the V_{CC} Capacitor

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 11.4 V to 9.8 V? The required time depends on the start–up sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 11.4 V to 9.8 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.5 mA, we can calculate the required capacitor using the following formula: $\Delta t = \frac{\Delta V \cdot C}{i}$, with ΔV = 2V. Then for a wanted Δt of 10 ms, C equals 8 μF or 10 μF for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 350 μA typical. This appends at V_{CC} = 9.8 V and it remains stuck until V_{CC} reaches 6.5 V: we are in latch–off phase. Again, using the calculated 10 μF and 350 μA current consumption, this latch–off phase lasts: 109 ms.

A Typical Application

Figure 21 depicts a low–cost 3.5 W AC/DC 6.5 V wall adapter. This is a typical application where the wall–pack must deliver a raw DC level to a given internally regulated apparatus: toys, calculators, CD–players etc. Thanks to the inherent short–circuit protection of the NCP1200, you only need a bunch of components around the IC, keeping the final cost at an extremely low level. The transformer is available from different suppliers as detailed on the following page.

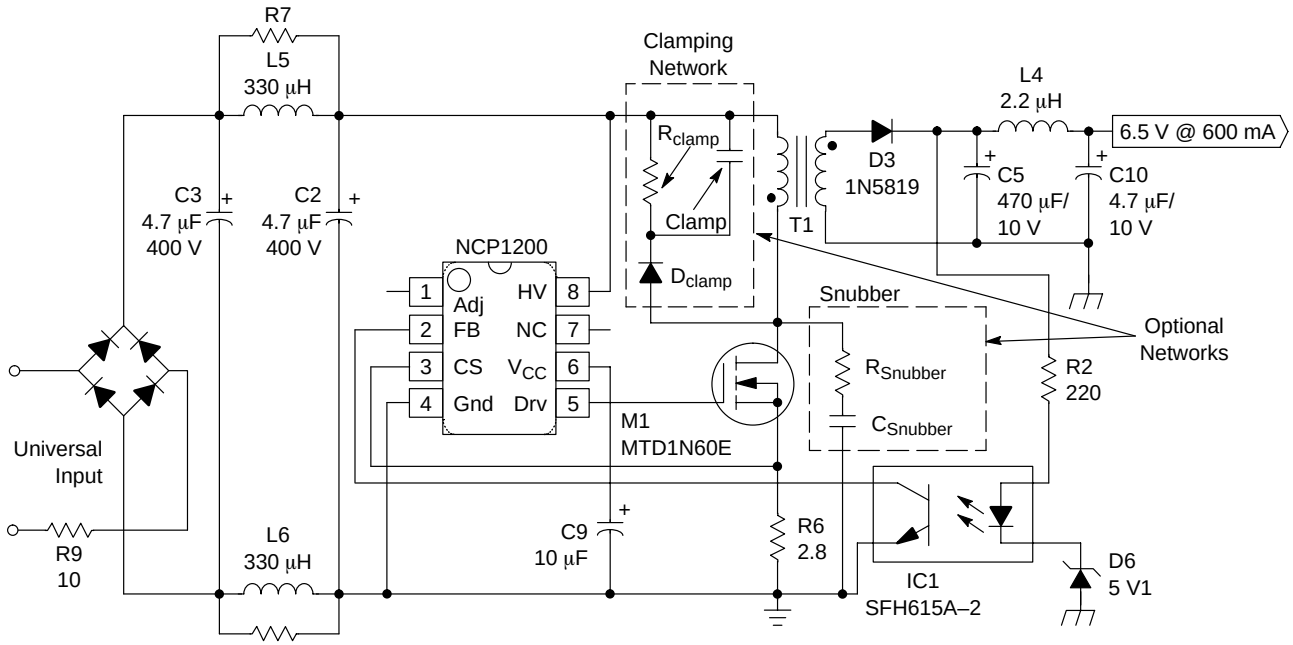


Figure 21. A typical AC/DC wall adapter showing the reduced part count thanks to the NCP1200

T1: Lp = 2.9 mH, Np:Ns = 1:0.08, leakage = 80 μH, E16 core, NCP1200P40

To help designers during the design stage, several manufacturers propose ready–to–use transformers for the above application, but can also develop devices based on your particular specification:

Eldor Corporation Headquarter
Via Plinio 10,
22030 Orsenigo
(Como) Italia
Tel.: +39–031–636 111
Fax : +39–031–636 280
Email: eldor@eldor.it
www.eldor.it
ref. 1: 2262.0058C: 3.5 W version
(Lp = 2.9 mH, Lleak = 80 μH, E16)
ref. 2: 2262.0059A: 5 W version
(Lp = 1.6 mH, Lleak = 45 μH, E16)

EGSTON GesmbH
Grafenbergerstraβe 37
3730 Eggenburg
Austria
Tel.: +43 (2984) 2226–0
Fax : +43 (2984) 2226–61
Email: info@egston.com
http://www.egston.com/english/index.htm
ref. 1: F0095001: 3.5 W version
(Lp = 2.7 mH, Lleak = 30 μH, sandwich configuration, E16)

Atelier Special de Bobinage
125 cours Jean Jaures
38130 ECHIROLLES FRANCE
Tel.: 33 (0)4 76 23 02 24
Fax: 33 (0)4 76 22 64 89
Email: asb@wanadoo.fr
ref. 1: NCP1200–10 W–UM: 10 W for USB
(Lp = 1.8 mH, 60 kHz, 1:0.1, RM8 pot core)

Coilcraft
1102 Silver Lake Road
Cary, Illinois 60013 USA
Tel: (847) 639–6400
Fax: (847) 639–1469
Email: info@coilcraft.com
http://www.coilcraft.com
ref. 1: Y8844–A: 3.5 W version
(Lp = 2.9 mH, Lleak = 65 μH, E16)
ref. 2: Y8848–A: 10 W version
(Lp = 1.8 mH, Lleak = 45 μH, 1:01, E core)

Improving the Output Drive Capability

The NCP1200 features an asymmetrical output stage used to soften the EMI signature. Figure 22 depicts the way the driver is internally made:

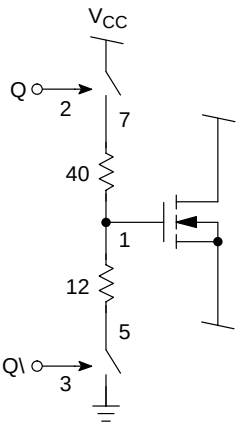


Figure 22. The higher ON resistor slows down the MOSFET while the lower OFF resistor ensures fast turn–off.

In some cases, it is possible to expand the output drive capability by adding either one or two bipolar transistors. Figures 23, 24, and 25 give solutions whether you need to improve the turn–on time only, the turn–off time or both. Rd is there to damp any overshoot resulting from long copper traces. It can be omitted with short connections. Results showed a rise fall time improvement by 5X with standard 2N2222/2N2907:

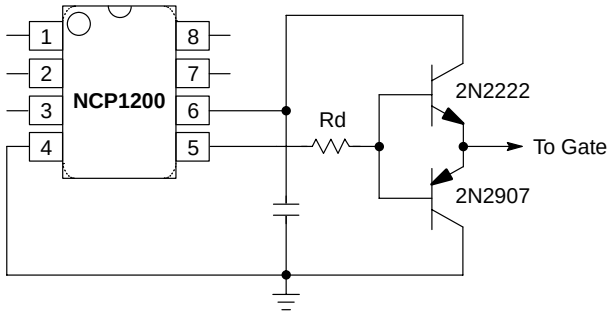


Figure 23. Improving Both Turn–On and Turn–Off Times

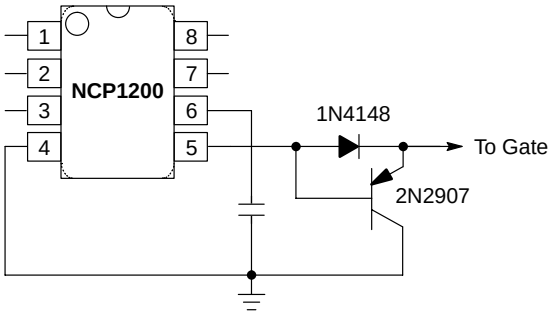


Figure 24. Improving Turn–Off Time Only

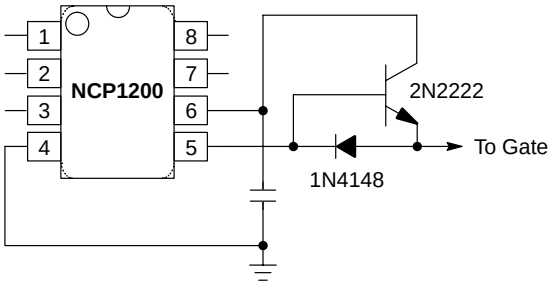


Figure 25. Improving Turn–On Time Only

If the leakage inductance is kept low, the MTD1N60E can withstand *accidental* avalanche energy, e.g. during a high–voltage spike superimposed over the mains, without the help of a clamping network. If this leakage path permanently forces a drain–source voltage above the MOSFET BVdss (600 V), a clamping network is mandatory and must be built around Rclamp and Clamp. Dclamp shall react extremely fast and can be a MUR160 type. To calculate the component values, the following formulas will help you:

$$R_{clamp} = \frac{2 \cdot V_{clamp} \cdot (V_{clamp} - (V_{out} + Vf\,sec) \cdot N)}{L_{leak} \cdot Ip^2 \cdot Fsw}$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple} \cdot Fsw \cdot R_{clamp}}$$

with:

V_{clamp}: the desired clamping level, must be selected to be between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

V_{out} + Vf: the regulated output voltage level + the secondary diode voltage drop

L_{leak}: the primary leakage inductance

N: the Ns:Np conversion ratio

F_{SW}: the switching frequency

V_{ripple}: the clamping ripple, could be around 20 V

Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn–off. The peak voltage at which the leakage forces the drain is calculated by: $V_{max} = Ip \cdot \sqrt{\frac{L_{leak}}{C_{lump}}}$ where C_{lump} represents the total parasitic capacitance seen at the MOSFET opening. Typical values for Rsnubber and Csnubber in this 4W application could respectively be 1.5 kΩ and 47 pF. Further tweaking is nevertheless necessary to tune the dissipated power versus standby power.

Available Documents

"Implementing the NCP1200 in Low–cost AC/DC Converters", AND8023/D

"Conducted EMI Filter Design for the NCP1200'', AND8032/D

"Ramp Compensation for the NCP1200'', AND8029/D

TRANSient and AC models available to download at: http://onsemi.com/pub/NCP1200

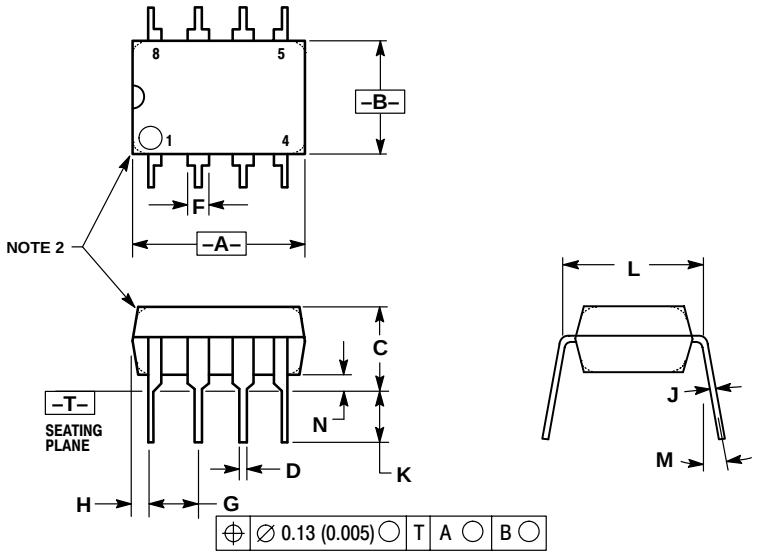
NCP1200 design spreadsheet available to download at: http://onsemi.com/pub/NCP1200

ORDERING INFORMATION

Device	Type	Marking	Package	Shipping
NCP1200P40	F_{SW} = 40 kHz	1200P40	PDIP8	50 Units / Rail
NCP1200D40R2	F_{SW} = 40 kHz	200D4	SO–8	2500 Units /Reel
NCP1200P60	F_{SW} = 60 kHz	1200P60	PDIP8	50 Units / Rail
NCP1200D60R2	F_{SW} = 60 kHz	200D6	SO–8	2500 Units /Reel
NCP1200P100	F_{SW} = 100 kHz	1200P100	PDIP8	50 Units / Rail
NCP1200D100R2	F_{SW} = 100 kHz	200D1	SO–8	2500 Units / Reel

PACKAGE DIMENSIONS

DIP8
P SUFFIX
CASE 626–05
ISSUE L

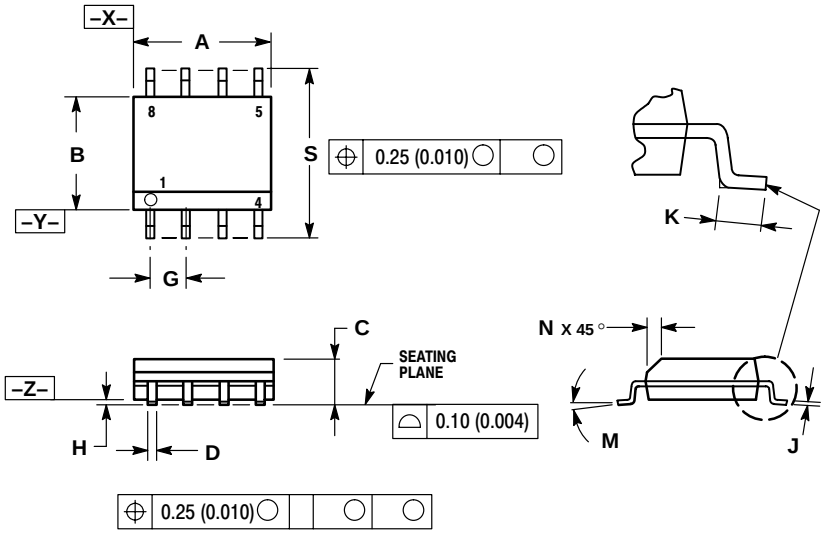


NOTE
1. I EN ION TO CENTER O EA EN OR E ARA E .
2. AC A E CONTO R O TIONA (RO N OR ARE CORNER).
3. I EN IONIN AN TO ERANCIN ER AN I 14.5 1 82.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3. 4	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 B C		0.100 B C	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2. 2	3.43	0.115	0.135
L	7.62 B C		0.300 B C	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PACKAGE DIMENSIONS

(SO–8)
D SUFFIX
CASE 751–07
ISSUE W



NOTE
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4. A I O ROTR ION 0.15 (0.006) ER I E.
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	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.18	0.1 7
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.06
D	0.33	0.51	0.013	0.020
G	1.27 B C		0.050 B C	
H	0.10	0.25	0.004	0.010
J	0.1	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

AND8023/D

Implementing the NCP1200 in Low-Cost AC/DC Converters

Prepared by: **Christophe Basso**
ON Semiconductor

ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

The NCP1200 implements a standard current mode architecture where the switch–off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part–count is the key parameter, particularly in low–cost AC/DC adapters, auxiliary supplies etc. Thanks to its proprietary Very High–Voltage Integrated Circuit (VHVIC) technology, ON Semiconductor NCP1200 will please experts as well as non–experts in the Switch–Mode Power Supplies (SMPS) arena as the following features demonstrate:

- **No need of auxiliary winding:** the VHVIC technology lets you supply the IC directly from the high–voltage DC rail. We call it Dynamic Self–Supply (DSS). In battery charger applications, you no longer need to design a special primary circuitry to cope with the transient lack of auxiliary voltage (e.g. when Vout is low).
- **Short–circuit protection:** by permanently monitoring the feedback line activity, the IC is able to detect the presence of a short–circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation. For given applications (e.g. constant output power supplies), you can easily disconnect this protective feature.
- **Low standby–power:** if SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping un–needed switching cycles, the NCP1200 drastically reduces the power wasted during light load conditions. In no–load conditions, the NPC1200 allows the total standby power to easily reach next International Energy Agency (IEA) recommendations.
- **No acoustic noise while operating:** instead of skipping cycles at high peak currents, the NCP1200 waits until the peak current demand falls below a user–adjustable 1/3rd of the maximum limit. As a result, cycle skipping can take place without having a singing transformer … You can thus select cheap magnetic components free of noise problems.
- **External MOSFET connection:** by leaving the external MOSFET external to the IC, you can select avalanche proof devices which, in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow, you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).
- **SPICE model:** a dedicated model to run transient cycle–by–cycle simulations is available but also an averaged version to help you closing the loop. Ready–to–use templates can be downloaded in OrCAD's PSpice, INTUSOFT's IsSpice and Spectrum–Software's μCap from the ON Semiconductor web site, www.onsemi.com, NCP1200 related section.
- **Low external part–count:** by integrating the principal electronic blocks in one die, the final NCP1200 implementation reveals an obvious gain in component reduction compared to other offers:
  - Built–in clock generator without external R–C elements. Operating frequencies at 40 kHz, 60 kHz or 100 kHz.
  - The optocoupler is directly wired to the feedback pin, the internal IC control taking care of the signal flow.
  - The 250 ns Leading Edge Blanking (LEB) circuitry also saves an external R–C network.

Dynamic Self–Supply

To avoid the use of a dissipative resistor, NCP1200 implements a controlled current source whose technology allows a direct connection to the high–voltage rail (up to 450 VDC). Figure 1a depicts the component arrangement. The current source always operates in the ON or OFF states, either delivering 4 mA or zero. As a result, the internal V_{CC} pin ramps up and down with a 2 V ripple centered around 10.6 V (Figure 1b).

April, 2001 – Rev. 3

Publication Order Number:
AND8023/D

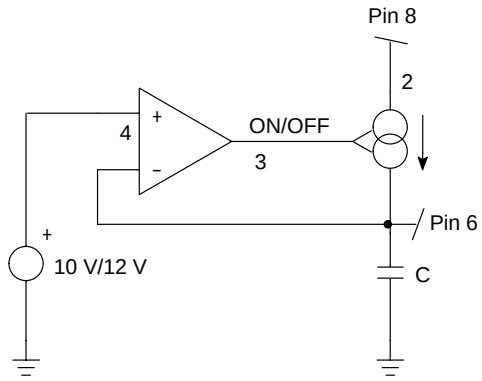

Figure 1a. Internal Implementation of the Dynamic Self–Supply

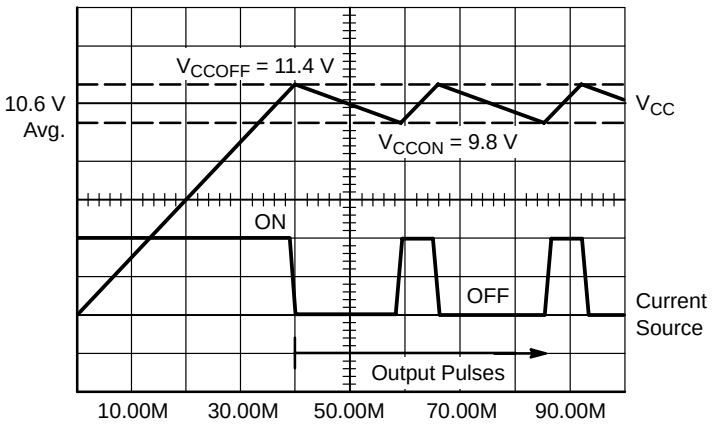

Figure 1b. DSS Waveforms During Start–Up and Normal Mode (CV_{CC} = 10 μF)

As one can see from Figure 1a, the current source supplies the IC and the Vcc capacitor. Thanks to the circuitry nature, the current source duty–cycle will automatically adjust depending on the IC average current consumption. Because this is a controlled source, this current stays constant whatever the high–voltage rail excursion (V_{HV}): from 100 VDC up to 370 VDC. The IC contribution to the total SMPS power budget is therefore: V_{HV} • I_{pin8}.

The internal IC consumption is made of the internal electronic blocks (clock, comparators, driver etc.) but also depends on the MOSFET's gate charge, Qg. If we select a MOSFET like the MTD1N60E, Qg equals 11 nC (max) and with a maximum switching frequency of 48 kHz, the average current necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is:

$$Fsw \cdot Qg = 530\ \theta A$$

Fsw = maximum switching frequency (Hertz)
Qg = MOSFET's gate charge (Coulomb)

If we now add this number to the normal IC consumption, we reach a typical total of 1.2 mA. The total IC power contribution alone is therefore: 330 V • 1.2 mA = 396 mW.

Decreasing the Standby Power

Below stands the future stand–by power recommendations issued by International Energy Agency (IEA). It concerns stand–by power when there is no output power demand:

Rated Input Power	Phase 1, January 2001	Phase 2, January 2003	Phase 3, January 2005
0.3 W and $\surd$ 15 W	1.0 W	0.75 W	0.30 W
15 W and $\surd$ 50 W	1.0 W	0.75 W	0.50 W
50 W and $\surd$ 75 W	1.0 W	0.75 W	0.75 W

A typical 4 W universal mains AC/DC wall adapter using the NCP1200 will exhibit a no–load power consumption of less than 380 mW @ Vin = 230 VAC. If a lower power consumption is required, you have several options to achieve it:

1. Use a MOSFET with lower gate charge Qg, but as we saw the driver's contribution is small.
2. Connect pin 8 through a diode to one of the mains input to apply a rectified half–wave on pin 8. Since we have either 4.0 mA or 0 synchronized with this half–sine wave, we should integrate the V–I product over a cycle to obtain the final average power. However, depending on the V_{CC} capacitor, we may have some half–sine portions where the current source if OFF: the V_{CC} capacitor level has not reached $UVLO_{Low}$ and the current source is left opened. To simplify the curves, we can assume a constant current flowing through pin 8 (actually the total NCP1200 consumption + a few losses) and integrate over a half–sine only. This leads to the final formula: $Pavg = \frac{2 * Vmainspeak * Iavg\ (Pin\ 8)}{}$. Our previous number drops to 250 mW. If you carefully look at Figure 2a, you will notice that the reverse voltage is sustained by the diode bridge. The maximum anode voltage of the Dstart diode is also clamped at the high–voltage rail. Therefore, a standard fast diode like the 1N4148 can safely be used in this option. However, because of the lack of synchronization between the DSS and the mains, it is necessary to equilibrate the diode voltage when both diode and DSS are inactive. This can be done by wiring a 220 kΩ in parallel with the diode. Otherwise, a standard 1N4937 can also do the job without any resistor in parallel…

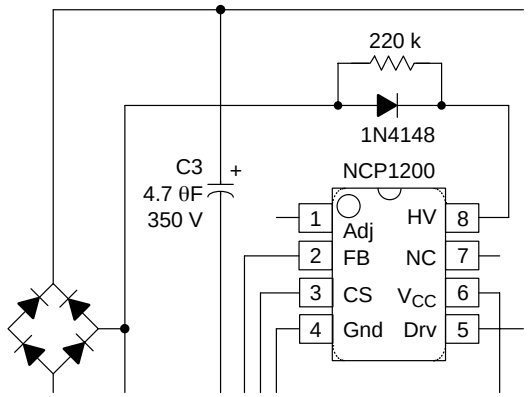

Figure 2a. A simple diode naturally reduces the average voltage on pin 8.

Figure 2b depicts the V_{CC} voltage obtained when using this method. Despite the lack of synchronization between the mains and the DSS, the average V_{CC} level is not affected.

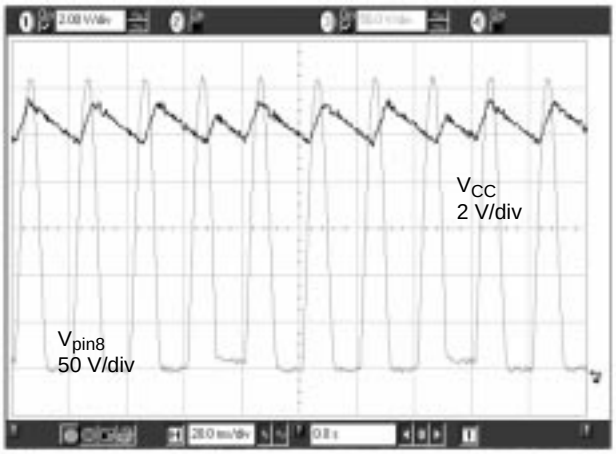

Figure 2b. By wiring a diode in series with pin 8, you do not affect the average V_{CC} level.

3. If you permanently force the V_{CC} level above V_{CCOFF} with an auxiliary winding, you will automatically disconnect the internal start–up source and the IC will be fully self–supplied from this winding. Again, the total power drawn from the mains will significantly decrease. However, make sure the auxiliary voltage never exceeds the 16 V limit, particularly in overshoot transients (e.g. the load is suddenly removed). To avoid this trouble and also implement an efficient Over Voltage Protection (OVP), Figure 3 schematic offers a possible solution:

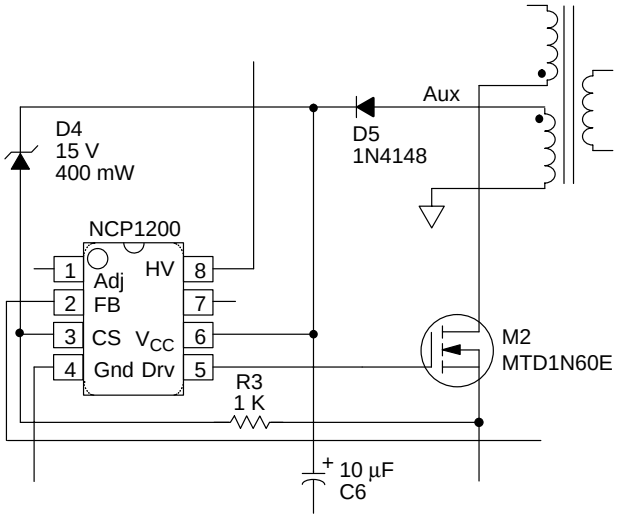

Figure 3. By wiring an auxiliary winding, you further decrease the standby power.

The typical operating voltage can be set at 12 V, with an overvoltage protection at 15 V. As a benefit, if the optocoupler fails, the SMPS turns into primary regulation mode and prevents any output voltage runaway. Typical measurements using this method gave a standby power of 84 mW at 230 VAC.

Skip Cycle Mode

The NCP1200 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin (pin 2). In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so–called skip cycle mode, also named controlled burst operation. Because this operation takes place at low peak currents, you will not hear any acoustic noise in your transformer. Figure 4a depicts how the IC implements the cycle skipping while Figure 4b shows typical switching patterns at different load levels.

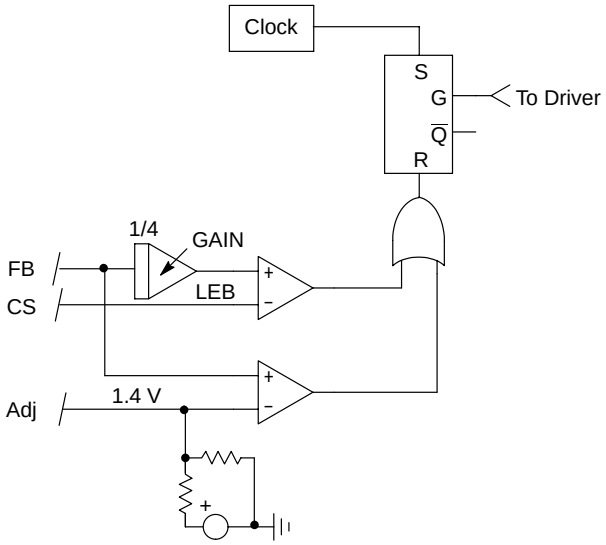

Figure 4a. NCP1200 Skip Cycle Implementation

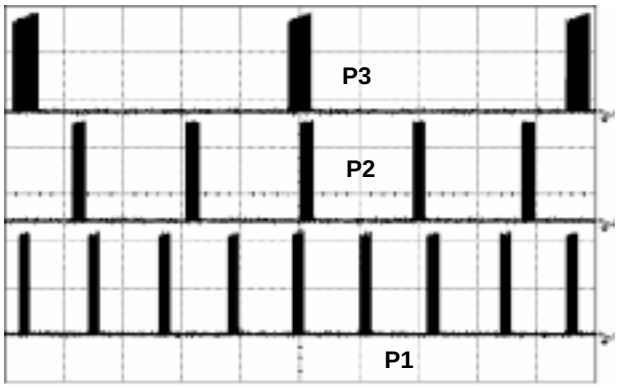

Figure 4b. Output pulses at various power levels (X = 5 μs/div) P3 < P2 < P1

When FB is above the skip cycle threshold (1.4 V by default), the peak current cannot exceed 1 V/Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1/4, 350 mV/Rsense by default (Figure 4c). The user still has the flexibility to alter this 1.4 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level.

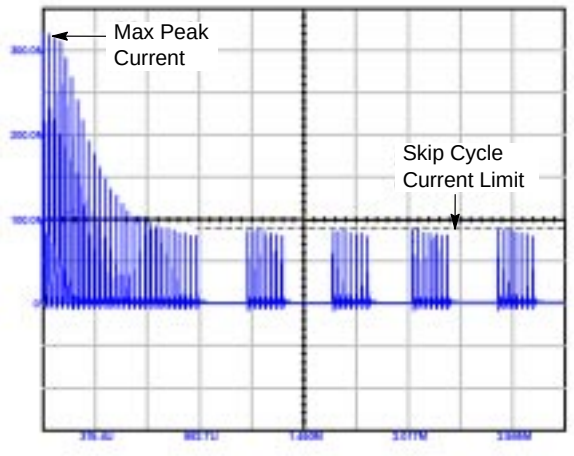

Figure 4c. The skip cycle takes place at low peak currents which guarantees noise–free operation.

The power transfer now depends upon the width of the pulse bunches (Figure 4b). Suppose we have the following component values:

Lp, primary inductance = 1 mH
Fsw , switching frequency = 48 kHz
Ip skip = 300 mA (or 350 mV/Rsense)

The theoretical (η = 100%) power transfer is therefore:

$$\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw = 2.16\ W \qquad \text{(eq. 2)}$$

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 2.1 . 0.1 = 216 mW.

Skip Adjustment

By altering the DC voltage present on pin 1, you have the ability to adjust the current level at which skip cycle operation will take place. By default, skip cycle occurs when the peak current demand falls below one third of the maximum peak current. If your design needs to enter standby at a higher or lower current (e.g. for noise reasons), you can alter the internal setpoint by imposing a different level than 1.4 V on pin 1. This can be achieved by using a resistor bridge between V_{CC} and ground. Pin 1 impedance is typically 25 kΩ.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is mandatory to implement a true short–circuit protection. A short–circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the FB pin level is pulled up to 4.8V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken optocoupler. To account for this situation, the NCP1200 hosts a dedicated overload detection scheme. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty–cycle. The system recovers when the fault condition disappears.

During the start–up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time–out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the V_{CCOFF} (typically 11.4 V) the device internally watches for an overload current situation. If this condition is still present when the V_{CCON} is reached, the controller stops the driving pulses, prevents the self–supply current source to restart and puts all the circuitry in standby, consuming as little as 350 μA typical (I_{CC3} parameter). As a result, the V_{CC} level slowly discharges toward 0. When this level crosses 6.3 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 11.4 V and again delivers output pulses at the V_{CCOFF} crossing point. If the fault condition has been removed before V_{CCON} approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 5 shows the evolution of the signals in presence of a fault.

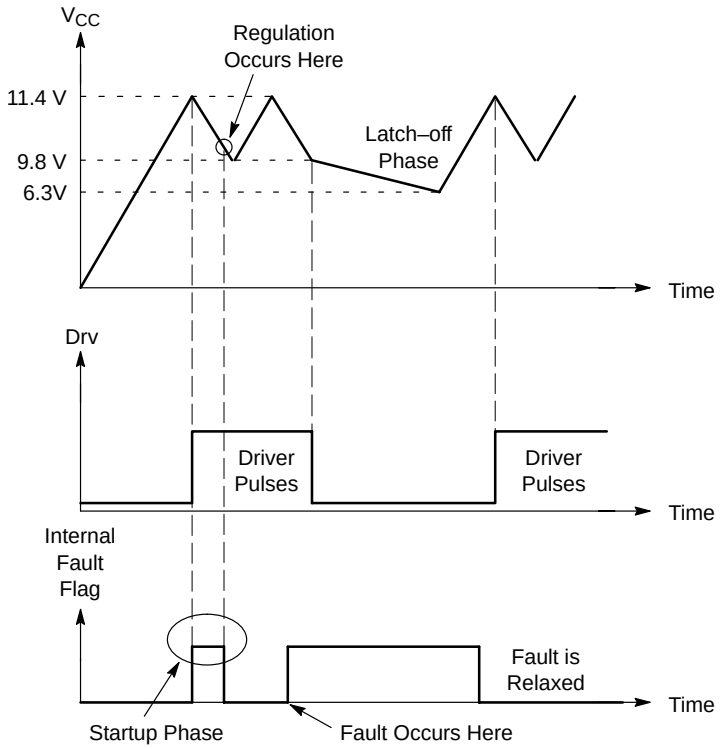

Figure 5. If the fault is relaxed during the V_{CC} natural fall down sequence, the IC automatically resumes. If the fault still persists when V_{CC} reached $UVLO_L$, then the controller enters burst mode until recovery.

* Always make sure that the output power you are looking for asks for an FB level less than the maximum value to avoid a false overload circuitry trigger.
* Because of component dispersions (NCP1200 frequency span, Rsense tolerance etc.), the overload protection will not be active as soon as you exceed the nominal power by a small amount. If you shoot for a given Pout, it is likely that the overload protection activates at roughly twice this value, especially if you implement a low–gain single zener feedback loop. You need to be sure that the output components sustain the corresponding current. Fortunately, because of temperature, the transformer core permeability will decrease as well as the primary inductance. This means less maximum power at higher temperatures.

Deactivating the Overload Detection

By wiring a 20 kΩ resistor from FB to ground, you permanently deactivate the overload protection circuitry. This is a very useful feature, especially if you need to build a constant output power converter.

Power Dissipation

The NCP1200 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the NCP1200 current consumption. The total power dissipation can be evaluated using: $(V_{HVDC} - 11\ V) \times I_{CC2}$. If we operate the device on a 250 VAC rail, the maximum rectified voltage can go up to 350 VDC. As a result, the worse case dissipation occurs on the 100 kHz version which will dissipate 340 . 1.8 mA @ Tj = 25°C = 612 mW (however this 1.8 mA number will drop at higher operating temperatures). A DIP8 package offers a junction–to–ambient thermal resistance $R_{\theta J-A}$ of 100°C/W. The maximum power dissipation can thus be computed knowing the maximum operating ambient temperature (e.g. 70°C) together with the maximum allowable junction temperature (125°C): $P_{max} = \frac{Tj_{max} - TA_{max}}{R_{J-A}} = 550\ mW$. As we can see, we do not reach the worse consumption budget imposed by the 100 kHz version. Two solutions exist to cure this trouble. The first one consists in adding some copper area around the NCP1200 DIP8 footprint. By adding a min–pad area of 80mm^2 of 35µ copper (1 oz.), $R_{\theta J-A}$ drops to about 75°C/W which allows the use of the 100 kHz version. The other solutions are a) add a series diode with pin 8 (as suggested in the above lines) to drop the maximum input voltage down to 225 V (707/π) and thus dissipates less than 410 mW b) implement a self–supply through an auxiliary winding to permanently disconnect the self–supply.

SO–8 package offers a worse $R_{\theta J-A}$ compared to that of the DIP8 package: 178°C/W. Again, adding some copper area around the PCB footprint will help decreasing this number: 12mm x 12mm to drop $R_{\theta J-A}$ down to 100°C/W with 35µ copper thickness (1 oz.) or 6.5mm x 6.5mm with 70µ copper thickness (2 oz.). As one can see, we do not recommend using the SO–8 package for the 100 kHz version with DSS active as the IC may not be able to sustain the power (except if you have the adequate place on your PCB). However, using the solution of the series diode or the self–supply through the auxiliary winding does not cause any problem with this frequency version.

Calculating the V_{CC} Capacitor for Overload

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 11.4 V to 9.8 V? The required time depends on the start–up sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 11.4 V to 10 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.5 mA, we can calculate the required capacitor using the following formula: $\Delta t = \frac{\Delta V \cdot C}{i}$, with ΔV = 2 V (eq. 3). Then for a wanted Δt of 10 ms, C equals 8 µF or 10 µF for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 350 µA typical. This happens at V_{CC} = 10 V and it remains stuck until V_{CC} reaches 6.3 V: we are in latch–off phase. Again, using the calculated 9.8 µF and 350 µA current consumption, this latch–off phase lasts: 109 ms.

Protecting the Power MOSFET

If the leakage inductance is kept low, an avalanche rugged MOSFET such as the MTD1N60E can withstand *accidental* avalanche energy, e.g. during a high–voltage spike superimposed over the mains, without the help of a clamping network. However, if this leakage path permanently forces a drain–source voltage above the MOSFET BVdss (e.g. 600 V), a clamping network is mandatory and must be built around a passive RC network or a Transient Voltage Suppressor (TVS). Figure 6a depicts the phenomenon while the below lines details the calculation steps:

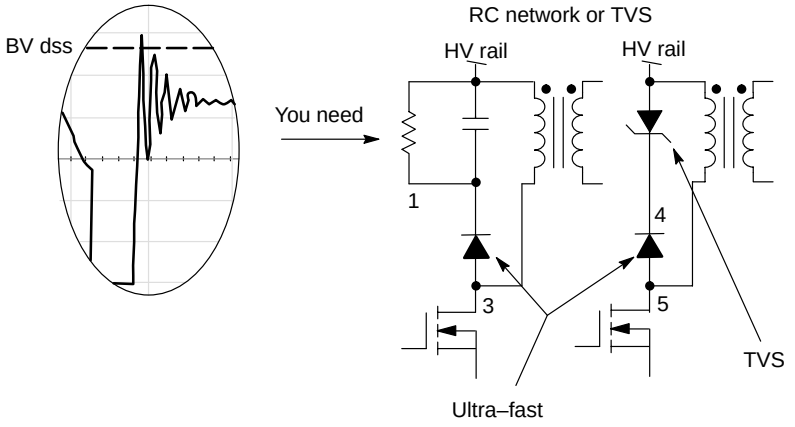

Figure 6a. Care must be taken to ensure a safe operation of the MOSFET

1. RC Network

The RC network will permanently impose a fixed clamping level that will oppose to the leakage voltage. As a result, the drain will be clamp to V_{HVrail} + Vclamp. You normally select a clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

To calculate the component values, the following formula will help you:

$$Rclamp = \frac{2 \cdot Vclamp \cdot (Vclamp - (Vout + Vf\,sec) \cdot N)}{Lleak \cdot Ip^2 \cdot F_{SW}} \quad \text{(eq. 4)}$$

$$Cclamp = \frac{Vclamp}{Vripple \cdot F_{SW} \cdot Rclamp} \quad \text{(eq. 5)}$$

The power dissipated by Rclamp can also be expressed by:

$$P_{Rclamp} = \frac{1}{2} \cdot Lleak \cdot Ip^2 \cdot F_{SW} \cdot \frac{\frac{Vclamp}{(Vout + Vf\,sec) \cdot N}}{\frac{Vclamp}{(Vout + Vf\,sec) \cdot N} - 1}$$

with:

Vclamp: the desired clamping level.

Ip: the maximum peak current (e.g. during overload)

Vout + Vf: the regulated output voltage level + the secondary diode voltage drop

Lleak: the primary leakage inductance

N: the Ns:Np conversion ratio

Fsw: the switching frequency

Vripple: the clamping ripple, could be around 20 V

2. Transient Voltage Suppressor

Despite the low–cost offered by the above RC solution, the clamping level unfortunately varies with the peak current. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die area is far bigger for a transient suppressor than that of zener. A 5 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. If the peak power is really high, then turn to a 1.5 KE200 which accepts up to 1.5 kW @ 1 ms.

Select the zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

3. Snubber Network

Another option lies in implementing a snubber network which will damp the leakage oscillations but also provide more capacitance at the MOSFET's turn–off. The peak voltage at which the leakage forces the drain is calculated by: $V_{max} = Ip \cdot \sqrt{\frac{Lleak}{Clump}}$ (eq. 6) where Clump represents the total parasitic capacitance seen at the MOSFET opening. Depending on the output power, you can either wire a simple capacitor across the MOSFET or an R–C network, as shown by Figure 6b.

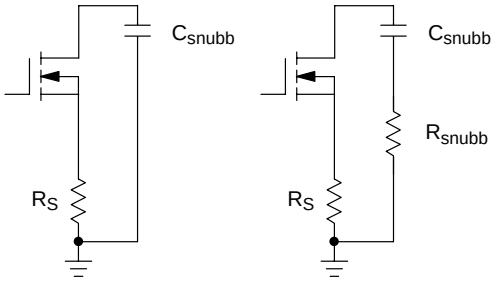

Figure 6b. If the output power is low, you can wire a simple capacitor MOSFET's drain and ground.

To calculate the values of this RC snubber, you need to measure the ringing frequency imposed by the leakage inductance and all the stray capacitances. Make sure you use a low capacitance probe, otherwise you might affect the observed frequency. Once you have it, calculate the impedance of the leakage inductance at the ringing frequency: $Z = 2 \cdot \quad \cdot F_{ring} \cdot L_{leak}$ (eq. 7). Wiring a resistor R whose value equals Z should solve the problem but at the expense of a large power dissipation. To lower the dissipated heat, you can wire a capacitor C in series with R: $C = \frac{1}{\cdot F_{ring} \cdot R}$ (eq. 8). If the output power is low, you can directly wire this capacitor between the MOSFET drain and ground (not between drain–source to avoid substrate injection). Unfortunately, you discharge this capacitor in the MOSFET every time it turns on... Further tweaking is thus necessary to tune the dissipated power versus standby power.

ON Semiconductor Protection Devices

SMPS protection clearly needs fast switching components to ensure a reliable operation in the event of dangerous transients. ON Semiconductor portfolio offers a comprehensive list of semiconductors dedicated to protection: fast diodes, zeners, TVS etc. Below is a small list of typical component you can select to protect the MOSFET in your application. The complete list of TVS devices can be found at the following URL: *www.onsemi.com* or by ordering the selection guide TVSPROMO1299/D by sending an email to: ONlit@hibbertco.com:

Clipping Elements

Reference	Nominal Voltage (V)	Average Power (W)	Maximum Peak Power
1N5953B	150	1.5	98 W @ 1 ms
1N5955B	180	1.5	98 W @ 1 ms
1N5383B	150	5.0	180 W @ 8.3 ms
1N5386B	180	5.0	180 W @ 8.3 ms
1N5388B	200	5.0	180 W @ 8.3 ms
P6KE150A	150	5.0	600 W @ 1 ms
P6KE180A	180	5.0	600 W @ 1 ms
P6KE200A	200	5.0	600 W @ 1 ms
1.5KE150A	150	5.0	1.5 kW @ 1 ms
1.5KE180A	180	5.0	1.5 kW @ 1 ms
1.5KE200A	200	5.0	1.5 kW @ 1 ms

Fast Diodes

Reference	V_{RRM}	Ton (typical)	IF max
MUR160	600 V	50 ns	3 A
MUR1100E	1000 V	25 ns	3 A
1N4937	600 V	200 ns	1 A
MSR860*	600 V	100 ns	8 A
MSRB860–1*	600 V	100 ns	8 A

*Soft recovery diodes

Calculating the Component Values for a Typical Application

Suppose that we would like to build a simple AC/DC wall adapter with an NCP1200 delivering a raw DC voltage with the following specs:

- Pout = 3.5 W
- Target efficiency: η = 75% $\rightarrow$ Pin = 4.66 W
- Vout = 6 V, Rload = 10.3 Ω, Iout = 580 mA
- V_{AC}in = 100 VAC to 250 VAC

The first step lies in calculating the peak rectified value obtained from this line range:

$$Vin_{peak} = Vin \cdot \sqrt{2} - 2 \cdot Vf \text{ with :} \qquad \text{(eq. 9)}$$

Vin: the AC input voltage
Vf: a forward drop of a bridge diode, 0.7 V @ Id

$\rightarrow Vin_{peak}$ = 140 V at low line
$\rightarrow Vin_{peak}$ = 352 V at high line

Bulk Capacitor

The bulk capacitor supplies the high–frequency current pulses to the SMPS, while it is refueled at low rate by the mains. Figure 7a shows a typical rectifying configuration. However, the bulk capacitor should be dimensioned to provide enough energy between the line peaks. The worse case appears at the lowest line level combined with the maximum output current. Figure 7b depicts the voltage waveform observed over C_{bulk} in Figure 7a example.

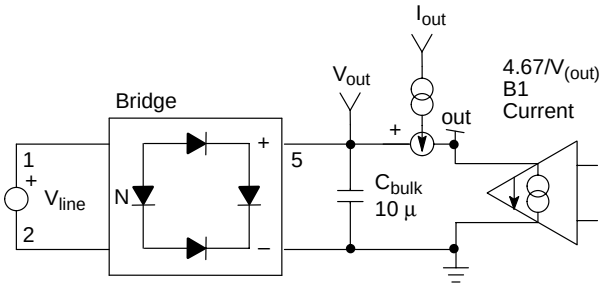

Figure 7a. A Full–Wave Rectification Configuration

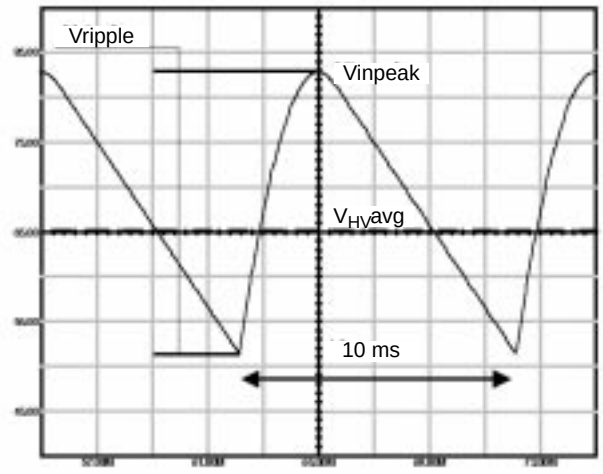

Figure 7b. A Typical Ripple Voltage over the Bulk Capacitor

To simplify the calculation, we will neglect the charging period and thus consider a total discharge time equal to $\frac{1}{2 \cdot Fline}$. From the design characteristics, we can evaluate the equivalent current (Iload) drawn by the charge at the lowest input line condition. Let's us adopt a 40% ripple level, or a 50 V drop from the corresponding Vin_{peak}. To evaluate the equivalent load current (which discharges Cbulk between the peaks), we divide the input power by the average rectified voltage:

$$Iload = \frac{Pin}{Vrect_{avg}} = \frac{Pout}{\pi \cdot \left(Vpeak - \frac{Vripple}{2}\right)} \text{ (eq. 10)} = 46 \text{ mA}$$

@ 100 VAC input voltage. Thanks to Figure 7b information, we can evaluate the capacitor value which allows the drop from Vpeak down to Vavg – (Vripple/2) to stay within our 50 V target: $dV \cdot C = i_{load} \cdot dt$:

$$Cbulk = \frac{Pout}{2 \cdot \pi \cdot Fline \cdot Vripple \cdot \left(Vpeak - \frac{Vripple}{2}\right)}$$

= (eq. 11) 9.3 θF or 10 θF for a normalized value.

High–voltage DC Rail Range

From the above formula, we can extract the ripple amplitude at any line level:

$$Vripple = Vpeak \cdot \left(1 - \sqrt{1 - \frac{Pout}{Cbulk \cdot \pi \cdot Fline \cdot Vpeak^2}}\right) \qquad \text{(eq. 12)}$$

Let us now calculate the final average DC value delivered to the SMPS at high but also low line:

$$V_{HVavg} = Vin \cdot \sqrt{2} - 2 \cdot Vf - \frac{Vripple}{2} \qquad \text{(eq. 13)}$$

$\rightarrow$ 115 VDC @ 100 VAC with a 50 Vpp ripple (initial target)
$\rightarrow$ 343 VDC @ 250 VAC with 19 Vpp ripple (calculated)

To confirm the validity of our calculation, a simple SPICE simulation can be run where the load is replaced by a current source. However, thanks to the feedback loop of the converter, the input current will vary depending on the line level. To avoid tweaking the current source at different line levels, Figure 7a's B1 element computes the input current according to the required power: $Iload = \frac{P_{SMPS}}{Vbulk}$ exactly as the final SMPS would do. Simulations gave a 29 Vpp ripple at low line (VHVavg = 126 V), turning into 12 Vpp at high line (VHV_{avg} = 342 V). The calculations gave less pessimistic results simply because we have neglected the capacitor re–charge time which reduces its discharge time.

Diode Bridge Selection

To select the right rectifiers, it is necessary to know the RMS current flowing through its internal diodes. Prior to reach this final result, we need to evaluate the diode conduction time. From Figure 8a, we can see that the diode starts to conduct when V_{AC}in reaches Vmin and stops when reaching Vin_{peak}:

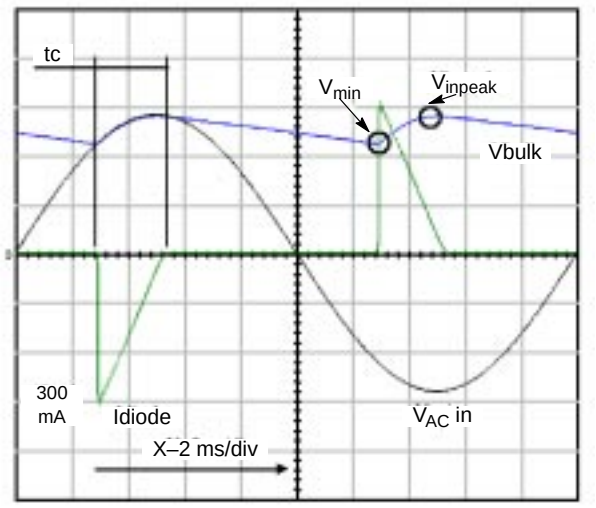

Figure 8a. When V_{AC}in reaches Vpeak, the diode stops conducting.

From a mathematical point of view, we can calculate the time V_{AC}in takes to reach Vmin:

$V_{AC}in \cdot \sin(\ \cdot t) = Vmin$. Since Vpeak is reached at the input sinusoid top (or one fourth of the input period), then the diode conducting time tc is simply:

$$tc = \frac{1}{4 \cdot Fline} - \frac{\sin^{-1}\frac{V\,min}{V_{AC}in \cdot \sqrt{2}}}{360 \cdot Fline} = 2.1\ ms\ @\ Vin =$$

100 VAC (eq. 14). During these 2.1 ms, Vbulk is the seat of a rising voltage equal to Vripple or 29 Vpp. This corresponds to a brought charge Q of: $Qbulk = Vripple \cdot Cbulk = 290\ \mu C$ (eq. 15).

From Figure 8a, we can calculate the amount of charge Q drawn from the input by integrating the input current over the diode conduction time: $Qin = \int_0^{tc} i_{diode}(t).dt$ (eq. 16). The expression of $i_{diode}(t)$ is: $Ipeak \cdot \frac{tc - t}{tc}$ (eq. 17). After proper integration, it comes: $Qin = \frac{1}{2} \cdot Ipeak \cdot tc$. If we now equate Qbulk and Qin and solve for Ipeak, it comes: $Ipeak = \frac{Qbulk \cdot 2}{tc}$ (eq. 17) or 280 mA peak, as confirmed by the simulation. We can now evaluate the RMS current flowing through the diodes: $Irms = \sqrt{Fline \cdot \int_0^{tc} (idiode(t))^2 \cdot dt} = Ipeak \cdot \sqrt{\frac{tc}{3} \cdot 2 \cdot Fline} =$

(eq. 18) 86 mA @ VAC = 100. A 400 V/1A diode bridge or four 1N4007 can thus be selected for the rectifying function. A small resistor is however put in series to ensure a surge current (when you plug the SMPS in the AC outlet) less than the diode maximum peak current (Ifsm).

Thanks to these numbers, we compute the apparent power at low line: 86 mA x 100 V = 8.6 VA which compared to our 4.66 Watts of active power (neglecting the input diode bridge and Cbulk losses) gives a power factor of: $PF = \frac{W}{V.A} = 0.54$ (eq. 19) conform to what we could expect from this kind of offline power supply. With a reverse voltage of 400 V, you can select either a 1 A/400 V bridge or 4 x 1N4007 diodes.

Transformer Calculation

Transformer calculation can be done in several manners: a) you evaluate ALL the transformer parameters, electrical but also physical ones, including wire type, bobbin stack–up etc. b) you only evaluate the electrical data and leave the rest of the process to a transformer manufacturer. We will adhere to the latest option by providing you with a list of potential transformer manufacturers you can use for prototyping and manufacturing. However, as you will discover, designing a transformer for SMPS is an iterative process: once you freeze some numbers, it is likely that they finally appear either over or under estimated. As a result, you re–start with new values and see if they finally fit your needs. To help you speed–up the transformer design, an Excel® design–aid sheet is available from the ON Semiconductor web site, *www.onsemi.com/NCP1200*. Let's start the process with the turn ratio calculation:

Turn Ratio and Output Diode Selection

The primary/secondary turn ratio affects several parameters:

- The drain plateau voltage during the OFF time: the lowest plateau gives room for the leakage inductance spike before reaching the MOSFET's BVdss: $Vplateau = \frac{Np}{Ns} \cdot (Vout + Vf) + VinDC_{max}$ (eq. 20).
- The secondary diode Peak Inverse Voltage (PIV) is linked to the turn ratio and the regulated output voltage by: $PIV = \frac{Ns}{Np} \cdot VinDC_{max} + Vout$ (eq. 21). If you lower the plateau voltage, you will increase the reverse voltage the secondary diode must sustain.
- The amp–turns equation Np . αIp = Ns . Is should satisfy the average output current demand with $Iout_{avg} = \frac{Ip \cdot toff \cdot Fsw \cdot \mu}{2 \cdot \frac{Np}{Ns}}$ (eq. 22). The α parameter illustrates the energy diverted by the leakage inductance at the switch opening (take 0.95 for low leakage designs).

With these numbers in mind, you can tweak the turn ratio according to the MOSFET BVdss and the diode. Below are given ON Semiconductor references for Schottky diodes:

Reference	V_{RRM} (V)	Io (A)	Case
MBRM120LT3	20	1.0	PowerMite
MBRM130LT3	30	1.0	PowerMite
MBRA130LT3	30	1.0	SMA
MBRA140LT3	40	1.0	SMA
MBRS120LT3	20	1.0	SMB
MBRS130LT3	30	1.0	SMB
MBRS140LT3	40	1.0	SMB
MBRS190T3	90	1.0	SMB
MBRS1100T3	100	1.0	SMB
MBRS320T3	20	3.0	SMC
MBRS330T3	30	3.0	SMC
MBRS340T3	40	3.0	SMC
MBRS360T3	60	3.0	SMC
1N5817	20	1.0	Axial
1N5818	30	1.0	Axial
1N5819	40	1.0	Axial

*Please see brochure BR1487/D for thermal and package details.

If we select an MBRA140LT3 (V_{RRM} = 40 V), then the PIV should be selected around 35 V at high line: $N = \frac{PIV - Vout}{VinDC_{max}}$ (eq. 23). If we select Np:Ns = 1: 0.08, then PIV = 34 V at 350 VDC input voltage which is okay with the selected diode. The plateau voltage at the drain will establish around 430 VDC: it leaves up to 170 V for the leakage spike.

The average diode Id_{avg} current is the converter's DC output current which is 580 mA, in line with our 1 A MBRA140LT3. The repetitive peak current seen by the diode is: $Ipeak_{sec} = \mu \cdot Ip \cdot \frac{Np}{Ns}$ (eq. 24). The diode RMS current Id_{rms} can be evaluated using: $Id_{rms} = Ipeak_{sec} \cdot \sqrt{\frac{Fsw \cdot toff}{3}}$ (eq. 25). Finally, the total conduction losses of the diode can be assessed through the following equation: $Pdiode_{avg} = Vf \cdot Id_{avg} + Rd \cdot Id_{rms}^2$ (eq. 26) with Vf the forward drop at Id = $Ipeak_{sec}$ and Rd, the dynamic resistance $\frac{dVf}{dId}$ @Id = $Ipeak_{sec}$.

Once Ip have been evaluated, you will need to confirm the agreement with the diode maximum rating specs.

Primary Inductance and Peak Current

When the SMPS operates in the Discontinuous Conduction Mode (DCM), the sum of the ON and OFF times equal the switching period: $ton + toff = \frac{1}{Fsw}$ (eq. 27). From the FLYBACK equations, we can easily calculate t_{on} and t_{off}. During the ON time, the converter applies VinDC to the primary inductance which forces the current to build up with a slope of $\frac{VinDC}{Lp}$. Because the NCP1200 operates in current–mode, the ON time expires when the current setpoint Ip has been reached: $ton = \frac{Lp \cdot Ip}{VinDC}$ (eq. 28). In DCM, we must satisfy equation 27. That is to say, the OFF time lasts until the core is fully reset or the secondary current has come back to zero: $toff = \frac{Lp \cdot Ip}{N \cdot (Vout + Vf)}$ (eq. 29), with N the turn ratio between the secondary and the primary and Vf the secondary rectifier forward drop at a given current (≈1 V). In a FLYBACK SMPS, the input power flow is evaluated using the formula: $Pin = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw$ (eq. 30) with Lp the primary inductance, Ip the primary current at the end of the ON time and Fsw the converter's switching frequency. Pin is linked to Pout by the efficiency using: $Pin = \frac{Pout}{\pi}$ (eq. 31). Combining equations 27, 28, 29, 30, 31 and solving for Lp we obtain the critical inductance value above which we would go into Continuous Conduction Mode (CCM) at the lowest input voltage $VinDC_{avg} - \frac{Vripple}{2}$ and maximum output power:

$$Lp \quad \left(\frac{N \cdot (Vout + Vf) \cdot VinDC}{N \cdot (Vout + Vf) + VinDC}\right)^2 \cdot \frac{\pi}{2 \cdot Pout \cdot Fsw}$$

(eq. 32). Finally, the peak current corresponding to this inductance value can be computed from equations 30, 31: $Ip = \sqrt{\frac{2 \cdot Pout}{\pi \cdot Lp \cdot Fsw}}$ (eq. 33). With our example data in

mind, the calculation gives a primary inductance of 6.4 mH at Fsw = 40 kHz (nominal NCP1200 switching frequency). The corresponding Ip is 190 mA.

In equation 30, two unknowns exist: Lp and Ip. The above calculations show how to select Lp from a conduction mode point of view (always stay in DCM), which leads to a final operating peak current. However, from equation 6, we can see that a high peak current leads to a large inductance spike when the switch opens. We should then try to work at a low primary peak current to avoid this potentially lethal voltage kick. However, working at a low peak current means a higher primary inductance to satisfy equation 30 which, in turn, induces a larger leakage energy (the leakage inductance is proportional to the square of the primary turns)…We thus need a balance between the low primary current requirements combined with our low leakage inductance needs. Let's go over the whole process and see how we can tweak the parameters, keeping in mind that the lowest turn number also ensures the lowest manufacturing cost…

Step 1:

Evaluate the critical inductance value with eq. 32. Ip is calculated via eq. 33 → Lp = 6.4 mH, Ip = 190 mA.

Step 2:

The NCP1200 limits the peak current to: $\frac{0.9\ V}{Rsense}$ (eq. 34), 0.9 V varying ±10%. We should then select a sense resistor from the E24 series, also affected by a ±5% tolerance, which authorizes the peak current to grow up to the number calculated by eq. 33. The E24 shunt series looks like the following for medium output powers: …0.56 Ω, 0.68 Ω, 0.82 Ω, 1 Ω, 1.2 Ω, 1.5 Ω, 1.8 Ω, 2.2 Ω, 2.7 Ω, 3.3 Ω, 3.9 Ω, 4.7 Ω… As you can see, it will be easier to pick up an available reference from the E24 series then refine the inductance value to reach our goal. This option avoids to freeze the inductance without having the necessary flexibility on the shunt. From step 1 and equation 34, Rshunt = 4.24 Ω. If we select 4.7 Ω, we will have difficulties to reach our peak current with the previous inductance (remember that we cannot increase it otherwise we go into CCM). Another problem would be the FB permanently pushed to the maximum current demand and triggering the overload mode. Therefore, let's select 3.9 Ω from the E24 series and later on diminish the inductance value to fit eq. 30. Now, we need to apply worse cases of tolerance variations to see how they affect the final output power result. To refine the calculation, we will include the NCP1200 overcurrent propagation delay which is 120 ns typical. Propagation delay corresponds to the actual time taken by the internal chain to really pull the MOSFET's gate to ground when the peak current setpoint has been reached. During this time, the primary current keeps growing up with a slope of $\frac{VinDC}{Lp}$ (eq. 36). Figure 9a details this principle.

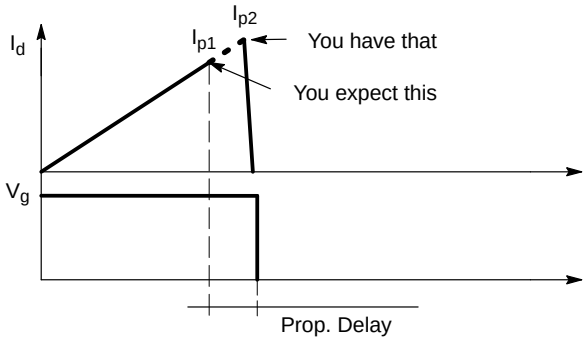

Figure 9a. The NCP1200 propagation delay leads to a slightly higher peak current than expected.

The data we have are: Lp = 6.4 mH ±10%, Fsw = 40 kHz ±15%, Rsense = 3.9 Ω ±5% and $Vsense_{max}$ = 0.9 ±5%. From these values, we can combine worse case together to see a) are we always able to deliver our 3.5 W? b) what is the maximum output power capability?:

$$Pout_{min} = \frac{1}{2} \cdot Lp_{min} \cdot \left(\frac{Vsense_{min}}{Rsense_{max}} + \frac{VinDC_{min}}{Lp_{min}} \cdot t_{prop} \right)^2 \cdot Fsw_{min} \quad 3.3\ W \qquad \text{(eq. 37)}$$

$$Pout_{max} = \frac{1}{2} \cdot Lp_{max} \cdot \left(\frac{Vsense_{max}}{Rsense_{min}} + \frac{VinDC_{max}}{Lp_{max}} \cdot t_{prop} \right)^2 \cdot Fsw_{max} \quad 6.3\ W \qquad \text{(eq. 38)}$$

From the above numbers, we can see that we cannot deliver the target power in the worse case. Let's reduce the Rsense value to the next reference, 3.3 Ω: (you can use the spreadsheet to speed–up this process)

$Pout_{min}$ = 4.6 W
$Pout_{max}$ = 8.8 W
Rsense = 3.3 Ω, Lp = 6.4 mH

From these results, we can consider that 4.6 W is more than we need. By reducing the inductance value to 5.5 mH, the numbers are updated to:

$Pout_{min}$ = 4 W
$Pout_{max}$ = 7.6 W
Rsense = 3.3 Ω, Lp = 5.5 mH

With this case, the 4 W output power offers a guardband above 14% (4 W compared to 3.5 W) and it will thus leave some dynamic on the FB level without triggering the overvoltage protection circuitry.

Step 3:

This final step should give us the type of transformer we can use for our application. In FLYBACK converters, we need a gap to expand the storage capability of a given un–gapped core. The gap presence imposes a decrease in the remnant flux density Br and allows a larger field excursion before reaching the saturation (a gap does not change the saturation level Bsat nor the coercitive field values Hc). However, the gap is usually made by grinding

the center leg of the selected core (E or RM etc.). This operation can be difficult, especially on small cores used for powers as the one we are looking for. For this reason, most of the manufacturers do not recommend gaps above 0.6 mm. Large gaps also generate fringing flux which can lead to disturbing ElectroMagnetic Interference (EMI) leaks.

Two methods can be used for the design of the transformer depending on the information given by the core manufacturer:

First Method

1. From eq. 34 and Lp value, evaluate the maximum required storage energy capability $Lp_{max}.Ip^2_{max}$.
2. Depending on your application constraints (dimensions, weight etc.) select a given core geometry (E, RM etc.).
3. From the core manufacturer handbook, look at the graph which gives $L.I^2$ versus A_L curves. Draw a horizontal line which corresponds to the above required $L.I^2$ number for the selected geometry. Any core references appearing below this curve can be used. However, in an attempt to minimize the leakage inductance (less primary turns), try to select the largest A_L .
4. Plot a vertical line which passes through the intersection point step 3 created. This gives you the A_L.
5. From the A_L versus air–gap length curve, extract the corresponding air–gap and check if it is machinable (< 600 μm?).
6. From the A_L, calculate the primary turn number with:

$$N = \sqrt{\frac{Lp}{AL}} \quad \text{(eq. 39)}$$

7. Finally, check that Bs . N . Ae > Lp_{max} . Ip_{max} with Bs the core saturation limit at 100°C and Ae the effective core area. If it fails, reduce the A_L value by keeping the air–gap within reasonable limits and check that the updated turn numbers are still in agreement with the bobbin capability (the transformer manufacturer will normally tell you about it).
8. With the help of the spreadsheet, you have the choice to tweak Lp in order to decrease the turn number to finally reduce the leakage inductance.

Second Method

1. Depending on your application constraints (dimensions, weight etc.) select a given core geometry (E, RM etc.)
2. From the calculated Lp value, evaluate the *minimum* turn number with: $N = \frac{Lp_{max} \cdot Ip_{max}}{Bs \cdot Ae}$ (eq. 40)
3. You now need to calculate the specific inductance value by applying: $AL = \frac{Lp}{N^2}$
4. Evaluate the desired gap length lg (in mm) through the following formula: $lg = \frac{\theta o \cdot \theta a \cdot N^2 \cdot Ae - Lp \cdot lm}{Lp \cdot \theta a} \cdot 1000$ (eq. 41) with μo the air permeability ($4.\pi.10^{-7}$), μa the amplitude permeability (the core permeability at high flux excursions), N the turn number, lm the mean magnetic path length (m).

Numerical Application

For our 3.5 W charger operating a 40 kHz, we have selected an E16 core in B2 material (Thomson–LCC) offering the following parameters:

Ae = 0.0000198m²
Bsat = 300mT @ 100°C
μa > 1000 (T° > 100°C, B = 330mT)
lm = 0.0348 meter

To lower the turn numbers (for leakage but also for winding time reasons), we have purposely decreased the previously calculated Lp value down to 2.7 mH which gives an operating peak current of 290 mA and a sense resistor of 2.7 Ω.

Applying method 1 leads to:

AL = 60 nH/turn²
Np = 212 turns
Ns = 17 turns

The manufacturer will need the primary and secondary RMS currents calculated at the lowest line level:

$$Isec_{rms} = Ipeak_{sec} \cdot \sqrt{\frac{Fsw \cdot toff}{3}} \text{ or } 2.7 \text{ A (eq. 42)}$$

The primary current is obtained with:

$$Iprim_{rms} = Ipeak_{prim} \cdot \sqrt{\frac{Fsw \cdot ton}{3}} \text{ or } 184 \text{ mA (eq. 43)}$$

MOSFET Selection

The transformer being designed, we can look at the MOSFET type. From equation 20, the plateau voltage (during the toff duration) rises up to 438 V. By selecting a 600 V device, we ensure enough headroom for the leakage spike. If this spike is finally too energetic, we can either clamp it with an adequate network or choose a 800 V MOSFET. From equation 43, a 1 A MOSFET is suitable and can be selected from the below devices:

Reference	BVdss (V)	$RDS_{(ON)}$ (Ω)	Peak Current (A)	Package
NTB10N60	600	0.75	–	TO–220
NTB10N60	600	0.75	–	D_2PAK
NTD4N60	600	2.3	–	DPAK
NTP6N60	600	1.1	–	TO–220
NTP6N60	600	1.1	–	D_2PAK
MTP4N80E	800	3.0	4.0	TO–220
MTD1N80E	800	12	1.0	DPAK
MTD1N60E	600	8.0	1.0	DPAK
MTB3N60E	600	2.2	3.0	D_2PAK
MTP2N60E	600	3.8	2.0	TO–220
MTP3N60E	600	2.2	3.0	TO–220
MTP6N60E	600	1.2	6.0	TO–220

Let's pick–up an MTD1N60E which features the following specs:

BVdss = 600 V
$RDS_{(ON)}$ = 13 Ω @ Tj = 100°C
Case = DPAK
$R_{\theta JA}$ = 71 °C/W on min pad area
Max junction temperature = 150°C
Qg = 11 nC max. (V_{GS} = 10 V)
Coss = 40 pF

If we operate at an ambient of 70°C, the maximum power the component can dissipate on free–air is given by: $Pmax = \frac{Tj_{max} - T_A}{R_{JA}}$ = 1.1 W (eq. 45). The total MOSFET losses are a combination of the conduction losses and the switching losses. From equation 43, we can compute the MOSFET conduction losses: $Pcond = RDS_{(ON)} \cdot Id^2_{RMS}$ = 440 mW (eq. 46).

Switching losses appear because of the overlap between drain current and drain–source voltage during transitions. We have losses during the switch closing (P_{sw}on) but also during the switch opening (P_{sw}off). In DCM, the turn–on losses are mainly created by the recurrent discharge of the stray parasitic capacitors in the MOSFET. The MOSFET contributes to these losses via its Coss capacitor. Unfortunately, Coss does not linearly vary with Vds during the transition and an accurate calculation would require the use of an equivalent capacitor, resulting from the Coss integral over the switching period. To simplify the evaluation, we will stick to the classical Coss given in the data–sheet, 40 pF max and neglect the other stray capacitance (e.g. from the transformer or a snubber): $P_{sw}on = \frac{Coss \cdot (Vds_{plateau})^2 \cdot Fsw_{max}}{2}$ (eq. 47) with $Vds_{plateau}$ given by eq. 20. We obtain 175 mW. To estimate this ON transition duration, we can calculate the time t_s needed to push enough Coulomb in the gate to properly bias the MOSFET. However, the time during which the drain falls corresponds to the charging time of the Miller capacitance or the V_{GS} "plateau" duration. This plateau, which occurs at 6 V for the MTD1N60E is not the V_{GS}th parameter (≈3 V). From the MOSFET's gate–charge chart, we can extract the amount of necessary Coulomb Qg2 to cross–over the plateau area: 3.2 nC. The time needed to push or extract this charge with a given gate resistor is: $tson = \frac{Qg2 \cdot Rsource}{Vcc - Vplateau}$ (eq. 48) and $tsoff = \frac{Qg2 \cdot Rsink}{Vplateau}$ (eq. 49), with V_{CC} the lowest supply level delivered by the DSS (9.2 V). To minimize the EMI problems, the NCP1200 output impedance is asymmetrical: Rsource = 40 Ω (turn–on) while Rsink = 12 Ω (turn–off), as already accounted for in eq. 47 and 48. With these values, we obtain ts_{on} = 45 ns and ts_{off} = 6.4 ns. These numbers are rather low because of the small parasitic elements constituting the MTD1N60E. At the switch opening, the MOSFET current immediately drops thanks to a small ts_{off}. But the leakage inductance forces Ip to circulate through all the stray capacitance (Clump) and pulls up the drain with a slope of $\frac{Ip}{Clump}$ (eq. 50). Because the MOSFET is fully open when Vds rises, there are very few associated losses. In the case Vds (rising) and Ip (decreasing) would intersect together in their middle, the final P_{sw}off losses could be computed by: $P_{sw}off = \frac{Vds_{max} \cdot Ip_{max} \cdot ts_{off} \cdot Fsw_{max}}{6}$ (eq. 51) with Vds the highest drain–source level (600 V in worse case and without a clamping network). After computation, we obtain 14 mW a slightly optimistic number. The total power dissipation is thus: 440 mW + 175 mW + 14 mW = 630 mW, neglecting the gate losses. This number is below eq. 45 result and offers a comfortable *theoretical* security margin. We will confront these results with practical measurements on the board to ensure reliable operation.

Output Capacitor Selection

To evaluate the output capacitor value Cout, we need to define a given, acceptable level of ripple. The ripple finds its root in two different sources:

1. The natural integration of the secondary current (amputed by the DC current delivered to the load) through the capacitance gives birth to a capacitive voltage of $Vcap = \frac{1}{Cout} \cdot \int i_{(t)} \cdot dt$. This integral is valid during the secondary current decay until DCM is reached (Isec = 0). The remaining portion of time includes the dead–time (if any) plus the switch ON time.
2. The total parasitic contribution of Equivalent Series Resistor (ESR) and Inductor (ESL) that produce a voltage spike at every switch openings. The ESR contribution only is usually culprit for the majority of the ripple amplitude.

Thanks to simulation**,** Figure 9b is able to show these components separately and how they combine together:

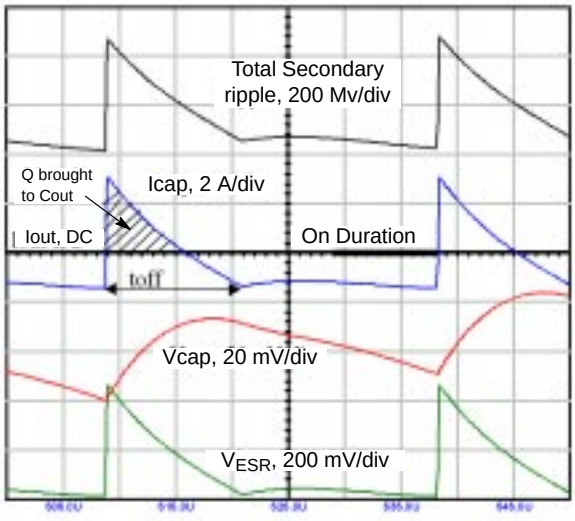

Figure 9b. The final ripple is made of the ESR and the output capacitance.

By looking at Figure 9b's INTUSOFT's IsSpice plot, we can evaluate the output capacitor voltage rise until the core is fully reset (t_{off} caption). First, let's calculate this t_{off} duration knowing that the secondary downslope is: $S_{sec} = \frac{(Vout + Vf) \cdot N^2}{Lp}$ or 405 mA/µs. With a secondary peak current Isec equal to N . Ip = 0.29 **.** 12.5 = 3.6 A, toff will last 8.9 µs for a 3.5 W nominal output power ($Iout_{DC}$ = 500 mA). With this value in mind, we can calculate the integrated voltage over Cout when subject to a ramping down current starting from (Isec – $Iout_{DC}$) and lasting 8.9 µs:

$$Vcap = \frac{1}{Cout} \cdot \int_0^{toff} \frac{toff - t}{toff} \cdot (Isec - Iout_{DC}) \cdot dt = \frac{toff}{2 \cdot C} \cdot (Isec - Iout_{DC})$$

. Thanks to this formula, we can extract the Cout value by: $Cout = \frac{toff \cdot (Isec - Iout_{DC})}{2 \cdot Vcap}$ or 490 µF with Vcap = 30 mV ripple. The simulation show higher ripple numbers because of an output power of 4.5 W.

Unfortunately, the ESR contribution is by far the higher contributor to the output ripple. This ohmic loss will generate a thin voltage spike equal to: R_{ESR} . (Isec–$Iout_{DC}$). In our case, a 100 mΩ ohmic loss produces up to 300 mV and adds up with the capacitor voltage ripple. The ESR also affects the capacitor dissipation by: $P_{Cout} = I^2_{capRMS} \cdot R_{ESR}$. You can smooth the ESR spike by inserting a secondary LC filter, as proposed by the various sketches of this application note.

Simulating the NCP1200

To ease your design phase, we have developed a transient and an AC averaged SPICE model for the NCP1200. Ready–to–use templates are available to download at www.onsemi.com in these three versions: INTUSOFT's IsSpice4, OrCAD's PSpice and Spectrum–Software's θCap. Describing these models is beyond the scope of this application note. However, we will show some typical waveforms you could quickly get with the help of these tools. Figure 10a portrays a typical IsSpice transient simulation using the NCP1200 in our 3.5 W charger application.

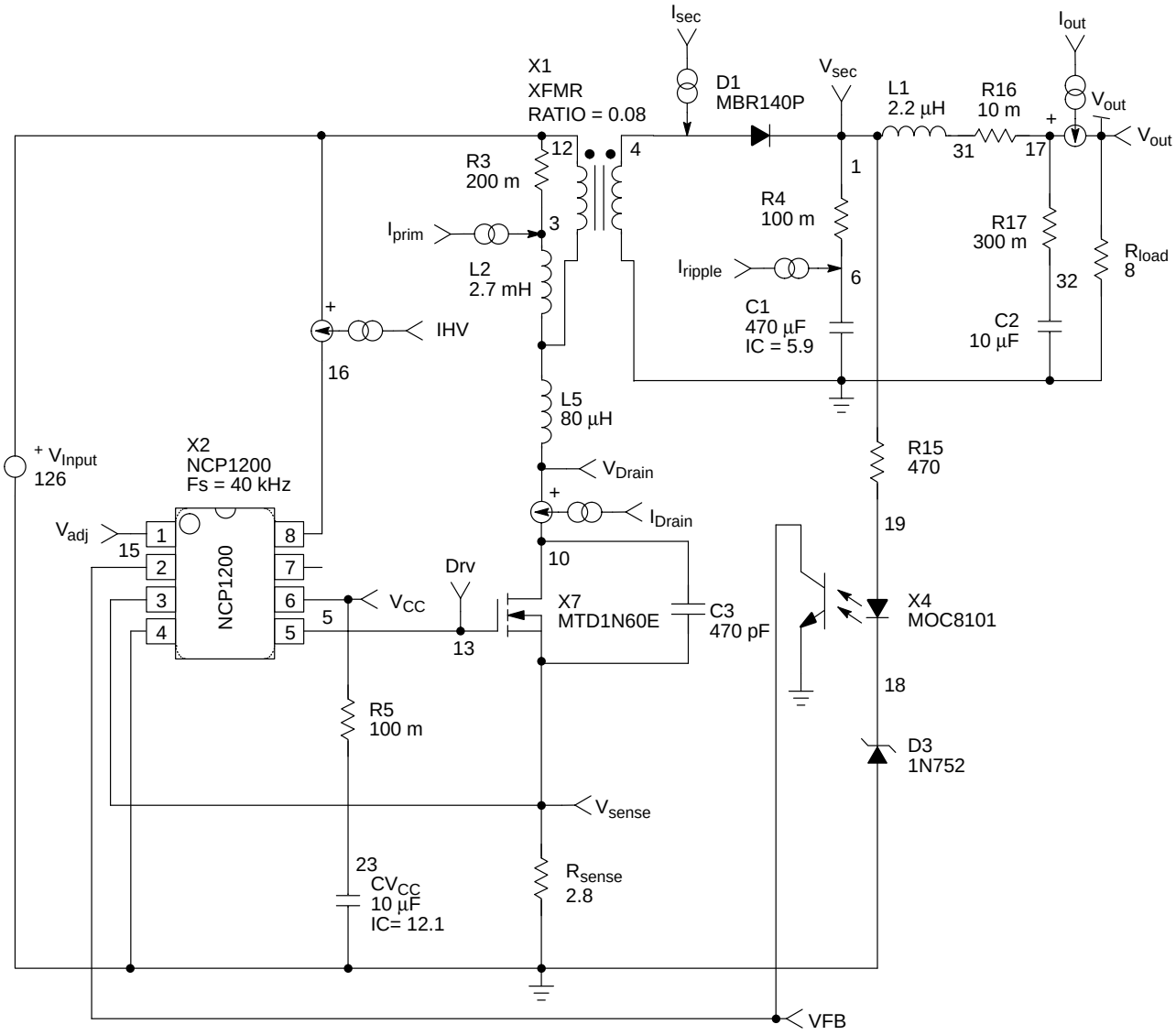

Figure 10a. A typical transient analysis of the NCP1200 with a dedicated SPICE model. C3 is purposely wired between drain–source to highlight the potential substrate injection problems.

The model includes the start–up source, various propagation delays, the short–circuit protection and the driver dual impedance concept. Typical waveforms are shown on Figure 10b and 10c. Thanks to short simulation times, the NCP1200 SPICE model will help you confirming the theoretical results you have already calculated.

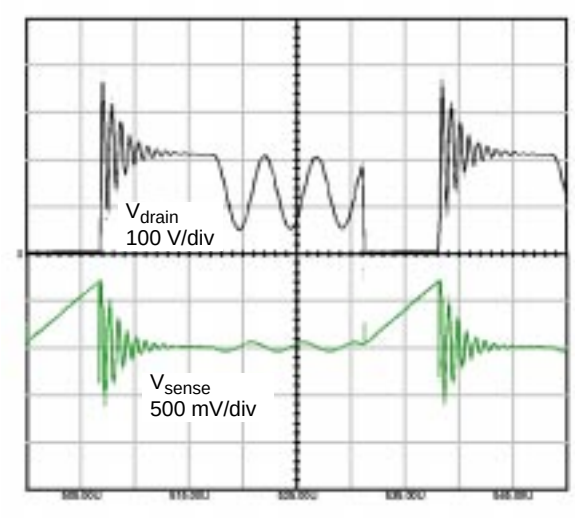

Figure 10b. Steady–State Drain–Source and Sense Voltages

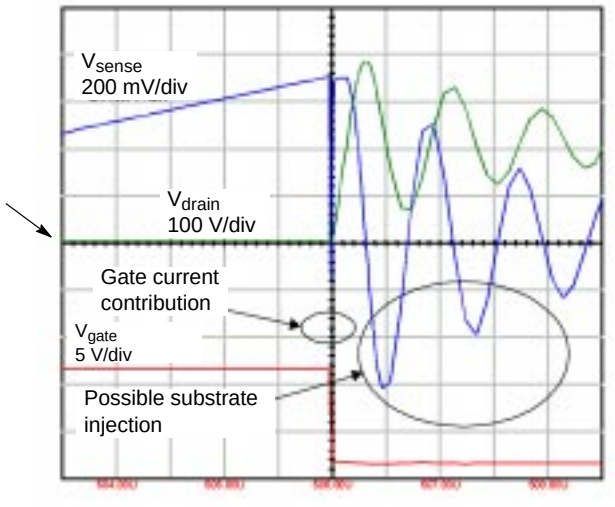

Figure 10c. Zoomed portion of MOSFET switch–off time when the snubber capacitor is wired between drain and source.

By feeding the various components with the choices you have made (e.g. transformer turn ratio), you can immediately verify that you do not exceed the safety limits. Such verifications could end–up into smoke on a real prototype test …

The Final Application Schematic

Figure 11a depicts the complete application schematic used in our NCP1200 AC/DC demoboard. Thanks to the weak leakage inductance exhibited by the transformer (≈80 μH), a simple capacitor in parallel with the MOSFET allows a safe operation up to 250 VAC, but to a slight detriment of switching losses (eq. 47).

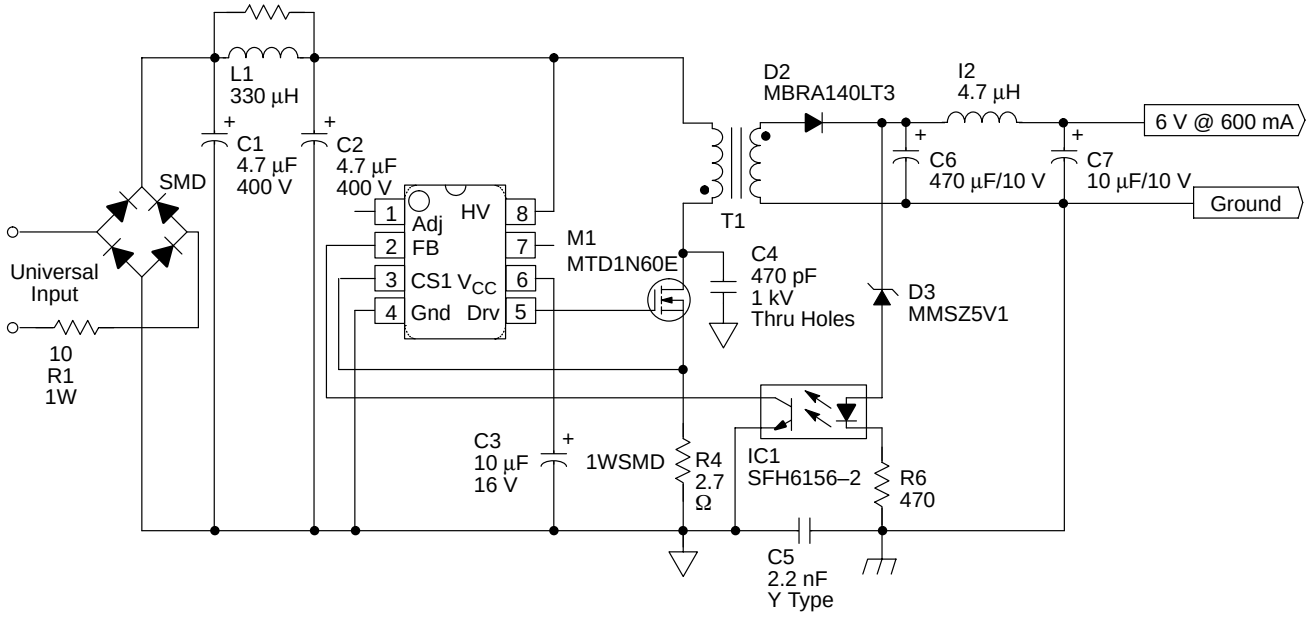

Figure 11a. The 3.5 W AC/DC adapter available as a demoboard

The PCB exhibits compact dimensions (64mm x 35mm) and includes a simplified EMI filter (L1). In case the common mode noise induced by M1 switching too fast exceeds the standard limits, you still have the option to slow it down a little bit by inserting a resistor between pin 5 and its gate. Below are some typical oscilloscope shots taken from the board:

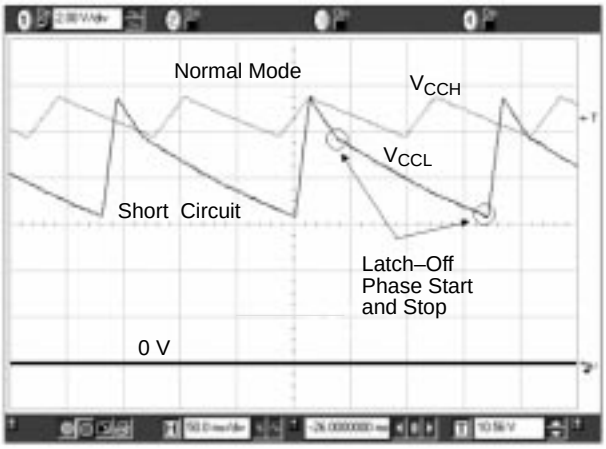

Figure 11b. The NCP1200 DSS behavior in normal and short circuit conditions.

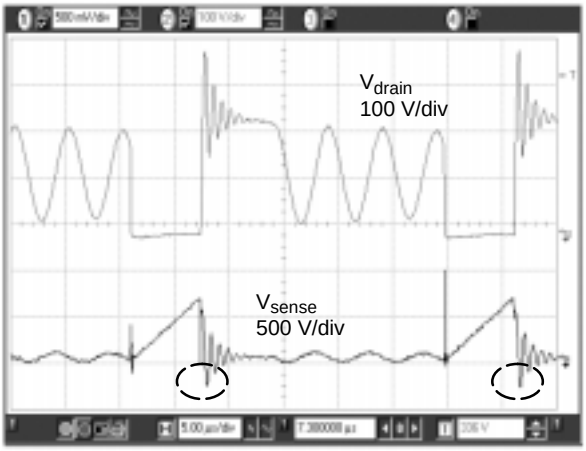

Figure 11c. Typical 3 W operation that can be compared to Figure 10b.

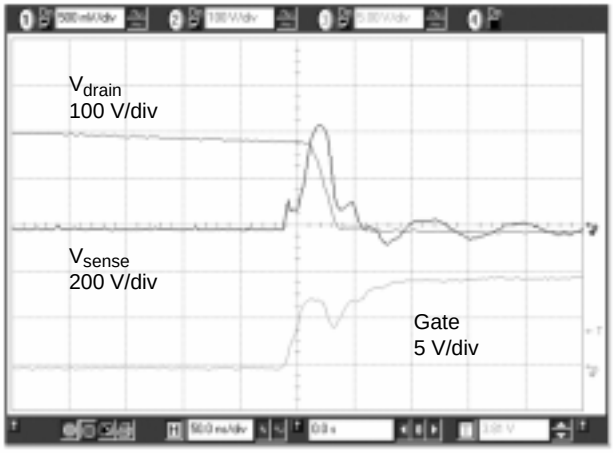

Figure 11c. This shot confirms our turn–on 45 ns calculation and shows the absence of immediate drain current. The capacitive peak is blanked with the NCP1200 LEB.

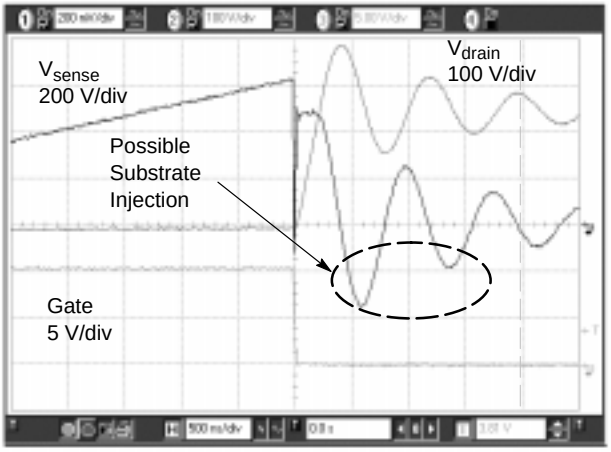

Figure 11d. As predicted by the calculations, the turn–off time is extremely fast and does not engender losses. The switch is immediately closed and the current is capacitive. This plot can be compared to Figure 10c.

Figure 11d represents the turn–off stage when the snubber capacitor is wired between drain and source. When the leakage starts to ring, the induced dV/dt forces a capacitive current to circulate inside the MOSFET Coss and the snubber. This current unfortunately creates a negative ringing over Rsense and can potentially inject into the NCP1200 substrate. This situation is highly undesirable as the injected electrons can go anywhere, possibly engendering an erratic behavior of the IC. To prevent this situation, simply wire the snubber between the drain and ground, as indicated by Figure 6b and confirmed by Figure 11e. In application where you do not install any snubber, the problem should not appear.

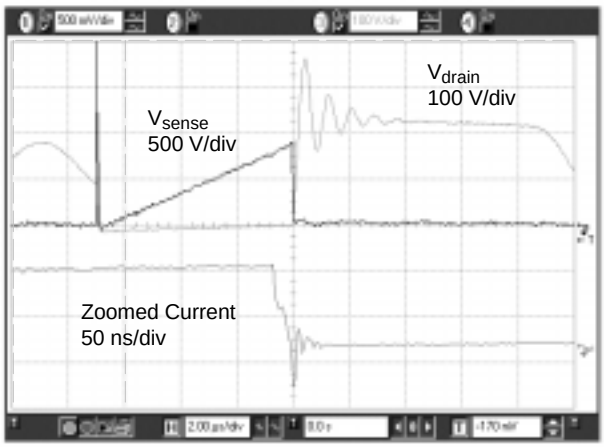

Figure 11e. Wiring the snubber between drain and source avoids the substrate injection.

However, in some higher power applications, the case can arise where the spike is present without the snubber in place. In that later case, we advise to wire a small low–pass RC filter between the sense resistor and pin 3. Typical values are R = 1 kΩ C = 220 pF. Another options lies in connecting a Schottky diode between pin 3 and ground (cathode to pin 3).

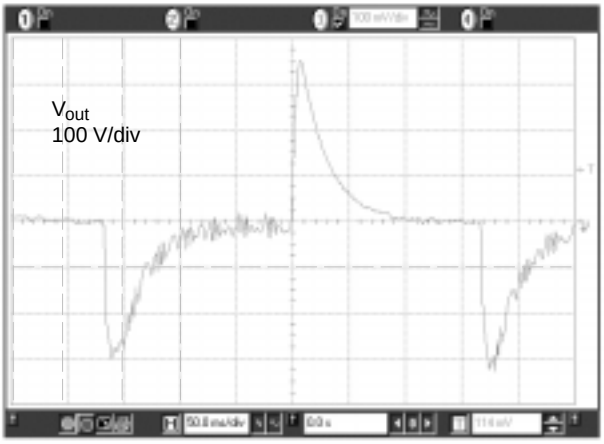

Figure 11f. Demoboard transient response when banged from 10 mA to 800 mA.

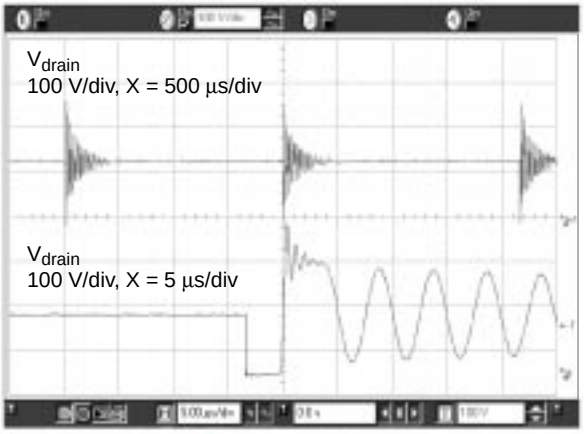

Figure 11g. Standby operation, upper curve is Vdrain with X = 500 μs/div.

Depending on the layout, the FB pin can pick–up some noise which leads to spurious oscillations. To cure this problem, wire a 1 nF capacitor between pins 2 and 4.

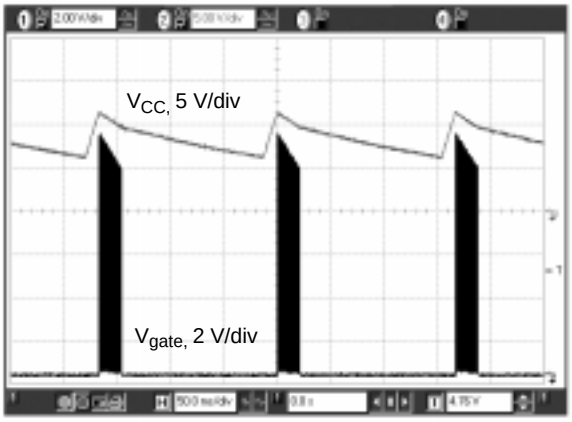

Figure 11h. Typical Operating Curves in Short–Circuit Conditions

Typical measurements on the 3.5 W AC/DC adapter:

DC Input Level	Input Power	Output Power	η
120	134 mW	0	–
120	732 mW	480 mW	65%
120	1.44 W	1.0 W	69.5%
120	4.08 W	3.3 W	80.6%
325	339 mW	0	–
325	1.06 W	480 mW	45%
325	1.84 W	1.0 W	54%
325	4.3 W	3.11 W	72%

At low line, the DSS contribution is low at about 100 mW. It represents nearly all the power consumption and does not significantly affect the efficiency. At higher line levels, because of the DSS constant current nature, its contribution increases and degrades the efficiency at weak output power levels. To greatly improve these numbers, you can apply Figure 2 trick or work with an auxiliary winding (Figure 3): it will save more than 200 mW. With the prototype under test, we measure an overload activation at a power level of 7 W.

Battery Charger Configuration

Certain applications require the control of the output current, e.g. battery chargers. To precisely monitor the output current flow, dedicated circuits already exist from ON Semiconductor such as the MC33341. This IC has been tailored to directly drive an SMPS optocoupler and turn your SMPS into a precise Constant Voltage–Constant Current (CV–CC) generator. For less precise requirements, Figure 12a depicts a configuration where a second loop has been added. This loop operates in parallel with the standard zener one and deviates the LED bias current to regulate the current (Q1 active). Of course, the current reference being the transistor Vbe, it is likely to change over temperature (–2.2 mV/°C)… However, this design can be selected where ± 10% current precision is enough. More precise designs can be made through a TL431 for better output precisions but also by combining the bipolar with a CTP to compensate the current loop temperature drift.

Figure 12a shows a typical configuration plugged into our NCP1200 averaged SPICE model. Thanks to this model, we can test for the open–loop stability by drawing a Bode plot of both loops (I or V) and transient test the validity of the CV–CC behavior:

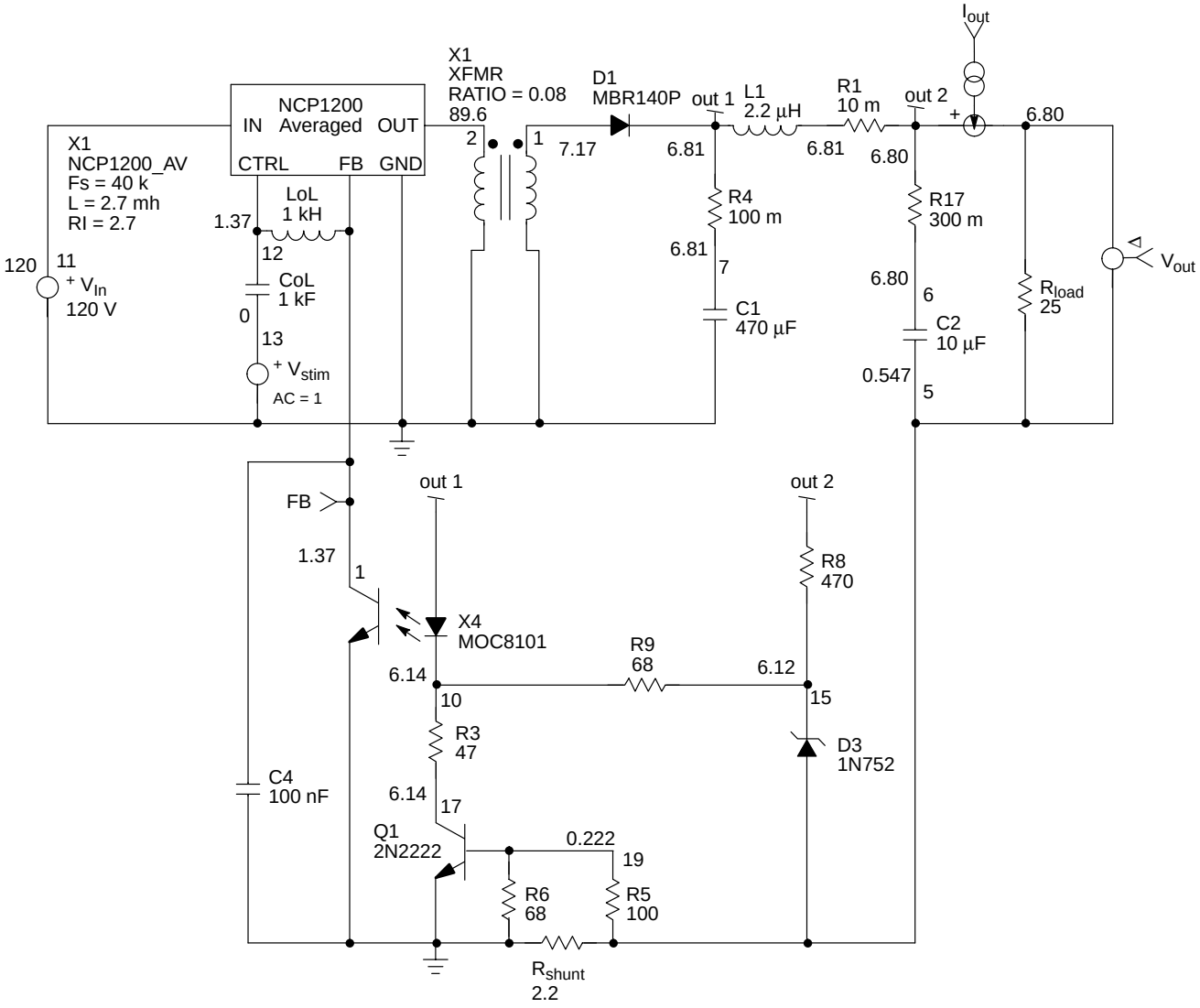

Figure 12a. An Averaged SPICE Simulation in a Battery Charger Application

By reflecting the bias points to the schematic, the simulator (IsSpice4 in this example), indicates which loop is active: the voltage loop in this case (Q1's Vbe is 203 mV and is off). By sweeping Vstim, Figure 12b and 12c reveal the Bode plot of the whole configuration where both loops have been represented.

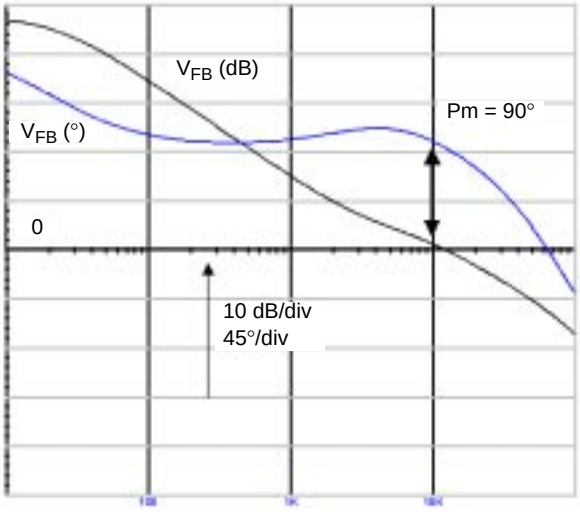

Figure 12b. The voltage sweep does not reveal any problem with a 90° PM...

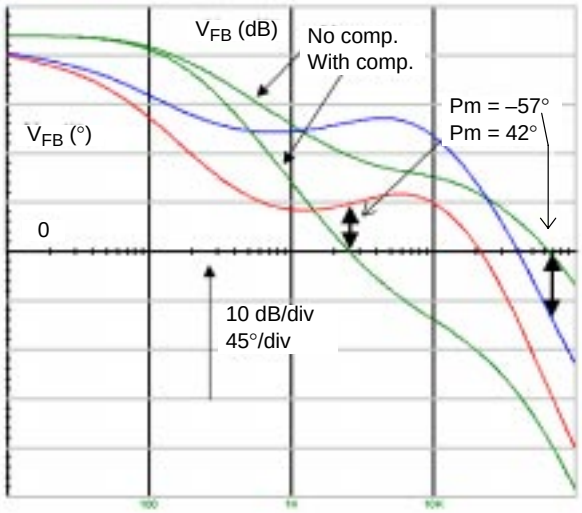

Figure 12c. However, the current loop is unstable with a large bandwidth.

As the below curves show, there is no problem when the voltage loop operates. The high gain finds one of its root in the NCP1200 internal collector resistance which equals 6.4 kΩ. But as you can see, it offers a good theoretical bandwidth associated with a safe phase margin. If we now activate the current loop, Figure 12c details a strong instability because of the bipolar presence. To cure this problem in the simplest manner, we can wire a 100 nF capacitor between FB and ground to roll–off the gain at lower frequencies. Updated Bode plots confirm the stability gained by this capacitor addition. This instability was observed on the evaluation board and also eradicated by the 100 nF capacitor.

By decreasing LoL and CoL elements down to 1p, we actually close the feedback loop. By sweeping the output load through a variable resistor, we plot the CC–CV curve as shown by Figure 12d.

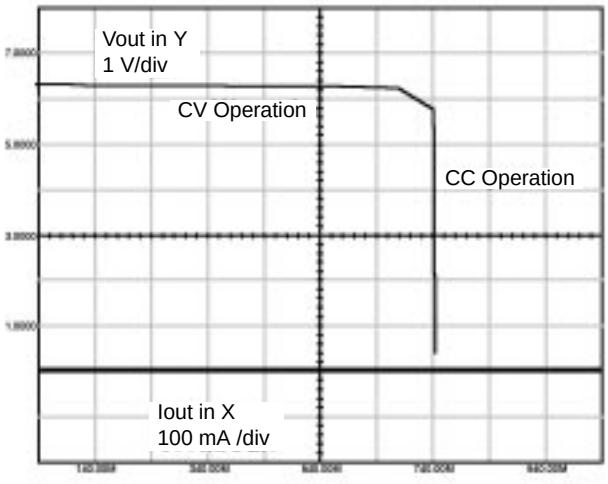

Figure 12d. The simulated CC–CV output shape as delivered by Figure 12a.

Please note that these average simulation circuits work with the demo versions of INTUSOFT, OrCAD and Spectrum–Software.

The complete battery charger schematic appears on Figure 13 and is available as another NCP1200 demoboard.

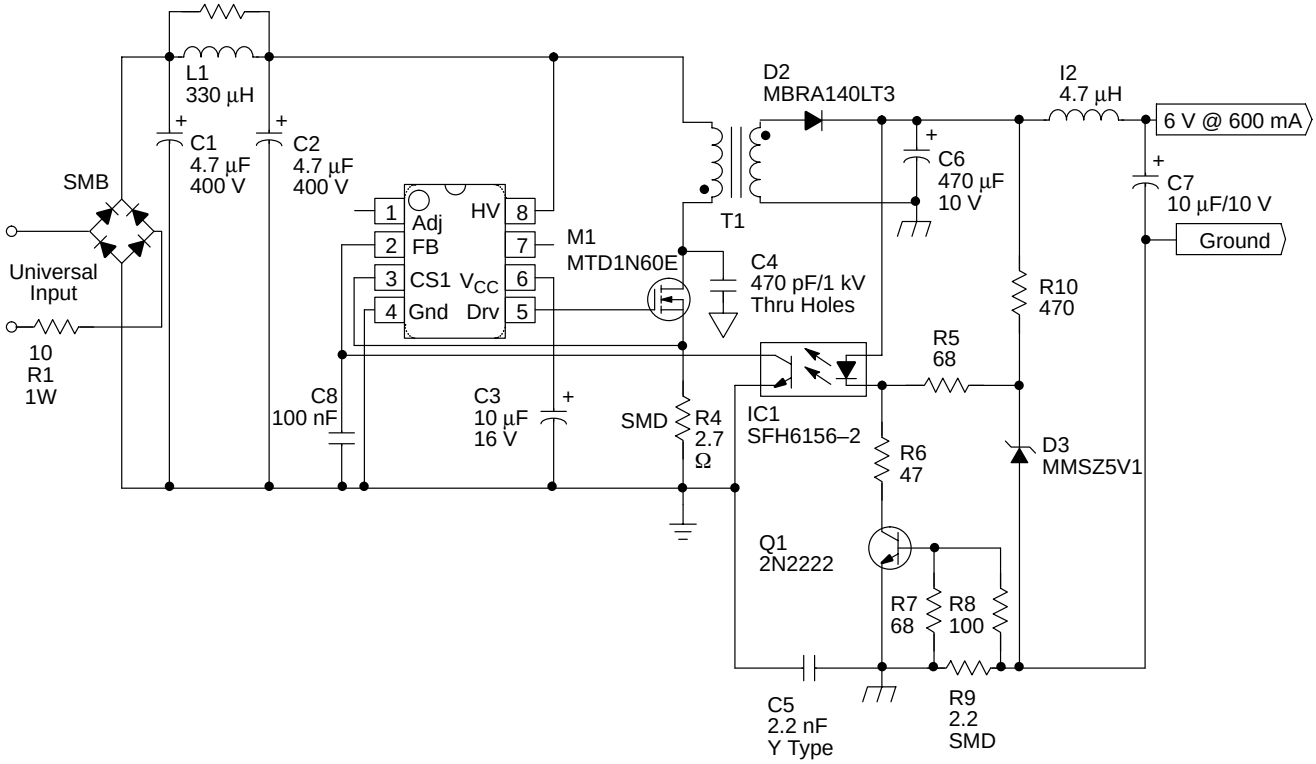

Figure 12e. The Complete Battery Charger Demonstration Board

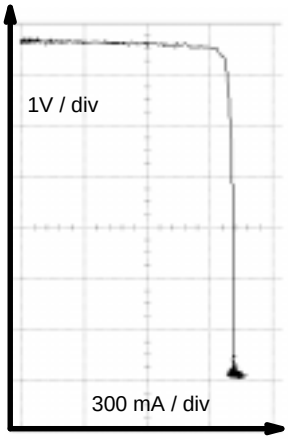

Figure 12f. The Resulting I–V Curve of the NCP1200 Charger Demoboard

Figure 12f depicts the resulting CV–CC obtained when sweeping the charger's output through a MOSFET and displaying the values with an X–Y oscilloscope.

Precise Secondary Regulation

Any TL431–based regulation scheme can be employed with NCP1200. Figure 13 gives in example the feedback section only when using a TL431 reference voltage. The TL431 is usually compensated by wiring a capacitor between the resistor bridge middle–point and the cathode. Different scheme will allow various bandwidth and response times. In that case, the averaged NCP1200 SPICE model appears as an invaluable tool to help you to place poles/zeroes at the correct location.

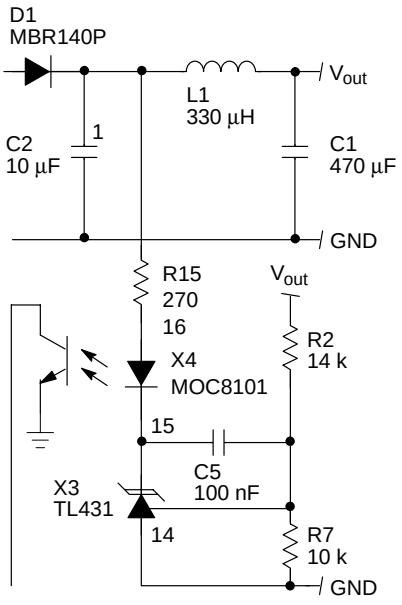

Figure 13. A Precise Regulation Option using a TL431 Reference Voltage

Primary Regulation Option

Despite the lack of internal error amplifier, two kind of primary regulation options can be implemented: one in which the short–circuit works as usual and another one where this option is permanently invalidated. Both options are depicted in Figure 13a and 13b sketches. To avoid classical peak rectification, a light load e.g. 470 Ω can be connected to load the auxiliary supply. Auxiliary and main power winding ratio should be adjusted to match the desired output voltage.

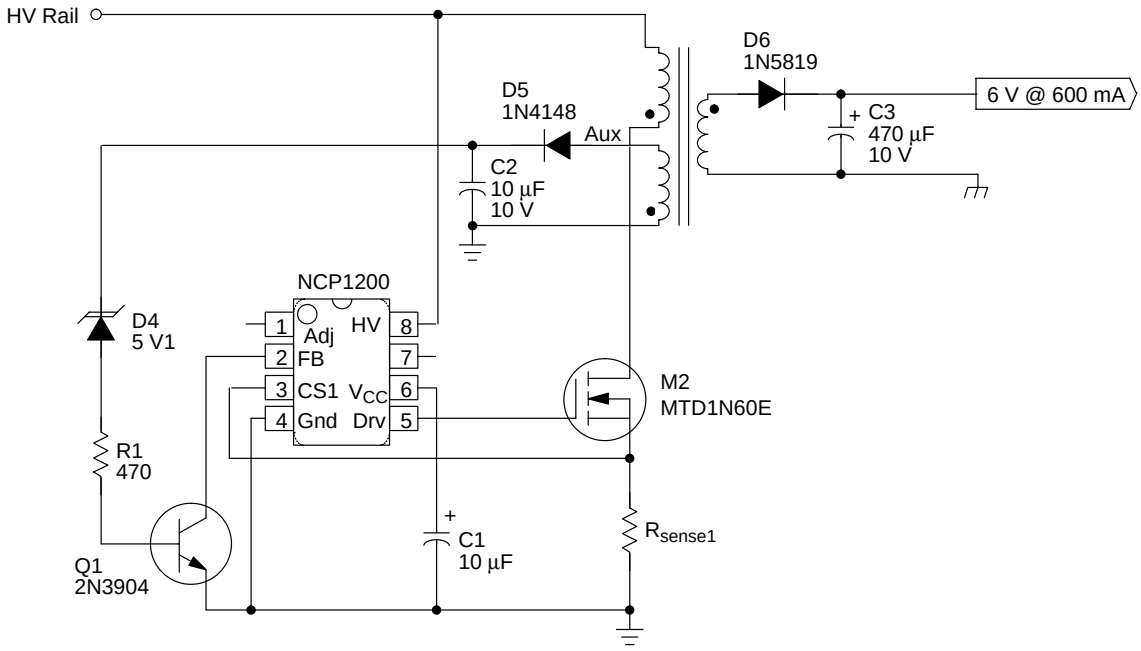

Figure 13a. A primary regulation possibility where the short–circuit protection still operates.

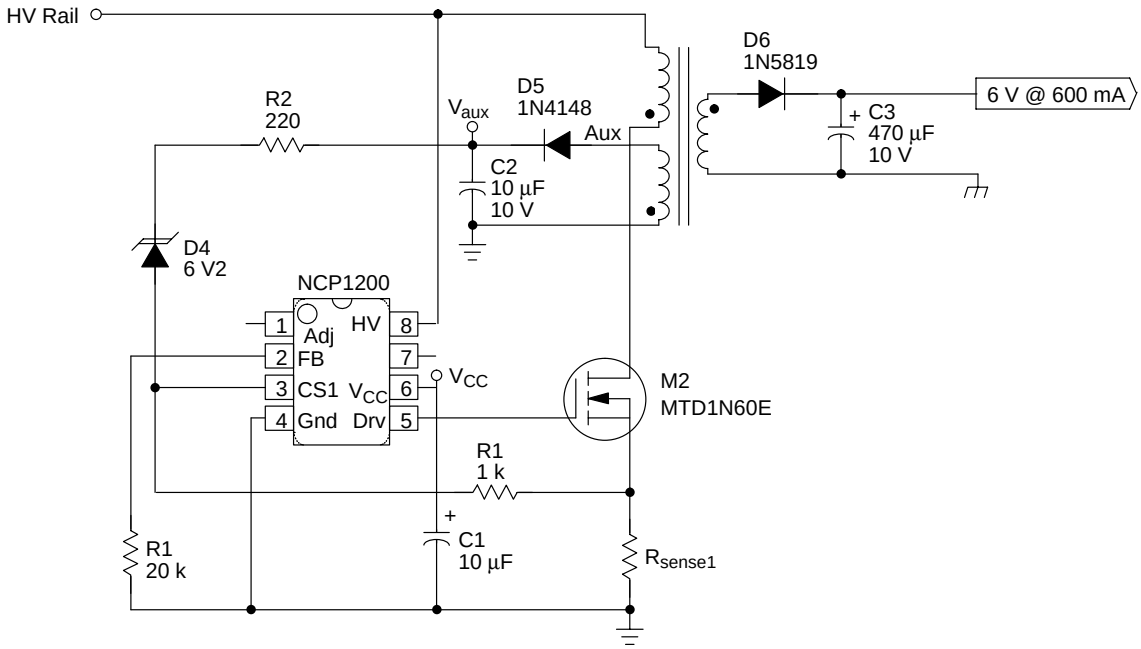

Figure 13b. Another primary regulation possibility where the short–circuit protection no longer operates.

Transformer Availability

T1 transformer for the depicted circuits (charger and AC adaptor) is immediately available from several manufacturers whose details are given below. The 2.7 mH E16 version corresponds to a 3.5 W charger operating with an NCP1200P40 (40 kHz) while the 1.8 mH version should be used for a 5 W NCP1200P60 version (60 kHz).

Eldor Corporation Headquarter
Via Plinio 10,
22030 Orsenigo
(Como) Italia
Tel.: +39–031–636 111
Fax : +39–031–636 280
Email: eldor@eldor.it
www.eldor.it

ref. 1: 2262.0058C: 3.5 W version
(Lp = 2.9 mH, Lleak = 80 μH, E16)
ref. 2: 2262.0059A: 5 W version
(Lp = 1.6 mH, Lleak = 45 μH, E16)

EGSTON GesmbH
Grafenbergerstraβe 37
3730 Eggenburg
Austria
Tel.: +43 (2984) 2226–0
Fax : +43 (2984) 2226–61
Email: info@egston.com
http://www.egston.com/english/index.htm

ref. 1: F0095001: 3.5 W version
(Lp = 2.7 mH, Lleak = 30 μH, sandwich configuration, E16)

Atelier Special de Bobinage
125 cours Jean Jaures
38130 ECHIROLLES FRANCE
Tel.: 33 (0)4 76 23 02 24
Fax: 33 (0)4 76 22 64 89
Email: asb@wanadoo.fr

ref. 1: NCP1200–10 W–UM: 10 W for USB
(Lp = 1.8 mH, 60 kHz, 1:0.1, RM8 pot core)

Coilcraft
1102 Silver Lake Road
Cary, Illinois 60013 USA
Tel: (847) 639–6400
Fax: (847) 639–1469
Email: info@coilcraft.com
http://www.coilcraft.com

ref. 1: Y8844–A: 3.5 W version
(Lp = 2.9 mH, Lleak = 65 μH, E16)
ref. 2: Y8848–A: 10 W version
(Lp = 1.8 mH, Lleak = 45 μH, 1:01, E core)

SPICE Editors

As mentioned in the text, NCP1200 ready–to–use SPICE platforms are available to download from the ON Semiconductor Web site in the following formats: OrCAD's PSpice, INTUSOFT's IsSpice and Spectrum–Software's μCap. You will find both transient and AC analysis templates as described by Figures 10a and 12a. Some of these examples can work on the editor's demo versions, some will require the full version to operate. Editors demo versions can be downloaded at the following locations: www.orcad.com (PSpice), www.intusoft.com (IsSpice) and www.spectrum–soft.com (μCap).

AND8029/D

Ramp Compensation for the NCP1200

Prepared by: Christophe Basso
ON Semiconductor

ON Semiconductor

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

As any current–mode controllers, the NCP1200 can be subject to subharmonic oscillations. Oscillations take place when the Switch–Mode Power Supply (SMPS) operates in Continuous Conduction Mode (CCM) together with a duty–cycle near or greater than 50%. For Discontinuous Conduction Mode (DCM) designs, this normally does not happen. However, at the lowest line levels and when the SMPS is pushed to its upper output power capability, CCM can engender these oscillations within the current loop. This application note details how to properly cure this problem by injecting the correct amount of ramp compensation.

Origin of the Problem

A current–mode power supply is a two–loop system: one loop controls the inductor peak current while the other monitors the output voltage. The current loop is actually embedded into the voltage loop which fixes the final current setpoint. In CCM operation, the action of the current loop can be compared to a sample and hold device. This sampling action creates a pair of RHP zeroes in the current loop which are responsible for the boost in gain at $F_{switching}/2$ but also stress the phase lag at this point. If the gain margin is too low at this frequency, any perturbation in the current will make the system unstable since, as we said, both voltage and current loops are embedded. You can fight the problem by providing the converter with an external compensation ramp. This ramp will oppose the duty cycle action by lowering the current–loop DC gain, correspondingly increasing the phase margin at $F_{switching}/2$, finally damping the high Q poles in the $V_{out}/V_{control}$ transfer function. As other benefits of ramp compensation, Ray Ridley [1] confirmed that an external ramp whose slope is equal to 50% ($m_c = 1.5$) of the inductor downslope could nullify the audio susceptibility in a BUCK converter, as already calculated by Holland [2]. As more external ramp is added, the low frequency pole ω_p moves to higher frequencies while the double poles will be split into two distinct poles. The first one will move towards lower frequencies until it joins and combines with the first low frequency pole at ω_p. At this point, the converter behaves as if it is operating in voltage mode.

Lowering the Peaking

A current mode controlled SMPS exhibits one low frequency pole, ω_p, and two poles which are located at $F_{switching}/2$. These poles move in relation to the duty cycle and the external compensation ramp, when present. The two high frequency poles present a Q that depends on the compensating ramp and the duty–cycle. Ridley demonstrated that the Q becomes infinite at D = 0.5 with no external ramp (mc = 1), confirming the inherent instability of a CCM current–mode SMPS operating at a duty cycle greater than 0.5. Below stands the definition of this quality coefficient:

$Q - \frac{1}{\mu \cdot (mc \cdot D + 0.5)}$ where $m_c = 1 + S_e/S_n$. S_e is the external ramp slope, S_n is the inductor on–time slope and $D' = 1 - D$.

For designers, once the system's Q has been determined, they should look for the amount of ramp compensation that will make this number equal to 1: $mc - \frac{1}{\mu} \times 0.5\sqrt{\frac{1}{D}}$.

How to Create a Ramp?

On the NCP1200, you do not have access to any oscillator sawtooth. However, you can easily charge a capacitor when the gate drive is high, and immediately discharge it when the MOSFET switches off. Figure 1a shows how to simply generate a sawtooth from the gate drive:

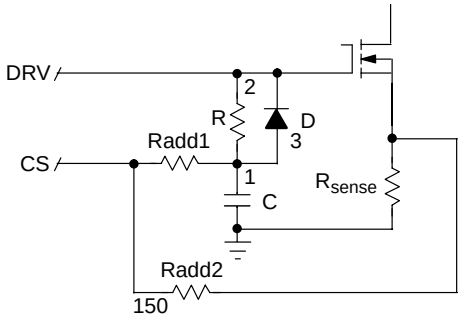

Figure 1a

A very simple way to generate a ramp from a square wave signal.

Calculating the RC component values is a rather easy task. By drawing the smallest current from the drive to avoid increasing the standby power, R shall be of high value. If this is the case, you can consider this system as a current generator. By applying $Vc \cdot C - i \cdot t$, you calculate R and C. Suppose we want to create a ramp that goes up to 5.0 V when a 60 kHz NCP1200 is operating at 50% duty–cycle. The ON time is therefore $\frac{1}{2 \cdot 60\ k} - 8.3\ \Omega s$. In order to not bothering the NCP1200 operation, let's select a charging current of 250 µA. With a gate plateau of 11 V, this leads to a resistor of ≈11 V/250 µA = 44 kΩ. With a charging current of 250 µA, what capacitor do we need to generate a ramp that reaches 5.0 V in 8.33 µs? Well, $C - \frac{250\ \Omega \cdot 8.33\ \Omega}{5} - 416\ pF$. However, because the charging current varies during the ramping (we actually obtain an exponential), we will to reduce both elements to their next lower normalized values, e.g., 39 kΩ and 390 pF. If we feed our SPICE simulator with these values, Figure 1b and 1c confirms the calculations:

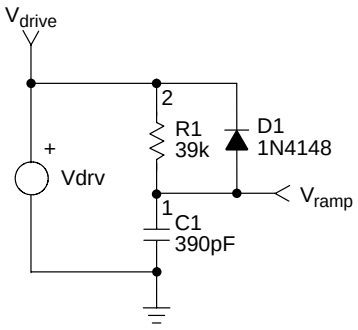

Figure 1b

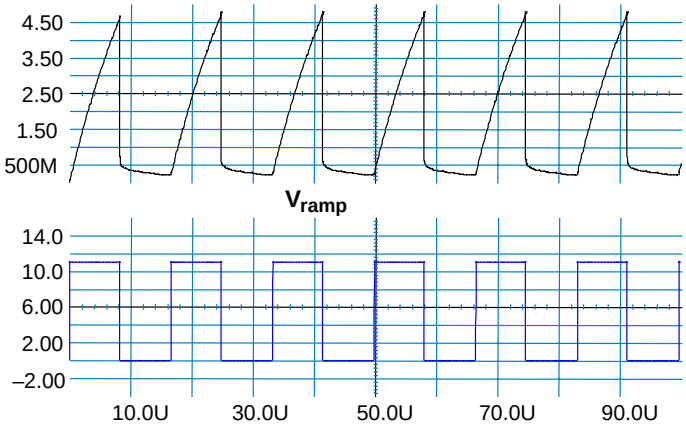

Figure 1c

A simple simulation schematic confirms the calculations: the capacitor voltage ramps up from a few hundred of mV up to nearly 5.0 V.

By ramping from 0.6 V to 4.5 V in 8.3 µs, we have created a signal exhibiting a slope of 468 mV/µs.

"What compensation level shall I inject?"

Let's suppose the following specs for our FLYBACK converter:

VHV_{DC} = 110 V
Fsw = 60 kHz
Lp = 1.8 mH
η = 80%
N = Np:Ns = 0.1
$Pout_{max}$ = 15 W

To calculate the operating duty–cycle D, we need to compute the peak current authorizing a 15 W output power flow from the 1.8 mH primary inductance: $Pin - \frac{1}{2} \cdot Lp \cdot Ip? \cdot Fsw$. From our specs, we know that Pin = 15/08 = 18.8 W. At the boundary between DCM and CCM, the peak current is evaluated to: $Ip - \frac{\overline{2 \cdot Pin}}{Lp \cdot Fsw} - 590\ mA$. To reach this value, we need to apply VHV_{DC} over Lp during: $Ip \cdot \frac{Lp}{VHV_{DC}} - 9.6\ \Omega s$. Compared to a 60 kHz switching frequency, it corresponds to a 58% duty–cycle or D = 0.58.

The external ramp injection will keep Q below 1. To adhere to this requirement, we must inject a compensating ramp mc equal to $\frac{1}{\pi} \times 0.5\sqrt{\frac{1}{D}} - 1.9$. By applying mc definition, we can deduct the final amount of external ramp we must inject: $mc - 1 \times \frac{Se}{Sn}$ or $Se - (mc + 1) \cdot Sn$. In a FLYBACK, the ON slope Sn is given by the rectified DC rail applied over the primary inductance Lp: $Sn - \frac{VHV_{DC}}{Lp}$. With Lp = 1.8 mH, Rsense = 1.5 Ω and the lowest main equals 110 V, then Sn = 91.5 mV/µs once reflected in volts over Rsense. To get the final level of ramp compensation, let's compute Se by: $Se - (mc + 1) \cdot Sn$ or 82 mV/µs. To obtain this ramp from our ramping generator, we must create a division ratio of 0.082/468 or 175 m. If we select a 10 kΩ resistor to convey the current sense information, then the ramp resistor is calculated using: $\frac{10\ k + 0.175 \cdot 10\ k}{0.175}$ or 47 kΔ in this example.

Simulation of the Converter

To check our calculation, we can use the NCP1200 SPICE model. Figure 2a portrays the application schematic for this converter with INTUSOFT's IsSpice4 model version:

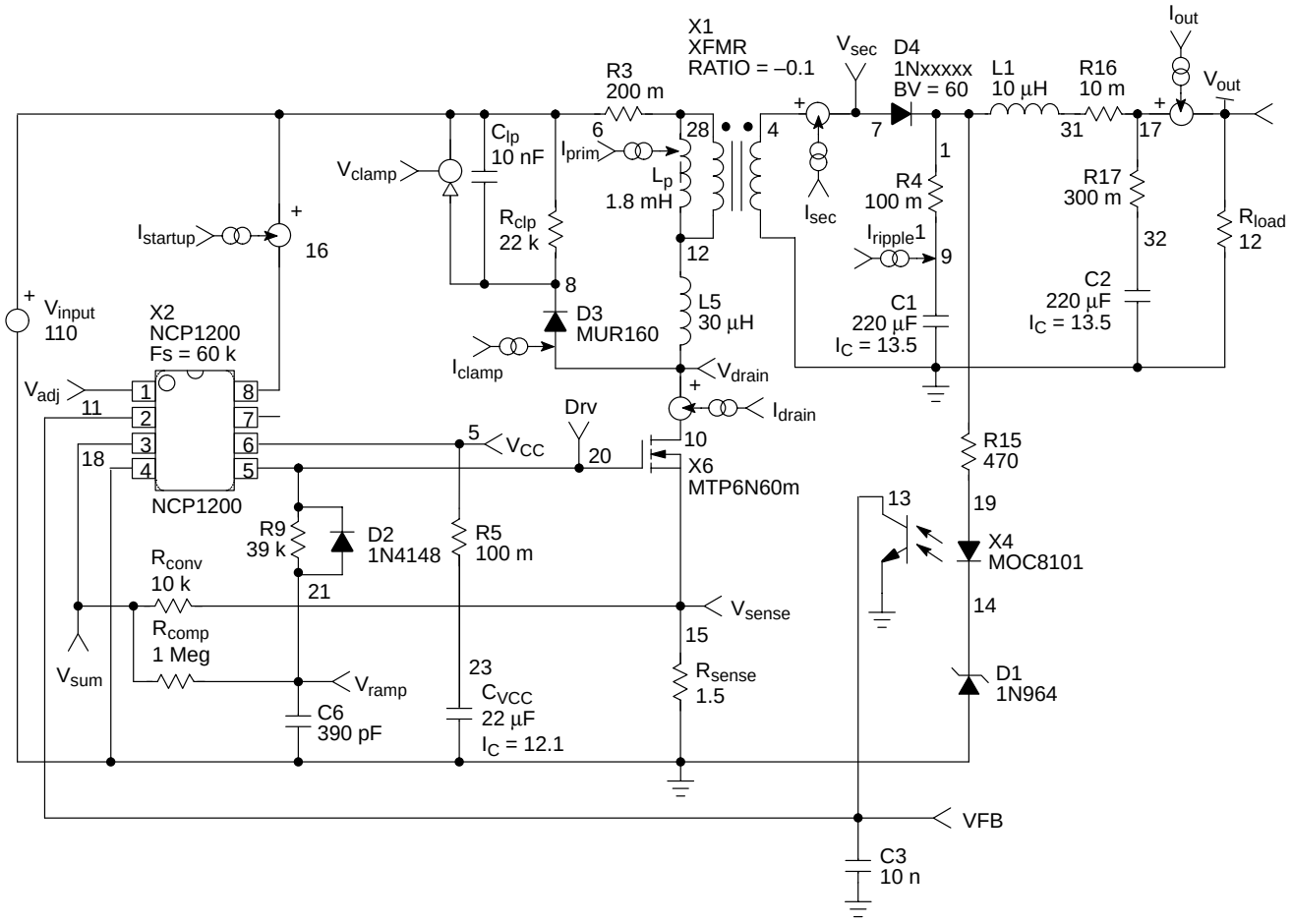

Figure 2a

The current–mode SMPS built with the NCP1200 SPICE model.

The system enters CCM for a load of 12 Ω and subharmonic oscillations take place, as shown by Figure 2b. Measurements on the board confirm the presence of these unwanted oscillations (Figure 2c). Rcomp was kept to a high value to suppress any compensating action.

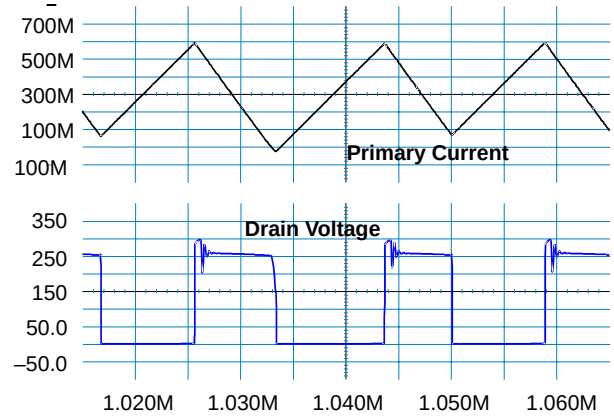

Figure 2b

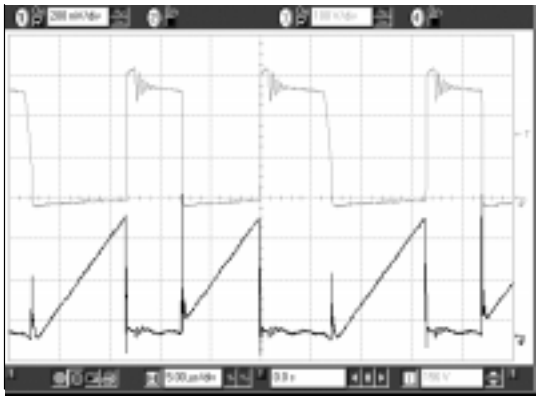

Figure 2c

Oscillations take place when entering CCM with a duty–cycle greater than 50% as confirmed by both models and measurements.

Let's now diminish Rcomp to 47 kΩ as previously calculated and run a new simulation. Results are depicted by Figure 2d and confirmed by Figure 2e:

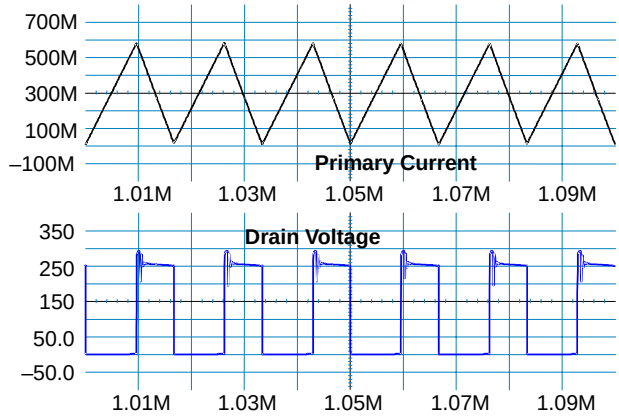

Figure 2d

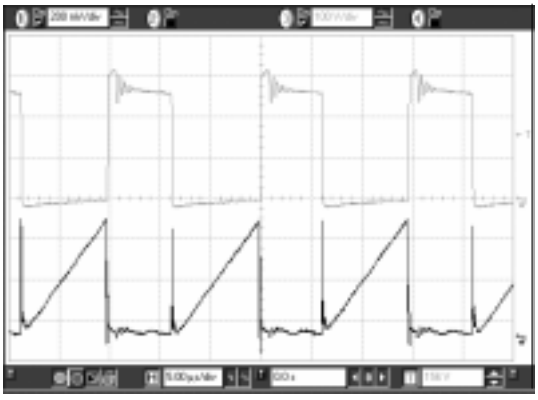

Figure 2e

The right amount of ramp compensation stabilizes the converter (2d simulated, 2c measured).

The previous default has disappeared and the converter is stabilized. However, the designer shall keep in mind that injecting a compensation ramp diminishes the current loop gain. This has the same effect as raising Rsense on the small–signal point of view. As a result, the controller grows its operating feedback voltage V_{FB} (that sets Ip) to impose the same peak current. If before compensation V_{FB} was already close to the maximum limit, the ramp injection will make it raise and the possibility exists that the NCP1200 goes into short–circuit protection ($V_{FB} \approx 4.1$ V).

We deliberately selected a rather high value for the ramp generator resistor in order to not load the NCP1200 (otherwise the standby power can be degraded). As a consequence, the summing resistor Rcomp cannot be too low to prevent from disturbing the ramp generator. In a noisy environment, the electrical paths conveying these signals to the NCP1200 pins shall be kept as short as possible to avoid undesirable peaking. In case of troubles, the solutions consists in lowering the ramp generator's output impedance and re–iterating the other elements.

References

1. R. B. RIDLEY, "A new small–signal model for current–mode control'', PhD. dissertation, Virginia Polytechnic Institute and State University, 1990 (e–mail : RRIDLEY@AOL.COM). This document can also be ordered from Ray Ridley's homepage: http://www.ridleyengineering.com/index.html
2. HOLLAND, "Modelling, Analysis and Compensation of the Current Mode Converter", Powercon 11, 1984 Record, Paper H–2.

AND8032/D

Conducted EMI Filter Design for the NCP1200

Prepared by: Christophe Basso
ON Semiconductor

ON Semiconductor

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

If the NCP1200 easily lends itself to designing Switch–Mode Power Supplies (SMPS) in a snap–shot, its presence among other equipments necessitates an adequate ElectroMagnetic Interference (EMI) input filter. Fortunately, friendly methods such as SPICE exist to isolate the guilty harmonics and make them stay below the limit. This application note briefly describes the mechanism of conducted EMI noise generation and depicts a way to circumvent it.

The Bulk Capacitor is a Natural Shield

As Figure 1a depicts, an SMPS is supplied by a network made of a diode bridge rectifier and a bulk capacitor. Every time the mains peak voltage exceeds the bulk capacitor level, two diodes of the input bridge conducts for a period of time given by the DC rail ripple: the larger the ripple, the longer the conduction time (≈ 1–3 ms). As a result, Cbulk is recharged at a rather low rate (every 10 ms for a 50 Hz mains) while the SMPS load draws pulses at its high switching frequency. During the refueling by the diodes, Cbulk stores energy and delivers this energy during the time the diodes are off (high series resistance, but still weakly capacitive).

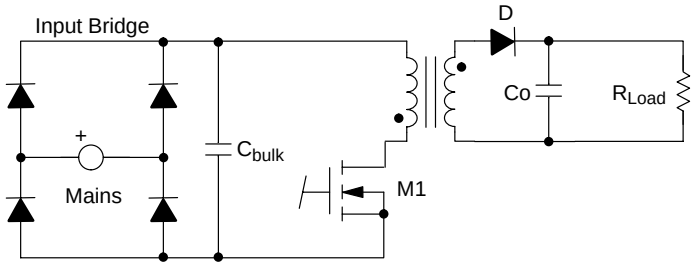

Figure 1a. A typical component arrangement for an SMPS (here a FLYBACK).

The current flowing through Cbulk is thus the ON time drain current for a FLYBACK converter. Cbulk is unfortunately not a perfect element and Figure 1a can be refined into Figure 1b where parasitic elements appear: the Equivalent Series Inductance (ESL) and the Equivalent Series Resistor (ESR).

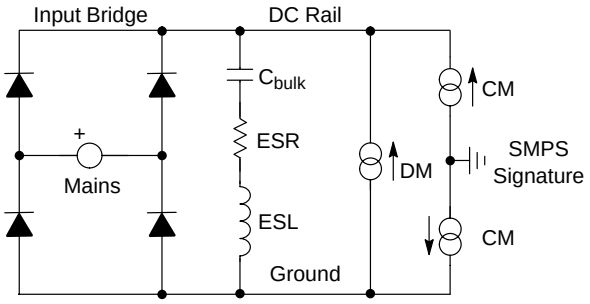

Figure 1b. A more realistic way to represent the EMI generation mechanism.

These technology dependent elements work together to prevent the capacitor from being a true capacitor. At low frequency, the impedance is capacitive (Z goes down when F goes up, C dominates), at medium frequency the impedance is resistive (Z stays flat, ESR dominates) and at higher frequencies, Z goes up because ESL dominates: this is depicted by the well know impedance versus frequency plot as shown by Figure 1c (a 400 V 33 μF snap–in capacitor, Y axis in dBΩ). In SPICE, this is rather easy to model, as portrayed by Figure 1d.

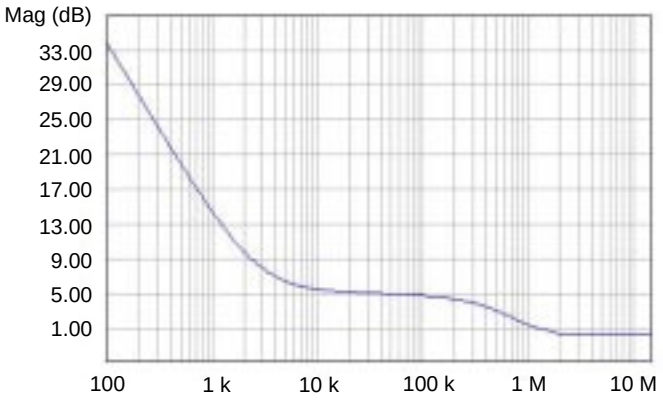

Figure 1c

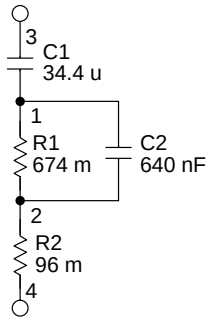

Figure 1d

A typical impedance plot of a 33 μF 400 V capacitor . . . and its equivalent SPICE model showing the resonating elements.

Differential and Common Mode

As you can see on Figure 1b, there are three current generators: one is for the differential mode (DM) currents that flow 180° out of phase on each branch while the remaining two generators depict the common mode (CM) current flowing in phase on both the DC rail and ground. The DM level is caused by the weakness of Cbulk to perform its filtering function over a large frequency range due to its friends ESL and ESR. The CM noise finds one of its roots in capacitive current displacements induced by high dV/dt over a key node: the MOSFET drain. This quickly varying voltage present on this pin pushes currents into capacitive elements exhibited by the transformer (disposed between all terminals), the MOSFET (Coss or an additional snubber) and the various capacitive leaks. Instead of coming back to drain through Cbulk, they continue to transit via the Ground and the DC rail and come back to the drain after exciting the measurement network (a LISN, see its definition below). DM currents usually cause troubles in the low frequency range of interest while CM currents bother the designers in the remaining higher portion of the spectrum. As you can read, it is of importance to be able to identify who is hurting the measurement the most in order to take the adequate solution: CM and DM cures are not the same. Finally, DM disturbances are rather easy to predict, to the opposite of CM currents which depend on various stray paths (copper traces position, stray capacitance etc.) and are extremely difficult to estimate. Furthermore, because of the unsymmetrical nature of stray elements, combinations of currents can lead to an unequilibrated noise distribution over Live and Neutral . . .

Measuring the Noise

Standards have been established to fix a limit below which your SMPS will not disturb the surrounding equipment sharing the same line or outlet (e.g. CISPR22, FCC15 etc.). However, since we deal with circulating currents, the reference impedance used to measure their action takes on importance: the mains impedance in ON Semiconductor labs is not quite the same as in your building for instance . . . As a matter of fact, international standards have defined a reference impedance on which the measurements will be made. This impedance is guaranteed by a Line Impedance Stabilization Network (LISN) and precisely defined by CISPR16 document. Figure 2 portrays how this device is made. The LISN offers a 50 Ω impedance over the frequency of interest (e.g. 150 kHz–30 MHz for CISPR22) and shields the measurement against unwanted incoming noises. Please note that the high values of some capacitors connected between Live and Earth require the adjunction of an isolating transformer between your mains and the LISN.

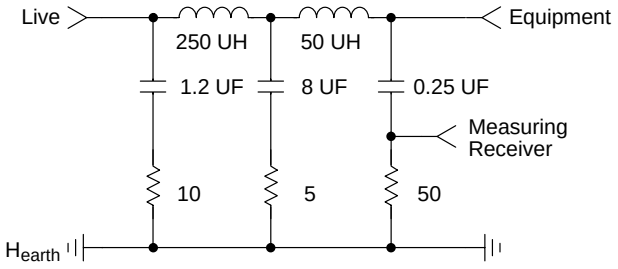

Figure 2. CISPR16 Network (Duplicated for the other line(s))

Fighting Against Conducted EMI

As we said, DM solutions differ from CM solutions. However, some parasitic elements can this time play in our favor . . . DM will usually be combated using the component arrangement of Figure 3a while CM requires Figure 3b arrangement.

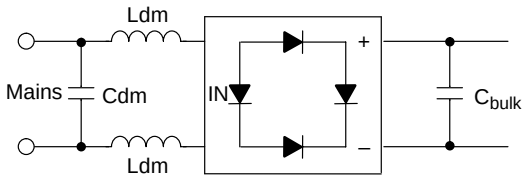

Figure 3a. By connecting two inductors (coupled or not), you attenuate the differential mode noise.

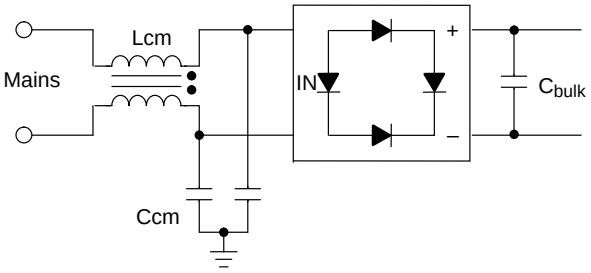

Figure 3b. Two coupled inductor (wounded in opposite directions) route the noise to earth via two Y–type capacitors.

CM inductors are usually of high values (≈ 1 mH to 50 mH) and strive to route the CM noise current through earth via Y–type capacitors. However, since earth leakage current is limited for security reasons, Y capacitors rarely exceed a few nano–farads thus requiring large CM inductors. Due to their winding technique (same directions), CM inductors do not offer any opposition to the DM mode (DM currents cancel the internal field). True DM inductors are either single component or coupled ones (values up to 1 mH). Fortunately, when these CM inductors are crossed by DM currents, the internal field is cancelled: the remaining inductances are the leakage inductances. If these leakage elements are of sufficient values, we can use them for filtering DM noise. Otherwise we need to add an external single coil for DM only (Figure 3c).

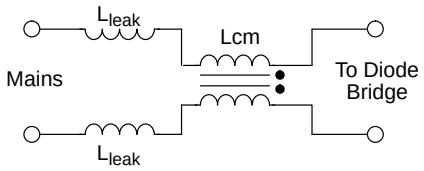

Figure 3c. When crossed by DM current, a CM inductor unveils two “leakage inductances”. Typical value would be 300 μH for a 27 mH type, but it really depends on the way the manufacturer winds the coils.

In some designs, there is no third earth conductor. In that case, you cannot wire two Y capacitors on the filter input. As we said, these Y capacitors are used to route most of the current displaced by the drain voltage back to the originator, a little crossing the LISN network but low enough to stay below the standard limit. The solution consists in providing this path through another Y capacitor but connected between primary and secondary grounds as shown by Figure 3d. Again, this capacitor cannot exceed a given value in order to keep the leakage current within the level imposed by the security standard (250 μA for all class II equipment).

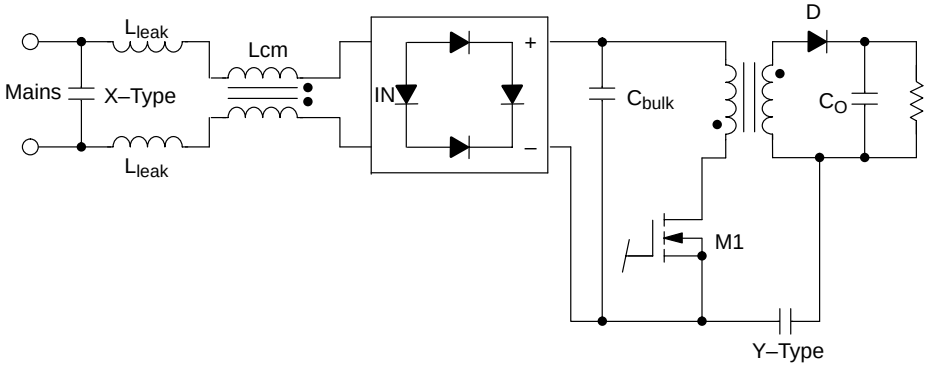

Figure 3d. A typical two–wire implementation when there is no earth conductor.

Evaluating the SMPS Signature

Before calculating any filter, we need to know the enemy: “what harmonic frequency hurts me the most?” On the paper, by hand or with a simulator, we can reasonably estimate the amount of DM noise the SMPS will deliver thanks to a good knowledge of the generation mechanism. CM will require a true measurement because many physical factors influence its content (PCB layout, stray capacitances etc.).

Depending on our topology and its operating mode (Continuous or Discontinuous Conduction Mode, CCM or DCM), we can draw the drain current signature. Figure 4a gives the typical plot for a DCM and a CCM FLYBACK converter.

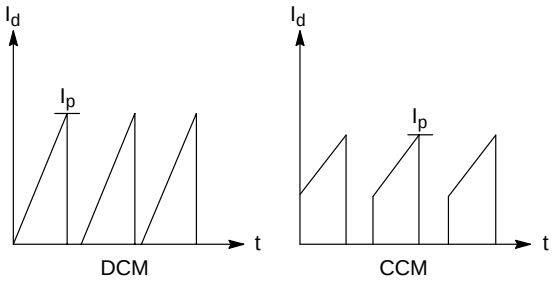

Figure 4a. Typical SMPS signature with two different operating modes.

In both cases, we need to evaluate the harmonic content through Fourier decomposition. In that area, SPICE can really help us through its Fast Fourier Transform (FFT) algorithm. Without entering into the details (see reference [1]), you can tailor the analysis bandwidth by adjusting the duration of your transient simulation:

.TRAN TSTEP TSTOP [TSART] [TMAX] [UIC] [optional]

.TRAN 100NS 801US 400US 50NS UIC
; 5.2MHz sweep range, 2.493kHz analysis BW, 4010 points (1)

.TRAN 24.44NS 500US 400US 12.22NS UIC
; 20.48MHz sweep range, 10kHz analysis BW, 4091 points (2)

.TRAN 489NS 2.1MS 100US 244.5NS UIC
; 1.024MHZ sweep range, 500Hz analysis BW, 4090 points (3)

CISPR22 specifies a 10 kHz analysis bandwidth above 150 kHz up to 30 MHz. This corresponds to the second .TRAN command line (2). But SPICE can even help more by predicting the exact operating point whatever input or output conditions. Figure 4b and 4c show a complete INTUSOFT’s IsSpice4 application using the NCP1200 together with a LISN built according to Figure 2. The complete SPICE netlist for the LISN is provided at the end of this document.

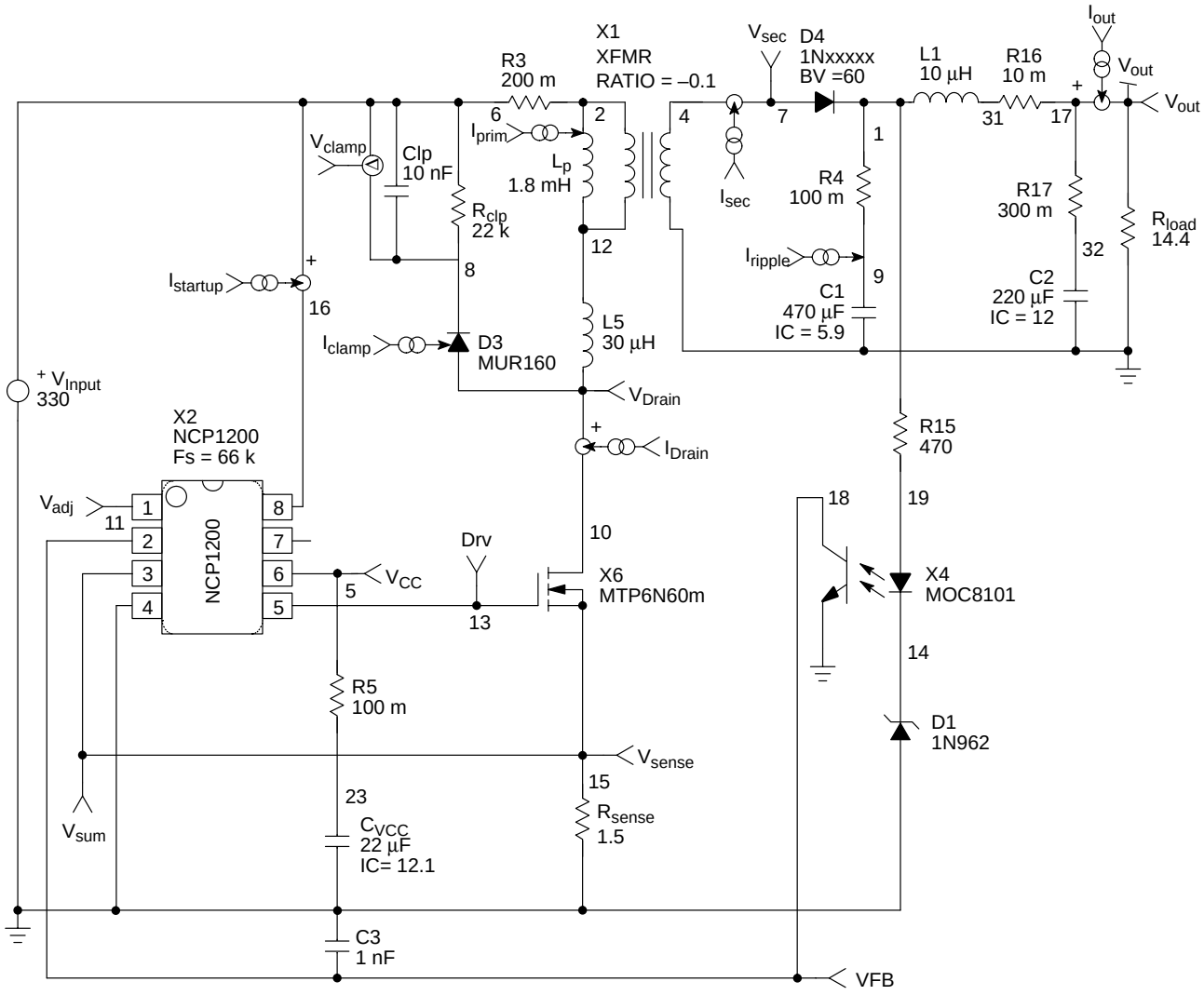

Figure 4b. A complete offline simulation template to unveil the desired operating point . . .

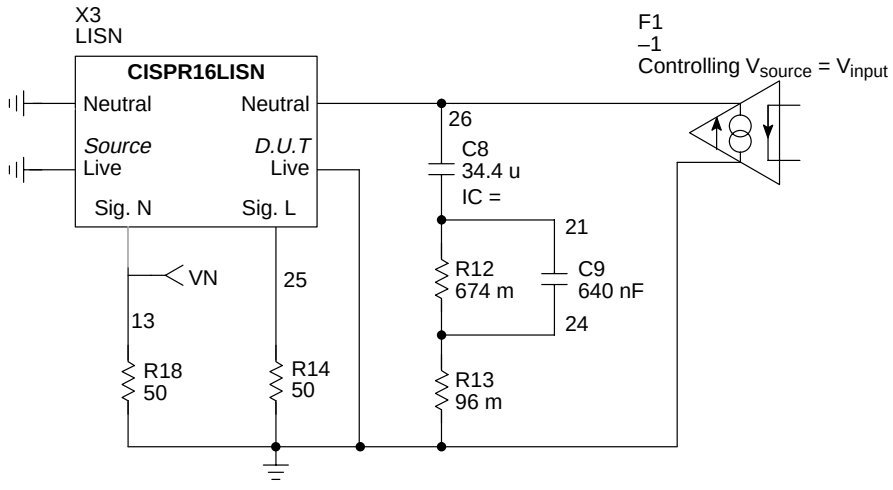

Figure 4c. . . . while the input EMI fixture lets you analyze the SPMS signature.

This application represents a 10 W universal input AC/DC wall adapter operating during given load/line conditions. To unmask the harmonics, F1 current–controlled current source routes the high frequency current pulses through the equivalent model of our 33 µF capacitor and develops the unwanted noise signal. This signal is confronted to the 50 Ω LISN network and a final reading is made on one of the outputs. For simulation reasons, we only use one input, the other one being loaded by a 50 Ω resistor.

Once the simulation is done, the data manipulation interface lets you run the FFT over VN node. After proper formatting, a graph such as Figure 4d is obtained where the vertical axis is displayed in dBµV (0 dBµV = 1 µV, 60 dBµV = 1 mV, etc.). To obtain dBµV, Log compress the Y axis and add 120. We purposely put the CISPR22 class quasi–peak limit to assess the needed amount of correction. Please keep in mind that a quasi–peak detector will give a smaller level compared to a peak detector as we naturally have with SPICE . . .

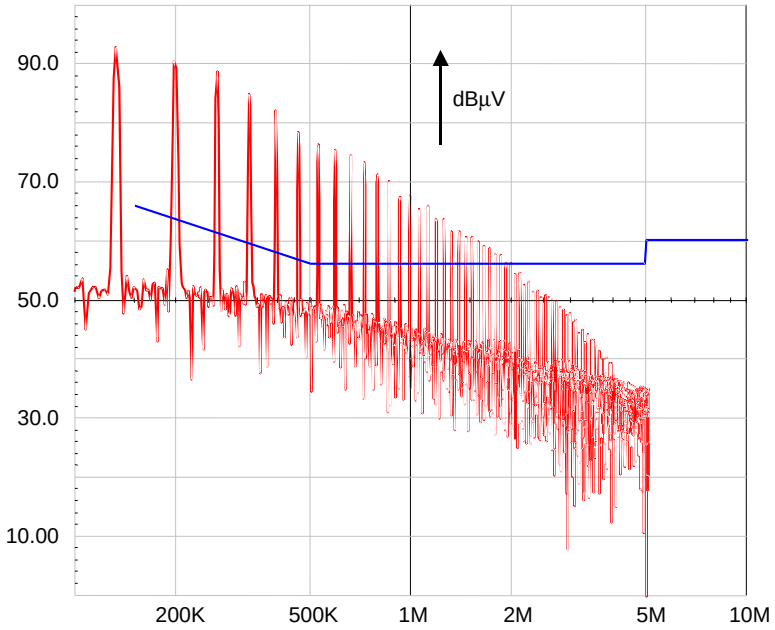

Figure 4d. Further to the simulation, an FFT plot is drawn by the graphical interface.

From this graph, we can clearly identify the value of the highest harmonic: 90 dBµV @ 190 kHz (below 150 kHz is out of the CISPR22 sweep range). To pass the limit, we shall reduce its contribution by more than 35 dB, taking into account a 10 dB safety margin:

1. Position the LC cutoff frequency fc at a given value to obtain the above rejection at 190 kHz : $-35 + -40 \cdot \mathrm{LOG}(190\,k \cdot fc)$ or $fc + \frac{190\,k}{10^{\frac{35}{40}}} + 25.3\,kHz$.

2. To avoid any resonance, the filter quality coefficient Q should be less than 1. By applying Q definition for a series LC filter, we obtain the following equation: $Q + \frac{\pi \cdot L}{Rs} = 1$ where Rs is the total series resistance and $\pi + \frac{1}{\sqrt{L \cdot C}}$. The resistance Rs will normally include all ohmic losses (ESR, inductor series resistance, load etc.) but since the 50 Ω load dominates, we will make Rs = 50 for our calculation.

3. Fix C to an arbitrary 100 nF value (for the first step) and calculate L by: $\frac{Rs}{2 \cdot \theta \cdot fc} + 315\,\mu H$. L should be in the range of 200–400 µH if you want to benefit from CM leakage inductances. If L is too big, select a bigger capacitor 220 nF, 330 nF or 470 nF.

4. Check the DC input impedance presented by the SMPS at the lowest line condition (η = 75%): Pin = Pout/0.75 = 13.3 W. With a 120 VDC input, $Rin + \frac{VinDC^2}{P} + 1082\,\Omega$.

5. Evaluate the LC filter characteristic impedance by: $Zo + \sqrt{\frac{L}{C}} + 56\,\Omega$ and be sure to follow Zmax << Rin to keep the stability. A plot example of the filter output impedance will reveal Zmax (the output impedance peaking) and endure that the above stability criterion is met. It can easily be done by sweeping the LC filter output terminal through a 1A AC source. Observing the terminal voltage will display ohms. In our application, the peaking shows a value of Zmax = $\frac{Zo?}{Rs} - 1 \times \sqrt{\left(\frac{Rs}{Zo}\right)^2}$ or 38.5 dBΩ with our application values.

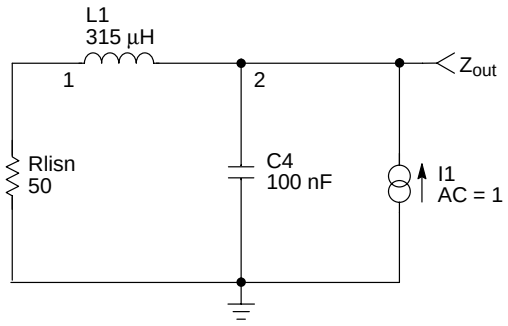

Figure 4e. By fixing the AC current source to 1 A, the voltage probe Zout directly gives ohms

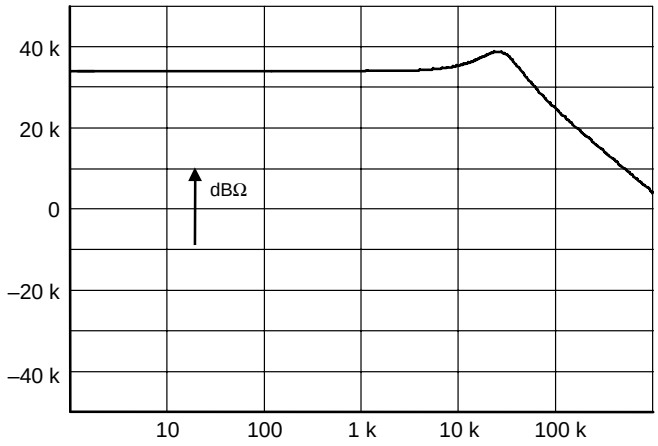

Figure 4f. This voltage plot show an output impedance affected by a low peaking

The exercise can be completed by sweeping the input impedance of the supply through its average model and pasting the results on figure 4e graph: there should be no overlap between the plots. Also the 50Ω impedance is a simplistic mains impedance representation and might obviously change depending on your local network arrangement. Different sweeps shall be carried on the LC filter to ensure a final low peaking. If the peaking is really strong, additional damping elements should be installed to decrease the filter Q.

The Final Filter Stage

We now have the choice to combine a CM filter together with a single inductor for the DM currents. As described in Figure 3d, we can also select a CM filter inductance knowing its leakage inductance and take benefit from it for DM cure. For a DM inductance below 500 µH, a 27 mH CM inductor can be a good choice. However, we need to precisely evaluate the available leakage inductance. With a 1:1 ratio, differential currents cancel the internal field. As a result, why not connecting together the dotted ends of the choke and letting naturally circulate differential currents while measuring the inductance . . . This is what is proposed by Figure 5a.

Figure 5b finally gives you the final impedance plot of the leakage inductor, showing again various stages: resistive in the lower portion, inductive in the medium portion and finally capacitive for higher frequencies. At 100 kHz, we can read 48 dBΩ or a 250 Ω impedance. The final calculation leads to an inductance of 398 µH or twice 199 µH when split into two components. Figure 5c gives its equivalent SPICE model with ohmic losses measured with a 4–wire multimeter.

Below stand measurement results comparing CM inductors provided by two different manufacturers:

Schaffner RN1140–08/2:
Lopen = 23 mH, Lleak = 238 µH or 2 x 119 µH.

Siemens B82723A2102–N1
Lopen = 31 mH, Lleak = 398 µH or 2 x 200 µH.

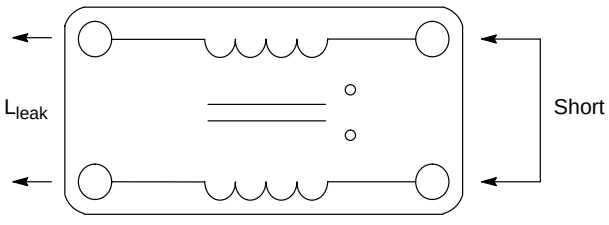

Figure 5a. Shorting the dot–ended windings gives you the value of the total leakage inductance.

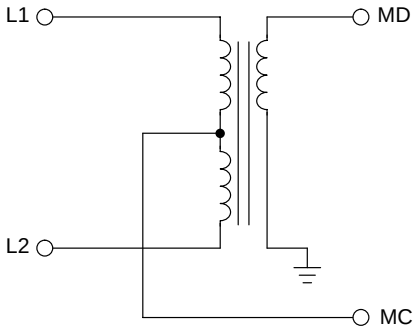

Figure 6a. A transformer to extract DM from CM.

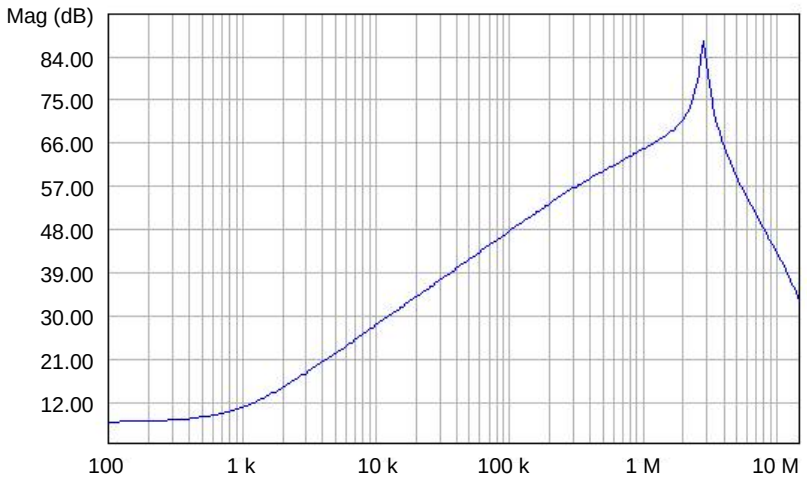

Figure 5b. A leakage inductance also welcomes parasitic elements.

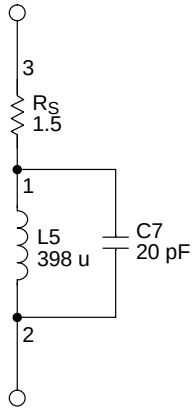

Figure 5c. These elements can be modeled using SPICE.

As you can imagine, combining the 100 nF–X2 capacitor (who also has parasitic elements) together with a Figure 5d–like inductor will deliver a result different from what we expect. Actually, the best would be to assess the final attenuation from the input of the filter (where the diode bridge connects) to the final output of the EMI receiver. SPICE does it in a snap–shot as shown by Figures 5d and 5e:

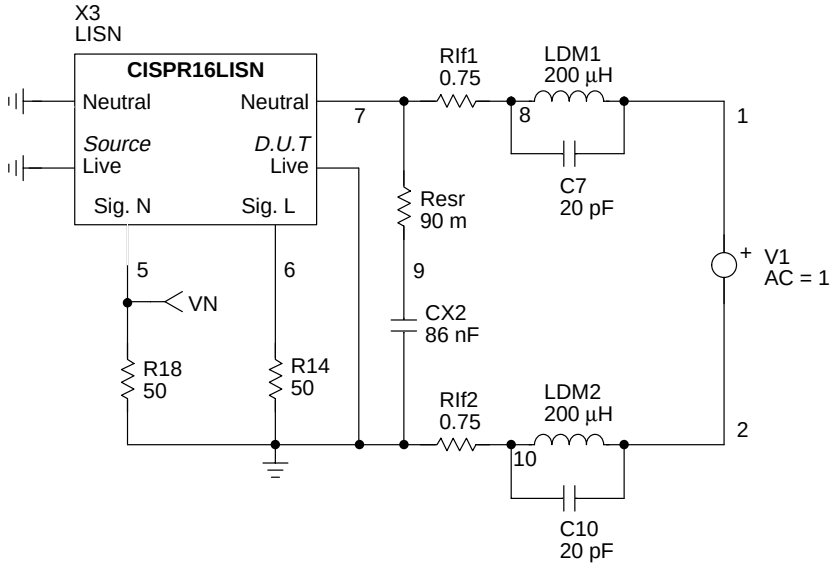

Figure 5d. This sketch lets you evaluate the filter attenuation once loaded by the LISN device.

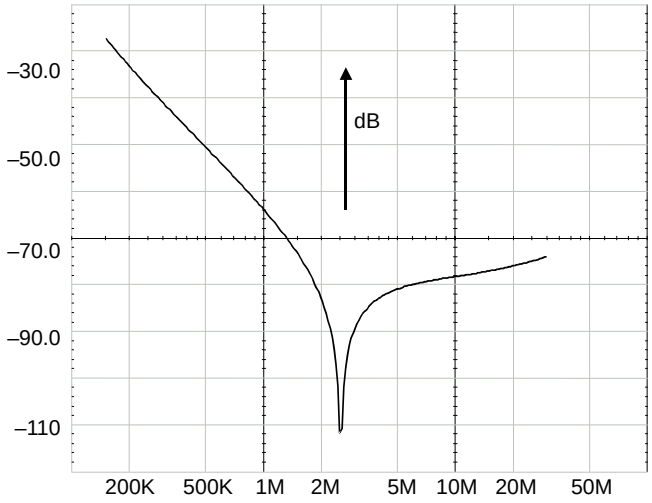

Figure 5e. The resulting final attenuation versus frequency.

As you can observe on Figure 5e, the rejection tends to degrade at higher frequencies due to the presence of parasitic components. But our attenuation at 190 kHz is 33 dB, enough to theoretically pass the DM test.

Let's now plug all these elements in Figure 4b test fixture and run a new test. Figure 5f shows how to install these elements before the LISN while Figure 5g plots the final results:

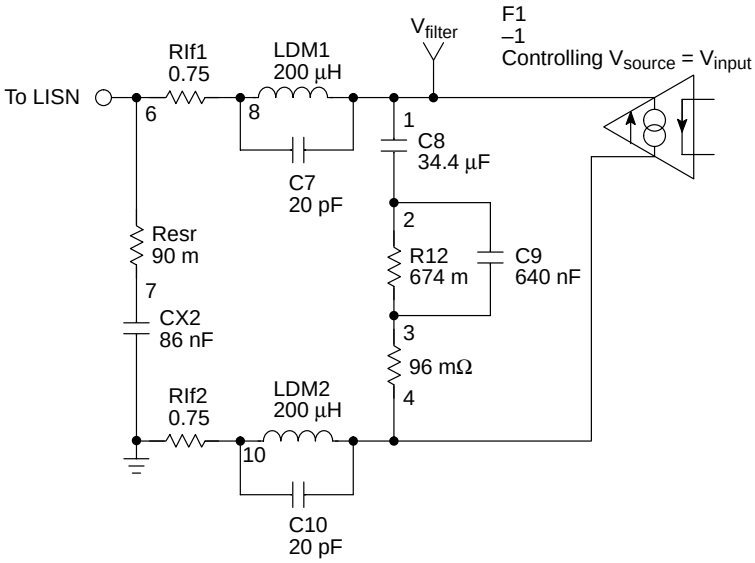

Figure 5f. This sketch shows how the filter finally behaves once loaded by the LISN device.

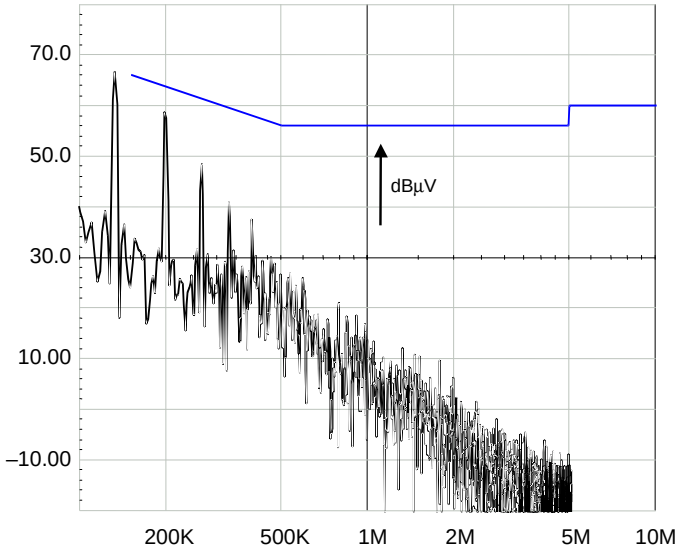

Figure 5g. The resulting spectrum confirming the filter action.

On the paper, we pass the test for DM measurements . . .

Real Measurements Versus Simulated Ones

Using the aforementioned approach, we are able to design a filter in a few iterations providing the computer is fast enough when running SPICE. But this approach is not worthwhile if true measurements on a board reveal large discrepancies. First of all, we must be able to extract differential mode from common mode noise. Unfortunately, standards fix limits regarding the total noise level (CM + DM) available on either L1 (live) or N (neutral), a switch routing either line to the receiver. To allow the study of both noise contents, we have modified a Rhode & Schwarz LISN (ESH–3) to which we added a second separated output. A switch simply loading one of the lines while running the final measurement on the other one. We now have L1 and N separated. If DM currents circulate 180° out of phase on the lines, summing L1 and N signals theoretically gives 0 while you obtain twice the CM level. At the opposite, subtracting the signals cancels CM and gives twice the DM. One limitation however exists: the impedance offered by both lines shall be perfectly equilibrated over the frequency range of interest, otherwise the rejection ratio will change . . . We have used an AEMC (Seyssins, France) DM/CM extractor (reference [2]) to perform our tests (Figure 6a). Figure 6b plots the DM quasi–peak SMPS signature without any EMI filter obtained with a Rhode & Schwarz ESPC EMI receiver. These results should be compared to Figure 4d drawing. The error on the main peak is only 8 dBs while the remaining peaks are not far away. Also quasi–peak measurements deliver levels lower than with a peak detector. Keep in mind that the DM/CM extractor ensures a good rejection up to 1 MHz (60 dB) while it tends to degrade in the higher portion. But the overall result is encouraging.

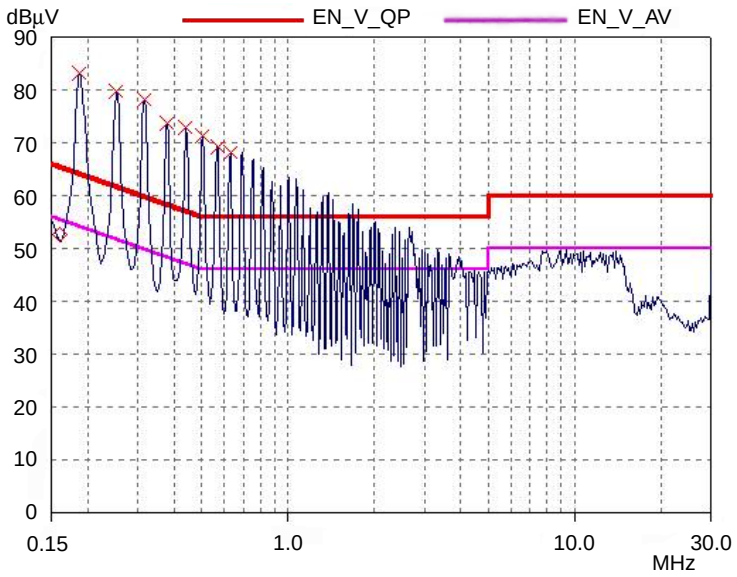

Figure 6b. The DM–only SMPS signature when operated without any EMI filter (quasi–peak detector).

Let's now connect our 27 mH CM inductance with a 100 nF–X2 capacitor over the line, as suggested by Figure 3d. If this capacitor needs to be increased above 100 nF, a discharge path has to be provided to avoid electrical shocks when touching the terminals immediately after unplugging the supply (IEC–950 defines a time constant less or equal to 1s). The final DM measurement is given by Figure 6c and confirms an attenuation of 35 dB at 190 kHz, exactly what we were looking for. The margin we have here is better than what we obtained in simulation, probably because of the quasi–peak internal time constants used during measurements.

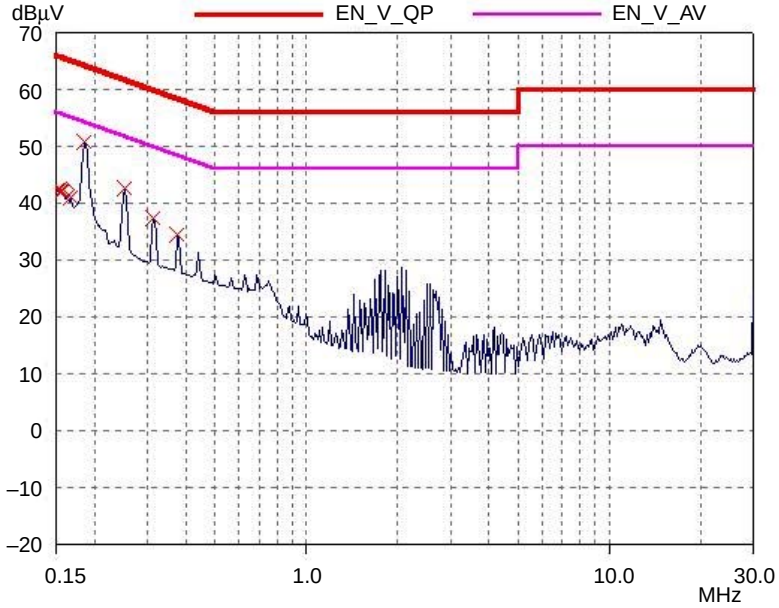

Figure 6c. The final quasi–peak DM–only measurement carried with an EMI receiver.

Total Noise Measurement

We now know that DM levels are within the limits. To attenuate the CM noise, we can wire a Y–type capacitor between the primary and the isolated ground as suggested by Figure 3d. For a two–wire applications, the IEC950 standard limits the maximum leaking current to less than 250 µA at 250 VAC power supply. The maximum capacitor value you can use is thus: Zmin = 250 V/250 µA = 1 MΩ. With a

50 Hz mains frequency, the Y capacitor cannot exceed $\frac{1}{2 \cdot \theta \cdot 50 \cdot 1E6}$ + 3 nF @ 50 Hz or 2.6 nF @ 60 Hz. Start by wiring a 1 nF capacitor or two 2.2 nF in series if you want to reinforce the security in case one of the Y capacitors would fail short. Figure 6d shows the final CM + DM plot in quasi–peak and clearly testifies for the CISPR22 compliance. This measurement was also successfully carried in average at worse operating conditions (100 VAC, 10 W).

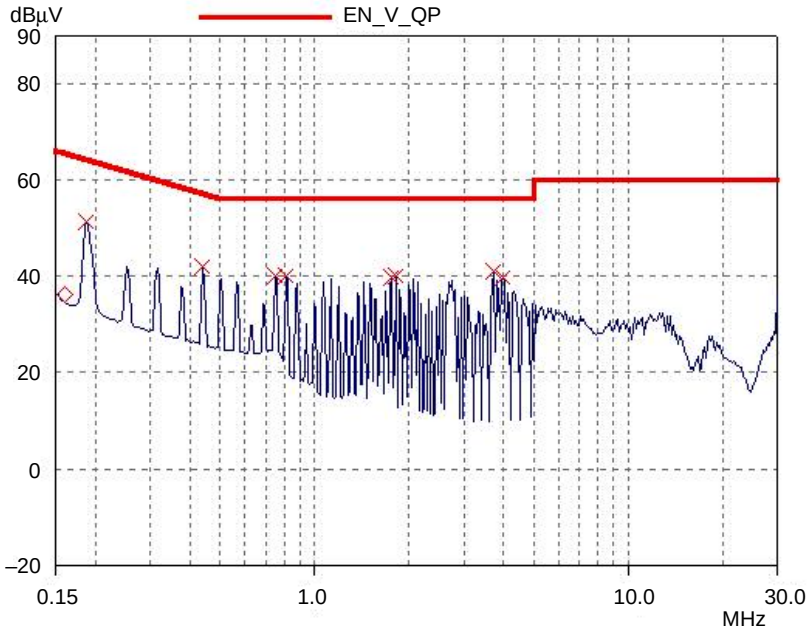

Figure 6d. The final composite QP plot carried over one line while the other is loaded (230 VAC, Pout = 10 W).

If the test would fail in common–mode, an option is to raise the CM inductor. Otherwise, you need to identify how noisy nodes can induce disturbances in adjacent copper traces or through the air. Carefully look at the rising time on the drain, how the output diode eventually rings, and various other unwanted ringing that could be snubbered by an RC network. As an advantage, the NCP1200 offers a controlled turn–on thanks to an asymmetrical output stage. Figure 7a shows how you normally slow–down the MOSFET during turn–on and speed up its discharge for turn–off. Figure 7b depicts how the NCP1200 output stage has been designed to save these two extra components. The driver's impedance at turn–on is about 40 Ω typically while it drops to 12 Ω for the turn–off phase. Figure 6d plot has been captured without any resistor in series with the MOSFET gate.

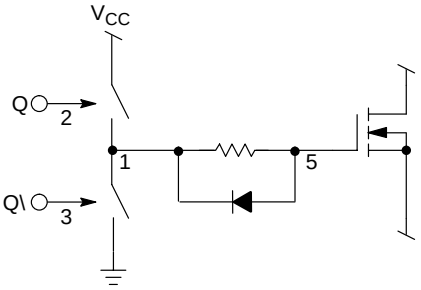

Figure 7a. A standard driver configuration needs external components to slow down the MOSFET without degrading the turn–off.

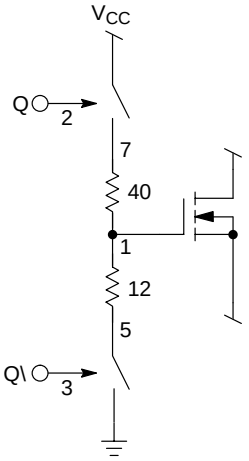

Figure 7b. The NCP1200 already integrates two resistors which avoid adding any other components.

Figure 8 portrays a complete working 10 W application example featuring an EMI filter.

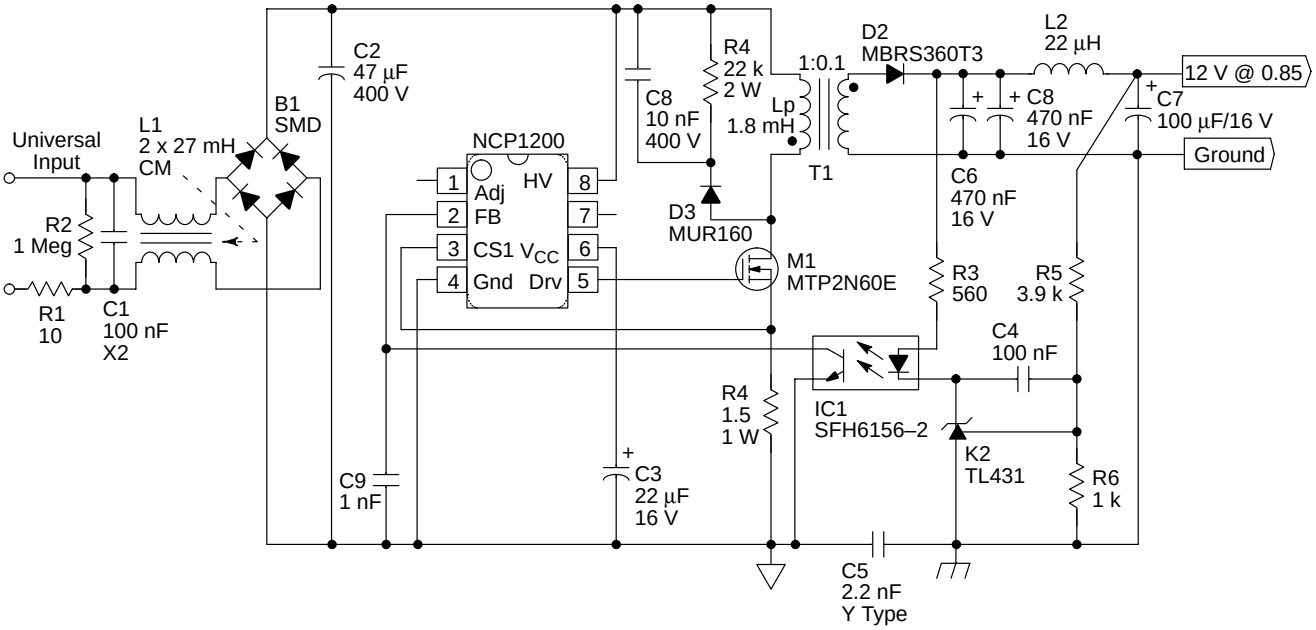

Figure 8. A complete 10 W AC/DC wall adapter featuring an EMI filter.

References

1. C. BASSO, “Spice predicts differential conducted EMI from switching power supplies”, EDN February 3, 1997.

2. AEMC, 86 rue de la Liberté 31180 SEYSSINS France. Tel. 33 (0)4 76 49 76 76, Fax. 33 (0)4 76 21 23 90.

3. T. WILLIAMS, “EMC for product designers”, Butterworth–Heineman, 1992, ISBN 0 7506 1264 9.

Line Impedance Stabilization Network SPICE Netlist:

```
.SUBCKT LISN mainsN mainsL1 measN measL1 L1 N
*
L4 measL1 1 100nH
R9 1 0 1k
C7 1 2 1uF
L5 2 3 1.75mH
R10 3 0 100m
C8 2 L1 1uF
L6 L1 6 50uH
R11 6 7 10m
R12 7 8 3.33
C9 8 0 8uF
C10 7 0 10n
L7 7 10 250uH
R13 10 mainsL1 10m
C11 mainsL1 0 2uF
R3 mainsL1 0 100m
C4 measN 0 10pF
L2 measN 11 100nH
R5 11 0 1k
C5 11 12 1uF
L3 12 13 1.75mH
R6 13 0 100m
C12 12 N 1uF
L8 N 16 50uH
R7 16 17 10m
R8 17 18 3.33
C13 18 0 8uF
C14 17 0 10n
L9 17 20 250uH
R14 20 mainsN 10m
C15 mainsN 0 2uF
R17 mainsN 0 100m
.ENDS
*********
```

AND8038

Implementing the NCP1200 in a 10 W AC/DC Wall Adapter

Prepared by: Christophe Basso
ON Semiconductor

ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

The NCP1200 implements a standard current mode architecture where the switch–off time is dictated by the peak primary current setpoint. By combining fixed frequency and skip cycle operation in a single integrated circuit, ON Semiconductor NCP1200 represents an excellent solution where cost and ease of implementation are premium: low–cost AC/DC adapters, auxiliary supplies, etc. Furthermore, the device does not require any auxiliary winding to operate and thus offers a real breakthrough alternative to UC384X based supplies. This application note details how to build an efficient and rugged 10 W adapter. This adapter is designed to operate from a universal mains (90–260 VAC) while providing a good standby power at no load.

The Electrical Schematic

Driving an external MOSFET, the NCP1200P60, only requires a sense element and a Vcc capacitor. Working together with an internal high–voltage current source, this Vcc capacitor provides the NCP1200 with an average DC level of 11 V typically while it also controls the short–circuit time out. All these parameters are detailed in the application note AND8023 available to download at *www.onsemi.com.* The electrical schematic appears in Figure 1:

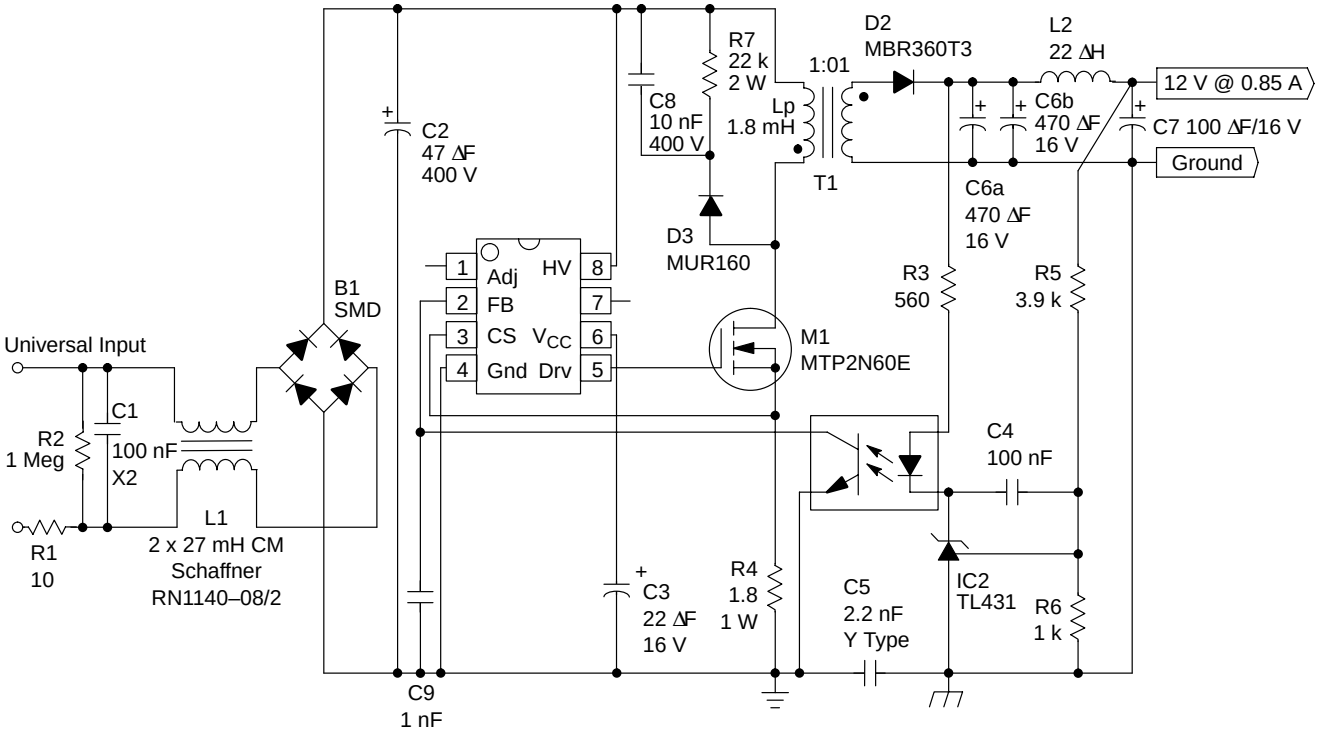

Figure 1. A 10 W AC/DC adapter built with the NCP1200

As stated in AND8023, the Vcc capacitor needs to be evaluated taking into account the startup sequence (actually seen as a transient short–circuit by the controller). An internal error flag is raised within the NCP1200 when an output overload occurs. If this error flag is still asserted when the Vcc capacitor reaches $UVLO_{Low}$ (around 10 V typical), then the IC goes into the latch–off phase: the output drive is locked and the internal consumption falls down to 350 μA typical. When another Vcc breakpoint is reached (around 6.0 V), then the internal current source turns on again and the IC tries to restart. If the error is still present, the protection activates again. If the short–circuit has gone, the IC resumes its operation and delivers its normal level. To check the correct value of the calculated Vcc capacitor, you need to monitor both output voltage and Vcc level on an oscilloscope. A shot as proposed by Figure 2 confirms the validity of a 22 μF choice. We can see that the internal error flag goes high first but as soon as Vout reaches its target level, the flag goes back to zero, confirming the normal controller behavior at the $UVLO_{Low}$ checkpoint. This experiment should be carried in the worse case conditions, e.g. low mains and maximum output load.

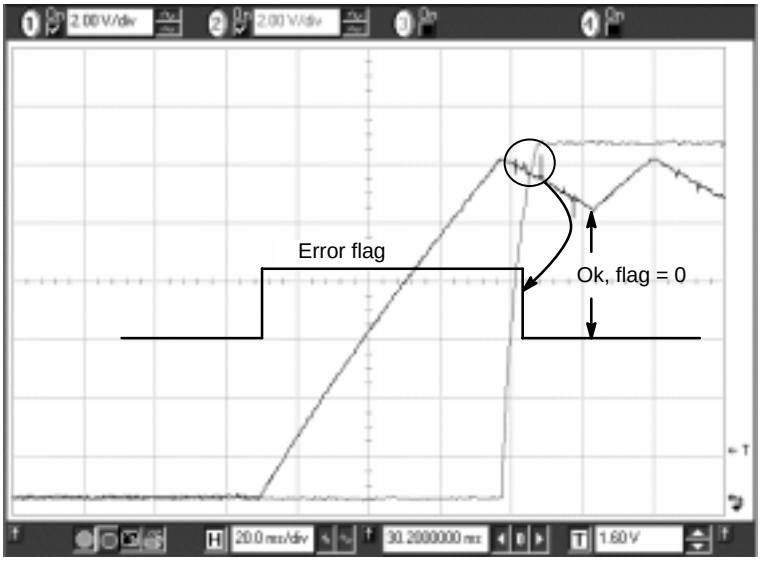

Figure 2. The startup sequence shows a V_{out} establishment before $UVLO_{Low}$ is reached

Feedback Loop

In this application, a precise output voltage is obtained through the use of a TL431. Since we target a 12 V output, you calculate the upper and lower voltage sense elements by applying the following formula:

$$V_{out} - \frac{Rupper}{Rlower} \times 1 \cdot Vref$$

Depending on the TL431 type, Vref can be 2.5 V or 1.25 V. With a 2.5 V reference, Rupper (R5) = 3.9 kΩ and Rlower (R6) = 1.0 kΩ. This network ensures a bridge current flow of 2.0 mA which is good for the noise immunity. As any closed loop systems, a compensation network needs to be tailored to stabilize the loop. In this aspect, the NCP1200 average SPICE model will save you a tremendous amount of time. The simulation template appears in Figure 3 on the following page, showing how to wire the NCP1200 average model with INTUSOFT's IsSpice4.

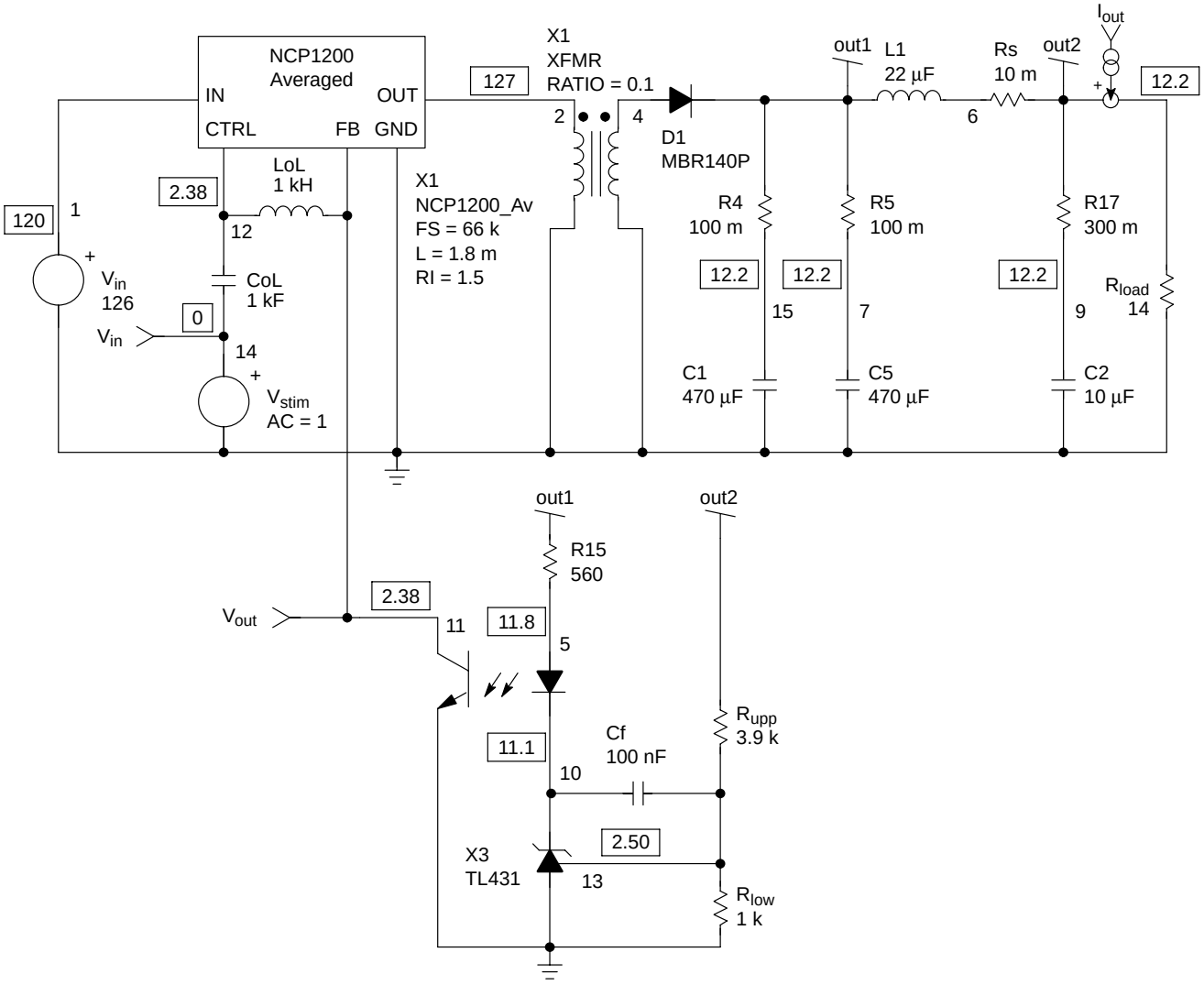

Figure 3. The average model of the NCP1200 when used in AC analysis

The loop is kept opened in AC thanks to LoL which exhibits a fairly high value. However, during its bias point calculation, SPICE opens all capacitors and shorts all inductors. Therefore, LoL closes the loop in DC but blocks the AC stimuli to allow Bode plot generation. Figure 4 portrays the simulated results with a 100 nF feedback capacitor, while Figure 5 offers the true measurement curves.

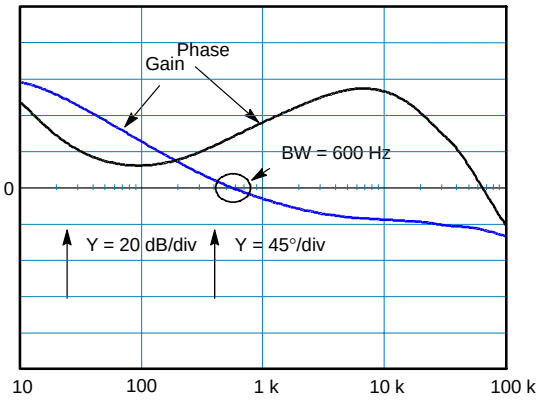

Figure 4. Bode plot obtained using SPICE…

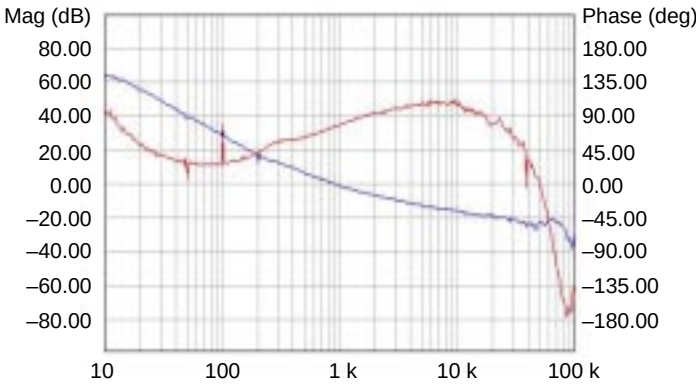

Figure 5. …confirmed by a network analyzer measurement

As you can see, curves are in good agreement, despite the small DC gain error which predicts a slightly lower bandwidth in the case of SPICE. In both cases, the phase and gain margins confirm the good stability of the design, but also the validity of the SPICE model (based on Ben–Gurion University GSIM approach). The NCP1200 FB pin being a high impedance path, a 1.0 nF placed between this pin and ground will prevent any noise picking during operation.

Transient Results

Using the NCP1200 design aid spreadsheet lead us to a transformer offering the following specs: Lprim = 1.8 mH, Np:Ns = 1:0.1, RM8 or E25 core. For ease of implementation, this transformer will be available from Coilcraft, as referenced in the bill of material. The maximum peak current has been fixed to 600 mA. This value essentially defines the air gap requirement in the transformer but also the final potential transformer mechanical noise generated in standby. As explained, the NCP1200 skips switching cycles in standby operation. By default, skip cycle takes place at 1/3rd of the maximum peak current: 200 mA in our case. Because skip cycle frequency will naturally enter into the audible range, it is important that the skip current value does not engender noise. Fortunately, if that would be the case, you could still wire a resistor bridge on pin 4 to fix a DC point different than the default one (1.4 V). As a result, you can force skip operation to happen at less than 1/3rd of the maximum peak current. However, keep in mind that the highest peak currents in skip mode offer the best standby power. This is because of the switching cycles population within the bursts: less cycles mean less switching losses and better efficiency at no load.

A quick method to assess the RMS current in the MOSFET consists in simulating the whole AC adapter with SPICE. This has already been presented in AND8029 and the schematic will not be reproduced here. The simulated results are given below through Figure 6 and Figure 7 while the supply is delivering 10 W:

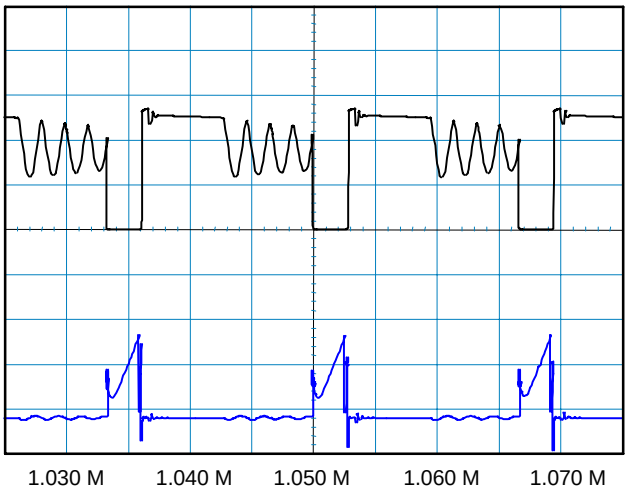

Figure 6. Transient results obtained with IsSpice4…

Figure 7. Compared to true measurements

Worse case conditions (low mains, maximum output current) gives an RMS drain current of 230 mA. Associated with a 6.5 Ω $Rds_{(ON)}$ @ Tj = 100°C, the conduction losses grow up to 340 mW. Using a TO220 package for the MOSFET, offers the ability to dissipate a given amount of power in free–air conditions (without a heatsink) of: $Pmax = \frac{Tj + Tamb}{R\Omega j + a} = 1.3$ W. Further switching losses measurements confirm the ability to use this MOSFET without any heatsink up to an ambient of 80°C.

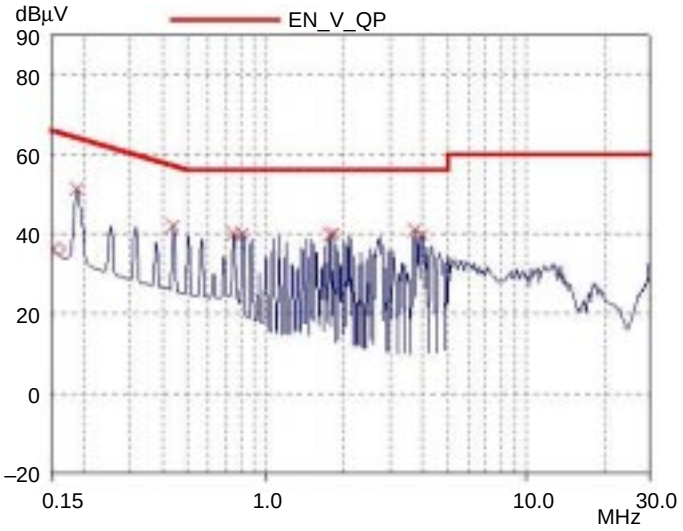

Figure 8. The final composite QP plot carried over one line while the other is loaded (230 VAC, P_{out} = 10 W)

Conducting EMI Filtering

The 10 W NCP1200 demo board is equipped with a front stage filter who lets you pass the CISPR22 EMI tests in both quasi–peak and average detector methods. The method we used for calculating the filter is described in AND8032 “Conducted EMI Filter Design for the NCP1200”. The front stage is made of a single common mode (CM) choke whose wiring method gives enough leakage inductance for differential mode (DM) filtering. Figure 8 plots the final CM+DM noise component confirming the test passing.

Final Performance

We have carried some power tests on the 10 W adapters and the below numbers will confirm the pertinence of choosing ON Semiconductor’s NCP1200 for your next designs:

Vin_{DC}	Pout(W)	Pin(W)	η(%)
126	0	0.245	–
126	10.5	12.6	83.3
356	0	0.462	
356	10.5	13.17	79.7

The standby power can be further reduced by implementing one of the method proposed in AND8023 either through an additional diode or an auxiliary winding.

Thanks to its inherent protection circuitry, NCP1200 protects the power supply in presence of a permanent output short circuit. When shorted, the average output current was less than 500 mA.

10 W Demoboard, Bill of Material

R1	10 Ω, 1 W through holes
R2a R2b	2 times 560 kΩ SMD in series
R3	560 Ω SMD
R4	1.8 Ω, 1W SMD or 1.8 Ω 1 W through holes
R5	3.9 kΩ SMD
R6	1 kΩ, SMD
R7	22 kΩ, 2 W through holes
L1	Schaffner RN114–08/2
L2	22 μH, 1 A
M1	MTP2N60E, TO–220 through holes, ON Semiconductor
IC1	SFH615A–2, SMD (optocoupler)
IC2	TL431BC (TO–92), ON Semiconductor
IC3	NCP1200P60, DIP8, ON Semiconductor
C1	100 nF X2/ 250 VAC
C2	47 μF/400 V, snap–in vertical
C3	22 μF/16 V, vertical
C4	100 nF, SMD
C5	1.5 nF Y1 type only
C6a	470 μF/16 V, vertical
C6b	470 μF/16 V, vertical
C7	100 μF/16 V, vertical
C8	10 nF/400 V
D1	MUR160, ON Semiconductor
D2	MBRS360T3, ON Semiconductor

B1 Bridge 1 A/600 V, mini DIP
Transformer available from Coilcraft U.S, ref. : Y8848–A
Mains connector: Schurter GSF1.1202.31 with fuse

Other Available Documents Related to NCP1200:

AND8023/D, “Implementing the NCP1200 in Low–Cost AC/DC Adapters”
AND8029/D, “Ramp Compensation for the NCP1200”
AND8032/D, “Conducted EMI Filter Design for the NCP1200”
PSpice, IsSpice4 and Micro–Cap *Averaged* and *Transient* models available in ready–to–use templates at *www.onsemi.com*
NCP1200 Design aid spreadsheet with EBNCP1200/D

Printed Circuit Board Details

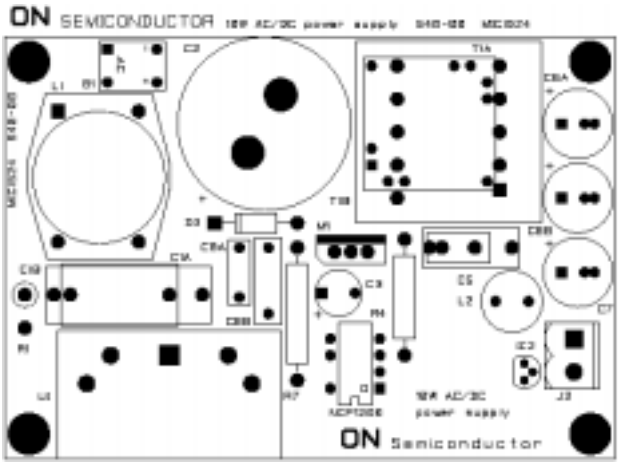

Figure 9. Component Side, Silk Screen, Scale 1

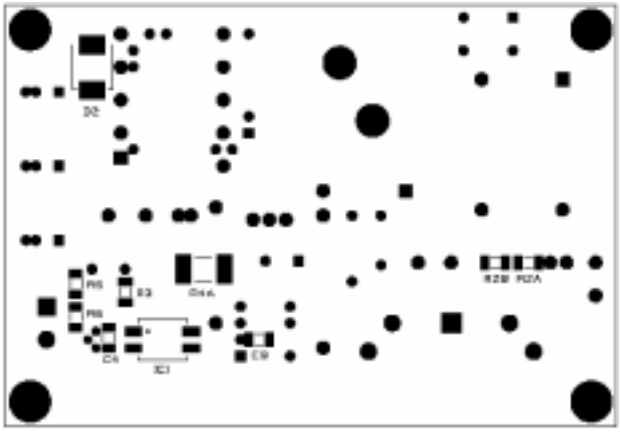

Figure 10. Solder Side, Silk Screen, Scale 1

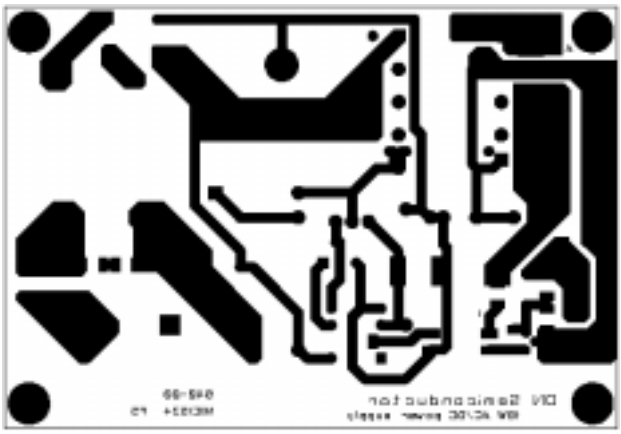

Figure 11. Copper Traces, Scale 1

Implementing Constant Current Constant Voltage AC Adapter by NCP1200 and NCP4300A

Prepared by: Hector Ng
ON Semiconductor

ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

Introduction

This paper describes a compact design of constant current constant voltage (CCCV) AC adapter based on the current mode PWM controller NCP1200 and the secondary side feedback IC NCP4300A. By these two ICs from ON Semiconductor, circuit design is much simplified. These devices enable users to meet ever increasing demand of smaller dimension and more sophisticated protection feature of AC adapter.

On the primary side, NCP1200 is used as the PWM controller. This current mode controller requires very few external components and no auxiliary winding is needed to supply this IC. In addition, NCP1200 can fulfill IEA recommendation easily because it features a pulse skipping low power consumption mode.

NCP4300A is a general purpose device which consists of two operational amplifiers and a high precision voltage reference. One of the operational amplifiers is capable of rail to rail operation. NCP4300A is employed to provide voltage as well as current feedback to NCP1200.

Output of the AC adapter is maintained at 5.2 V from no load to 600 mA. Further increase in load enters constant current output portion and output is kept at 600 mA down to zero volt. This output characteristic assures a basic protection against battery overcharge which is needed by a lot of applications, for instance cellular phone AC adapter.

Circuit Description

Circuit and BOM of the AC adapter is shown in Figure 1 and Table 1. This design can accept universal AC input from 90 V to 264 VAC. Bulk capacitors C5 and C6 are split by inductor L1 and L2 to form the EMI filter as well as to provide energy storage for the remaining DC to DC converter circuit. Thanks to dynamic self supply of NCP1200 (please refer to NCP1200 data sheet), Vcc capacitor C7 is charged to startup voltage 11.4 V and the power MOSFET MTD1N60E starts switching. To reduce power consumption of NCP1200, HV pin (pin 8) is supplied by half wave rectification through a parallel combination of diode D6 and resistor R13. A small signal diode 1N4148 is enough for this function because diode D6 just has to withstand one diode drop during negative half cycle. R13 is to equilibrate the voltages on the 1N4148 when both diodes and high volt current source of NCP1200 are in the off state. R12 is to set the power level at which NCP1200 goes into pulse skipping, please refer to below section for more details. RCD snubber R1, C1 and D3 provides the necessary snubbing function to prevent drain voltage of MTD1N60E to exceed 600 V. Choosing suitable value for the sensing resistor R7 is very important as it limits the primary peak current during power up. If its value is too low, the system cannot deliver enough power during full load low AC input. On the contrary, the transformer may go into saturation and damages Q1 and NCP1200. Information on how to determine value of R7 is elaborated in latter paragraph.

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Publication Order Number:
AND8042/D

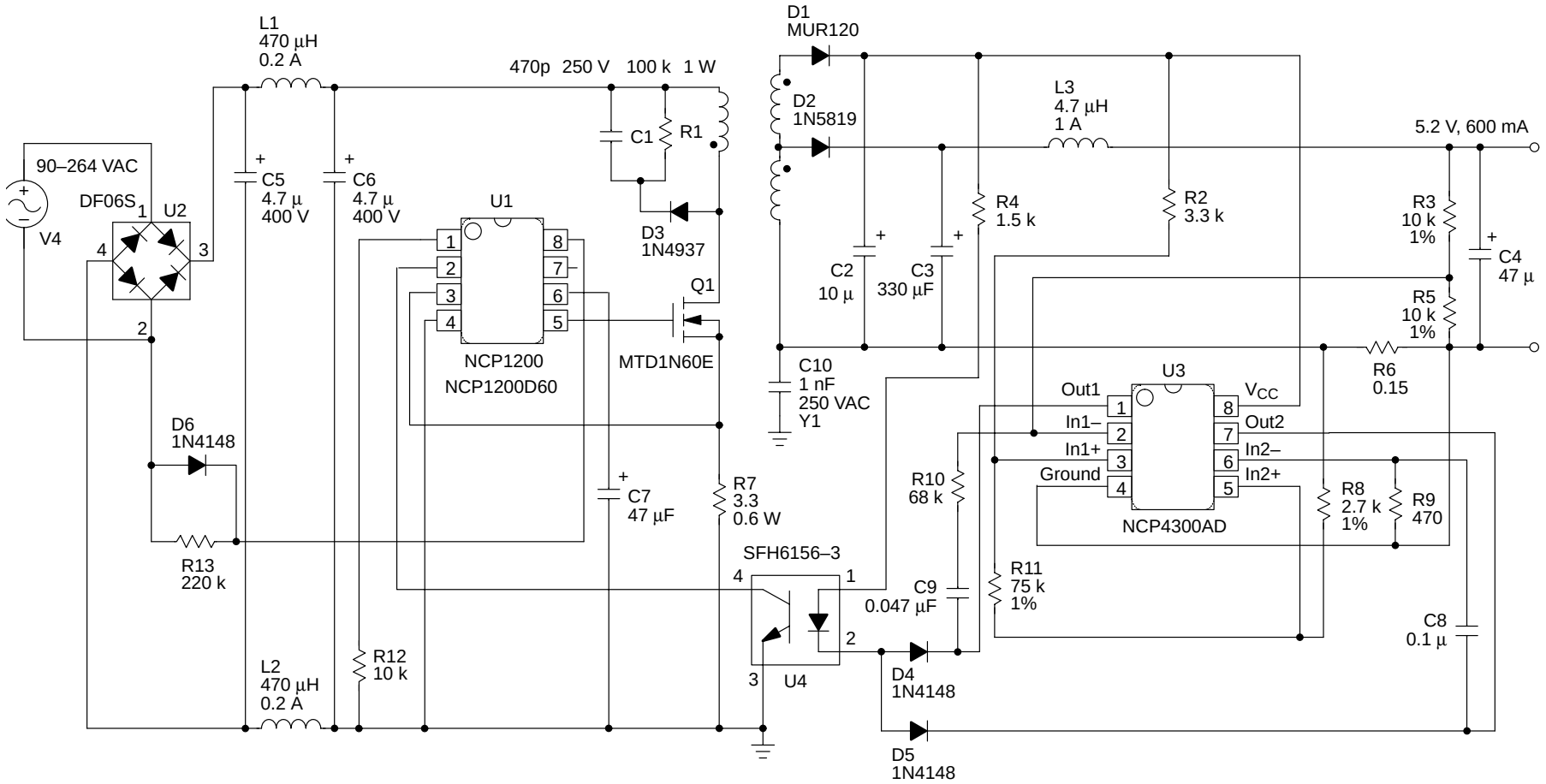


Figure 1. Circuit Description

Table 1.

Reference	Part	Quantity	Manufacturer
U1	NCP1200D60	1	ON Semiconductor
U2	DF06S	1	General Semi or IR
U3	NCP4300AD	1	ON Semiconductor
U4	SFH6156–3	1	Infineon
Q1	MTD1N60E	1	ON Semiconductor
C1	470 p, 250 V	1	
C2, C7	10 F, 25 V	2	
C3	330 F, 35 V	1	Panasonic FC Series or Rubycon JXA Series
C4	47 F, 16 V	1	Panasonic FC Series or Rubycon JXA Series
C5, C6	4.7 F, 400 V	2	
C8	0.1 F	1	
C9	0.047 F	1	
R1	100 Kμ , 1.0 W	1	
R2	3.3 K	1	
R3, R5	10 K, 1%	2	
R4	1.5 K	1	
R6	0.15 W, 0.1 W SMT	1	
R7	3.3 μ , 0.6 W	1	
R8	2.7 Kμ , 1%	1	
R9	470 μ	1	
R10	68 K	1	
R11	75 Kμ , 1%	1	
R12	10 Kμ	1	
R13	220 Kμ	1	
D1	MUR120	1	ON Semiconductor
D4, D5, D6	1N4148	3	
D2	1N5819	1	ON Semiconductor
D3	1N4937	1	ON Semiconductor
L1, L2	470 H, 0.2 A	2	
L3	4.7 H, 1.0 A	1	
T1	Transformer	1	
C10	1.0 nF, 250 VAC, Y1 Cap	1	

The secondary side of the transformer consists of 2 windings, the output winding as well as a higher voltage winding which is used to supply power to NCP4300A. As the output may drop to 0 V during constant current operation, turn ratio of this higher voltage winding must be able to sustain minimum Vcc as specify by NCP4300A. Or else, the system will be lost of feedback and the output is not under control anymore. Figure 2 shows the internal block of NCP4300A. A 2.6 V, 1.0% tolerance voltage reference is connected to the non–inverting terminal of OP1. Thus, OP1 gives voltage feedback when its inverting terminal is connected to the potential divider R3 and R5. Characteristic of the voltage reference is similar to industry standard TL431 and a bias current supplied by R2 is needed to guarantee proper operation. This 2.6 V is also divided down by R11 and R8 to provide reference for output current sensing. Voltage developed at the non–inverting terminal of OP2 is:

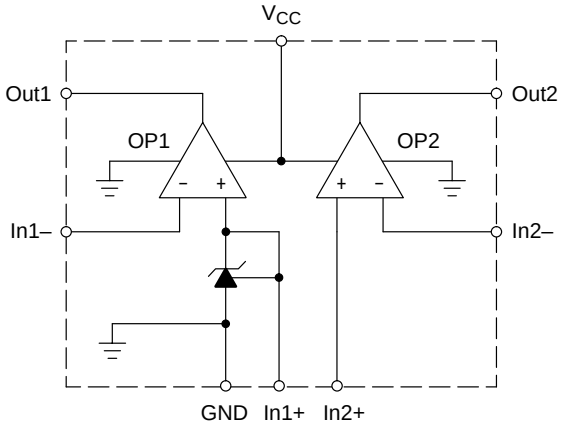


Figure 2.

$$V_{current\ -\ reference} = \frac{2.7\ K}{2.7\ K + 75\ K} \cdot 2.6 = 0.09\ V$$

Since Out1 and Out2 are wired together by diodes D4 and D5, feedback current through the opto–coupler U4 is dominated by whichever op–amp output that has a lower voltage. Thus feedback is dominated by OP1 until voltage developed across R6 reaches 0.09 V and this is equivalent to 600 mA passing through R6. Thanks to the rail to rail capability of OP2 in NCP4300A, current sensing function is guaranteed although voltage of non–inverting terminal of OP2 is below ground. Once the output current reaches 600 mA, feedback action is taken over by OP2 and one will see a drop in output voltage if load is further increase but output current remains constant. C9, R10 and C8, R9 provide necessary feedback compensation for voltage and current loop respectively.

Transformer Design

Transformer design involves very tedious calculation. An Excel spreadsheet has been specially designed for NCP1200 to facilitate user with a quick determination of transformer parameters. Table 2 and Table 3 display the results of the spreadsheet after keying in system parameters. Although recommended transformer primary inductance is 4.6 mH, 3.2 mH is chosen instead. A lower primary inductance enables us to have a lower flyback voltage added to the drain of the power MOSFET. This in turn allow us to use a less heavy snubber which implies less power dissipated on the snubber. Disadvantage of a lower primary inductance is the increase in MOSFET conduction loss because of higher primary peak current. However, output of this AC adapter is only 3.0 W and typical $R_{DS(on)}$ of MTD1N60E is merely 5.9 μ. Increment in conduction loss is not significant in this case.

After the primary inductance is determined, we have to decide on the ferrite core. It can be seen from the Excel spreadsheet that E16/8/5 core is big enough for this transformer. Primary (N1) and secondary (N2) number of turns needed are 166 and 12 respectively. However, one more winding N3 is required to supply NCP4300A. It is critical that voltage output of N3 must be higher than minimum operating voltage of NCP4300A even when output has dropped to 0 V. Under this condition, output winding loop can be represented by Figure 3.

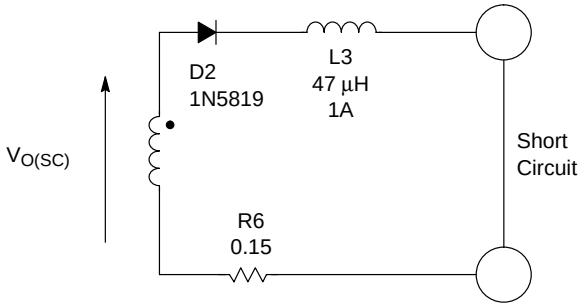


Figure 3.

Table 2.

NCP1200 DISCONTINUOUS MODE DESIGN WORKSHEET			
System Parameters			
V_{max}	264 V	Maximum AC Input Voltage	User Input Cells
V_{min}	90 V	Minimum AC Input Voltage	Results
F_{line}	50 Hz	Line Frequency	
$V_{min(DC)}$	85.73 V	Minimum DC Voltage	
$F_{s(max)}$	69 KHz	Maximum Switching Frequency	
$F_{s(typ)}$	60 KHz	Typical Switching Frequency	
$F_{s(min)}$	51 KHz	Minimum Switching Frequency	
V_o	5.2 V	Output Voltage	**Selected Device**
I_o	0.6 A	Maximum Output Current	60 KHz
θ	75%	Efficiency	
V_{bd}	600 V	Power MOSFET Breakdown Voltage	
V_d	1 V	Output Diode Voltage Drop	
P_I	4.16 W	Input Power	
$I_{in(pk)}$	0.21 A	Maximum Primary Peak Current	
$V_{o'}$	85.72 V	Reflected Output Voltage	
$V_{pwr\_sw(max)}$	459.07 V	Maximum Voltage across the Power Switch Circuit (Less Leakage Spike)	
D_{max}	0.50	Maximum Turn On Duty (Full Load, Low Line)	
$I_{in(av)}$	0.05 A	Maximum Input Average Current	
Ratio N1/N2	13.83	Turn Ratio Between Primary and Secondary	
Recommended L_p	4.650 mH	Recommended Primary Inductance	
L_p	3.200 mH	Primary Inductance	
$R_{DS(ON)}$	16 ohm	Maximum $R_{DS(ON)}$ of Power MOSFET	
$P_{dls(pwr\_sw)}$	0.12 W	Maximum Conduction Loss of Power MOSFET	
Input Filter Capacitor			
Recommended C_{in}	14 F	Recommended Input Filter Capacitance	
C_{in}	9.4 F	Input Filter Capacitance	
Output Diode Selection			
$I_{o(pk)}$	2.40 A	Output Peak Current	
V_{ro}	32.20 V	Output Maximum Reverse Voltage	

Table 2. (continued)

NCP1200 DISCONTINUOUS MODE DESIGN WORKSHEET							
Wire Selection							
$I_{in(rms)}$	0.08 A	Maximum Input RMS Current					
$I_{o(rms)}$	0.98 A	Maximum Output RMS Current					
Lay_p	1	Layer of Primary Winding					
Lay_s	1	Layer of Secondary Winding					
Primary Wire Size	AWG 35						Maximum Wire Size
Secondary Wire Size	AWG 24						AWG 24
RMS Current Density	4.9 (A/mm^2)						
Core Selection							
Flux Density Safety Factor	0.4						
Bobbin Usage Factor	0.4						
Core Type	Core Type A	Core Type B	Core Type C	Core Type D	Core Type E		
Core Name	E 16/8/5	EI28–Z	E25/13/7	E 30/15/7	E32/16/9		
A_e	20.1	86	52.5	60	83	mm^2	Effective Area
B_{sat}	0.5	0.5	0.5	0.5	0.5	T	Saturation Magnetic Flux Density
A_w	22.3	39.4	61	90	108	mm^2	Bobbin Winding Window Area
A_{bob}	8.92	15.76	24.4	36	43.2	mm^2	Usable Area of Bobbin for Winding
Gap Length d	0.22	0.05	0.08	0.07	0.05	mm	
N_1	166	39	63	56	40		Primary Number of Turns
N_2	12	3	5	4	3		Secondary Number of Turns
A_p	0.02	0.02	0.02	0.02	0.02	mm^2	Area of Single Turn of Primary Wire
Lay_p	1	1	1	1	1		Layer of Primary Winding
A_{pri}	3.98	0.93	1.52	1.33	0.96	mm^2	Area of Primary Winding
A_s	0.26	0.26	0.26	0.26	0.26	mm^2	Area of a Single Turn of Secondary Wire
Lay_s	1	1	1	1	1		Layer of Secondary Winding
A_{sec}	3.12	0.73	1.19	1.04	0.75	mm^2	Area of Secondary Winding
A_{sum}	7.09	1.66	2.72	2.38	1.72	mm^2	Total Winding Area
Enough Space?	OK	OK	OK	OK	OK		
Maximum Peak Current (Sensing Resistor) Setting							
DL_p	10%	Tolerance of Primary Inductance					
$L_{p(min)}$	2.880 mH	Lowest Primary Inductance					
$L_{p(max)}$	3.520 mH	Highest Primary Inductance					
$I_{p(worst)}$	0.24 A	Worst Case Maximum Primary Peak Current (Lowest Switching Frequency and Lowest Primary Inductance					
$R_{sense(max)}$	4.20 ohm	Maximum Allowable Sensing Resistance					
R_{sense}	3.30 ohm	Sensing Resistance					
B_{init}	0.32 T	Magnetic Flux Density During Startup					

Table 3.

Transformer Specification			
Primary Inductance	L_p	3.200 mH	
Core Type	=	E 16/8/5	
Primary Wire Size	=	AWG 35	
Layer of Primary Winding	=	1	**Select Core Type**
Primary Number of Turns	N_1	166	Core Type A
Secondary Wire Size	=	AWG 24	
Layer of Secondary Winding	=	1	
Secondary Number of Turns	N_2	12	
Gap Length	d	0.22 mm	
Enough Space?	=	OK	
Input Filter Capacitor			
Input Filter Capacitance	C_{in}	9.4 F	
Output Diode			
Maximum Reverse Voltage	V_{ro}	32.20 V	
Sensing Resistor			
Sensing Resistance	R_{sense}	3.30 ohm	

During flyback cycle, voltage across the output winding $V_{o(sc)}$ is:

$V_{o(sc)}$ = V(D2) + V(L3) + V(R6) + V(PCB trace)

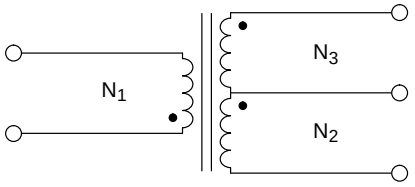
V(D2) = forward voltage drop of 1N5819 ≈ 0.6 V
If resistance of L3 is 0.1 μ, V(L3) = 0.1 μ × 0.6 A = 0.06 V
V(R6) = 0.15 μ × 0.6 A = 0.09 V
If resistance of PCB trace is 0.15 μ, V(PCB trace) = 0.15 μΔ× 0.6 A = 0.09 V

Therefore $V_{o(sc)}$ is 0.84 V and volt/turn is 0.84/12 = 0.07.

Minimum operating voltage of NCP4300A is 3.0 V. Its supply winding voltage has to be 0.6 V higher if we assume forward drop on MUR120 is 0.6 V. Minimum number of turns required for this winding is 3.6/0.07 ≈ 52 turns. As can be seen from the schematic, these 52 turns can be added on top of the output winding. Therefore 40 turns is enough for N3. When output is 5.2 V, supply winding voltage of NCP4300A is approximately 24.5 V. Thanks to its wide operating voltage, 24.5 V is below maximum operating voltage of NC4300A (35 V). The final design of the transformer is shown in Figure 4.

Another important consideration is the value of sensing resistor R7. Value of R7 control maximum primary peak current by the following equation.

$$I_{p(max)} = \frac{1.0\ V}{R7}$$



N_1 = 166T, AWG # 34, π : 0.16 mm
N_2 = 12T, AWG # 24, π : 0.51 mm
N_3 = 40T, AWG # 34, π : 0.16 mm

Core = E16/8/5
Magnetic Material = PC40 or N67
Air Gap = 0.22 mm (center limb)
Primary Inductance (Across N_1) = 3.2 mH

Figure 4.

For discontinuous mode operation, maximum power that can be delivered by the system is:

$$P_{max} = \frac{1}{2} L_p I_{pk(max)}^2 f$$

Where L_p is the primary inductance which we already decided and f is the switching frequency. In other words, $I_{pk(max)}$ must be high enough to give full load power and this implies that R7 cannot be too high. The Excel spreadsheet has calculated for us that R7 must be lower than 4.2 μ. 3.3 μ is chosen to give some headroom during transient response. Before finalizing on this value, one must make

sure that transformer does not saturate at power up. During power up when output voltage is much lower than rated value, MTD1N60E is switched off not by PWM action. The power MOSFET is switched off because the primary peak current has reached its maximum allowable value, $I_{p(max)}$. $I_{p(max)}$ drives the transformer core up the B–H curve of the magnetic material. B, magnetic flux density must be lower than the saturation value B_{sat}. For most magnetic material, B_{sat} equals 0.5 T at room temperature. Nevertheless, B_{sat} falls as temperature increases and at 120°C, B_{sat} becomes 0.35 T. Last row in Table 2 shows the magnetic flux density during startup. The value is 0.32 T, thus 3.3 μ should give us a safe startup.

Pulse Skipping Mode

NCP1200 has a pulse skipping standby mode feature and the power level to enter standby mode is adjustable. Figure 5 shows the equivalent circuit of the Adj pin with a 10 K resistor connecting Adj pin to ground. When the voltage at FB pin falls below Adj pin, NCP1200 starts to skip cycle. This voltage V_{stby} is:

$$V_{stby} = \frac{10\ K \cdot \cdot 29\ K}{10\ K \cdot \cdot 29\ K + 75.5\ K} \cdot 5.2\ V = 0.466\ V$$

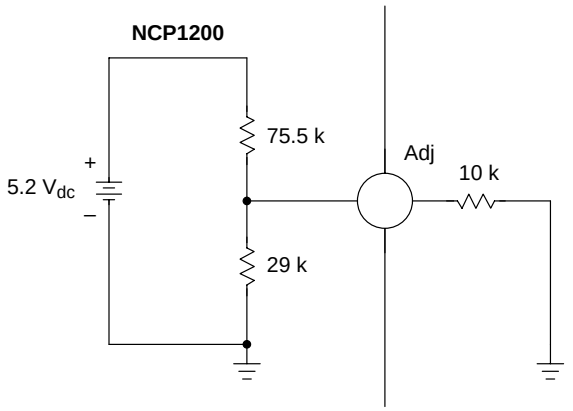


Figure 5.

Since NCP1200 is a current mode device, there is a direct relationship between voltage at the FB pin and the voltage developed by the peak current across the sensing resistor, ie. voltage at CS pin, V_{cs}. As can be seen from the block diagram of NCP1200 datasheet, V_{cs} is compared with one fourth of FB pin voltage. Therefore at the verge of entering into pulse skipping mode, we should see a relationship as shown on Figure 6.

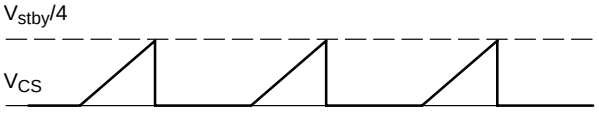


Figure 6.

Therefore the input power level P_{stby} that enters standby mode is given by the following equation.

$$P_{stby} = \frac{1}{2} L_p \left(\frac{V_{stby}}{\sqrt{4R_7}}\right)^2 f$$

$$= 0.5 \times 3.2\ E^{-3} \times \left(\frac{0.466}{\sqrt{4 \times 3.3}}\right)^2 \times 60000$$

$$= 0.12\ W$$

At light load condition, efficiency should be lower than that of full load. Assume efficiency is 50% when input power is at 0.12 W, load current $I_{o(stby)}$ at that time is:

$$I_{o(stby)} = \frac{0.12\ W \times 50\%}{5.2\ V} = 0.01\ A$$

Remember that Vo drops when Io attains 0.6 A. When Vo drops below certain voltage, NCP1200 will also enters pulse skipping mode. Once again, assume efficiency is 50% when input power is at 0.12 W, $V_{o(stby)}$ at that time is:

$$V_{o(stby)} = \frac{0.12\ W \times 50\%}{0.6\ A} = 0.1\ V$$

In summary, NCP1200 starts pulse skipping when Io is below 0.01 A or Vo is below 0.1 V.

Actual Performance

Figure 7 and Table 4 shows the actual performance of the circuit.

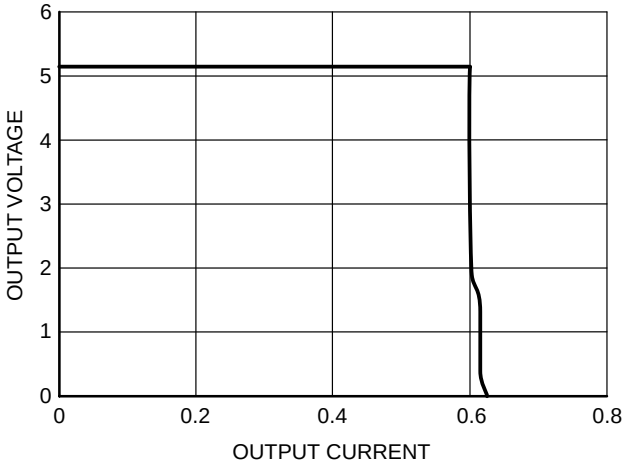


Figure 7. V_o–I_o Characteristic @ 110 VAC Input

Table 4.

Test	Conditions	Results
Line Regulation	V_{in} = 90 to 264 VAC, I_o = 0.6 A	Ω = 0.5 mV
Load Regulation	V_{in} = 110 VAC, I_o = 0 to 0.6 A V_{in} = 220 VAC, I_o = 0 to 0.6 A	Ω = 3.0 mV Ω = 3.0 mV
Output Ripple	V_{in} = 110 VAC, I_o = 0.6 A V_{in} = 220 VAC, I_o = 0.6 A	40 mVpp 40 mVpp
Efficiency	V_{in} = 110 VAC, V_o = 5.2 V, I_o = 0.6 A V_{in} = 220 VAC, V_o = 5.2 V, I_o = 0.6 A	68% 61%

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Tips and Tricks to Build Efficient Circuits with NCP1200

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APPLICATION NOTE

Prepared by: Christophe Basso
ON Semiconductor
14, rue Paul Mesplé – BP1112 – 31035 TOULOUSE Cedex 1, France
33 (0)5 34 61 11 54
e–mail: christophe.basso@onsemi.com

Introduction

The NCP1200 easily lends itself to designing Switch–Mode Power Supplies (SMPS) in a snap–shot and its success speaks for itself. However, customers applications (and problems) are unique and often necessitate the addition of specific component arrangements around the IC. As usual, solving one particular design constraint brings another one with it, perhaps puzzling the designer even more. This application note answers typical questions that a designer can raise when starting his own system analysis, but also tries to answer some problems common to Switch–Mode Power Supply applications.

Adding an External Latching Circuit for Over Voltage Protection or Over Temperature Shutdown

When pulling NCP1200's feedback pin below the skip cycle level (pin1 voltage), output oscillations cease. If this action is accomplished through a thyristor, permanent latch–off occurs until the user cycles the Vcc down and up again by unplugging the power supply. By firing the thyristor via a zener diode connected to an auxiliary winding, an efficient Over Voltage Protection (OVP) circuit can be implemented. Figure 1 depicts the solution.

At rest, when the SMPS is properly working, Q1 and Q2 are transparent to the operations because the 10 kΩ resistors block them. As soon as the auxiliary winding level exceeds the zener voltage and fires Q2, the whole SCR turns on and via the 1N4148, pulls FB low. As a result, it immediately stops the 1200 driving pulses: the SMPS shuts off. However, the Dynamic Self–Supply (DSS) being still alive (Vcc ramps up and down between 10–12 V), the 47 kΩ resistor keeps the SCR latched despite the disappearance of the default. Once the user cycles Vcc down and up again (e.g. by unplugging the power supply from the mains outlet), the SCR de–biases and allows the 1200 to restart. Q1/Q2 could be ON Semiconductor dual combo bipolar MMBT3946DW. If for transformer noise reasons Vpin1 is much lower than its default value (1.4 V), a BAT54 must be wired in place of the 1N4148 to ensure that FB passes well below Vpin1: $Q2\_Vce_{sat}$ + Vf < Vpin1. Increasing the value of the 47 k will change the total latch–off behavior into auto–recovery mode, as the default over current protection does.

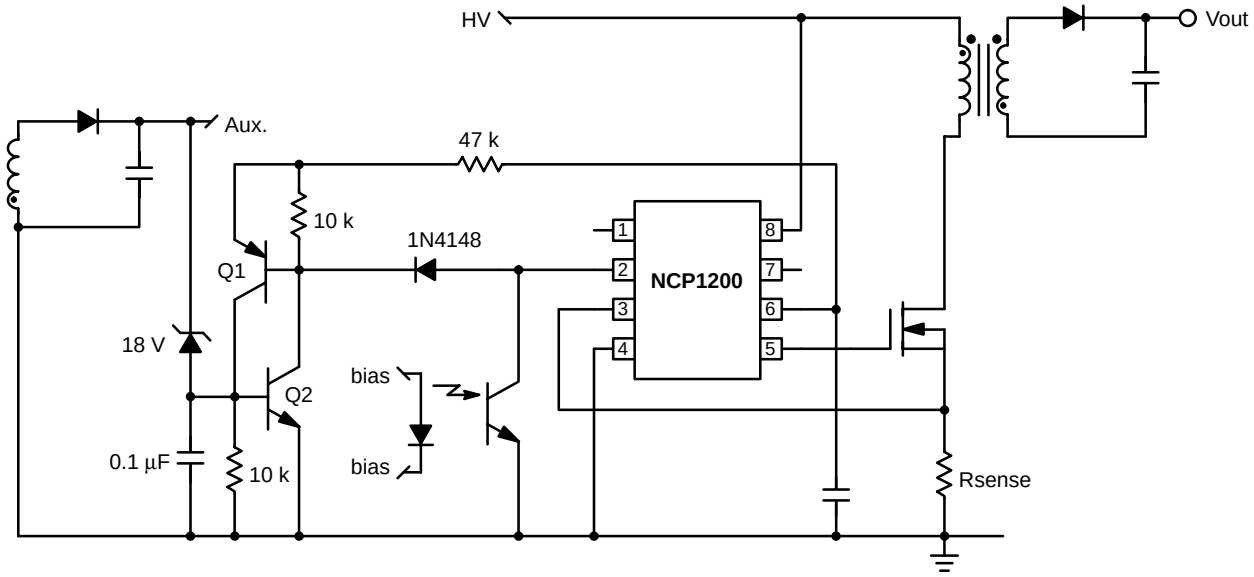

Figure 1. A Dual–Transistor Arrangement Latches–Off the NCP1200 in Case of an OVP Event

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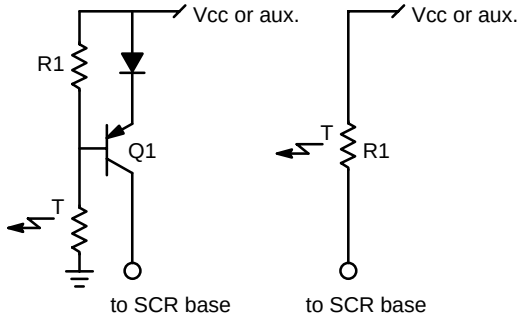

Figure 2. A NTC and a Simple PNP Make an Easy–to–Build Thermal Sensor Which Fires the SCR

A temperature shutdown can be realized on top of the above SCR by adding a PNP, as portrayed by Figure 2. The Negative Temperature Coefficient sensor (NTC) is selected to pull the PNP's base toward ground at the wanted shutdown level. To obtain slightly more dynamic on the base level, a simple diode is inserted in series with the emitter. A more economic solution involves a single thermistor, also shown on the same picture.

Driving Big Gate–Charge MOSFETs

What actually limits the NCP1200 drive capability is the DSS and not its driver stage. The driver output connects a 40 Ω resistor between Vcc and gate (see 1200 data sheet) during the ON state whereas a 12 Ω is connected in the discharge path (OFF time). If the MOSFET exhibits a large total gate charge Qg, turn–on and turn–off times will be longer but it will properly work, probably generating high switching losses. Problems usually arise because those big MOSFETs heavily load the DSS and it is important to assess the total current consumption in worse conditions. This total consumption can be evaluated through the following formula: Itotal = Icc1 + $Fswitching_{max}$ x Qg_{max}. Suppose that we use a 3 A MOSFET affected by a 25 nC Qg, then the total average current that the DSS must deliver is: 750 μA + 72 k x 25 n = 2.5 mA, if you would select a P60 version. The DSS current is 4 mA @ Tj = 25°C. However, when supplied by the high–voltage rail, the junction temperature will quickly rise, lowering the DSS capability to its minimum value stated in the data–sheet. This value being 2.8 mA @ Tj = 125°C, care must be taken that Tj stays lower than this number to ensure adequate safety margin. Needless to say that the DIP8 option offering much better thermal specs compared to SO–8, it will be preferred in high Qg applications. A good news is that the internal NCP1200 consumption significantly reduces with temperature (see characterization curves in the data sheet) and consequently eases the DSS.

Now suppose that you would like to drive big MOSFETs, featuring large Qg e.g. 60 nC or even 100 nC. It becomes impossible to use the DSS. Should you try, you would observe a Vcc that immediately collapses below 10 V after turn–on: all the current the DSS delivers is eaten by the MOSFET driving. Even if this poor situation would work, you would not be able to sense a short–circuit anymore because the function is activated only if the Vcc goes up and down, e.g. between VccOFF and VccON. As a result, using an auxiliary winding becomes the only solution. However, we will see below that the aux. winding can degrade the Over Current Protection (OCP) trip point. Figure 3 offers an interesting intermediate solution where the aux. winding plays an important role but does not bother the DSS operation, keeping the precise OCP trip point intact.

In this example, Q1 buffers the drive output and the energy necessary to drive the big MOSFET is derived from the auxiliary winding. At power–on, the DSS charges both capacitors, Caux and CVcc which are isolated by D1 as soon as the auxiliary voltage has built up above the NCP1200 VccON level. The drive current passes through Q1 and the 1200 delivers a small current to bias its base. At the opposite, D3 routes the gate current inside the 1200 as usual. A resistance can be inserted between the emitter and the gate to slow–down the turn–on transition. The no–load standby performance is better than without auxiliary winding because the only current seen by the DSS is roughly Icc1 which is low. Figure 3 clearly allows the NCP1200 to build SMPS of any output power levels, Flyback or Forward.

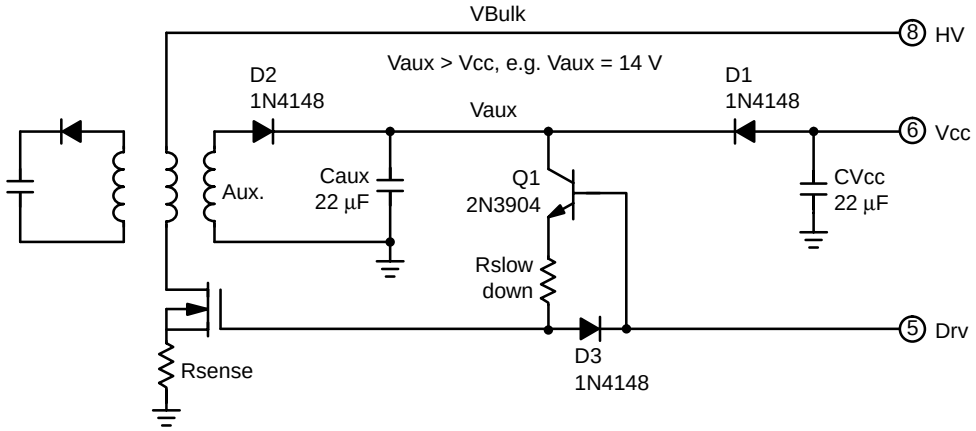

Figure 3. By Taking the Energy from the Auxiliary Winding Only at Turn–On, DSS Operation Is Not Bothered and IC Consumption Is Kept Within Safe Limits

Reducing the Standby Power with an Auxiliary Winding that Disables the DSS Operation

In certain applications, a low standby power is mandatory. This option clearly prevents from using the DSS because the 1200 supply would be the most consuming portion of the SMPS in no–load conditions. To stop the DSS, an external voltage must force the 1200 Vcc to be permanently above VccON or 11 V as given in the data sheet. Failure to reach that level would imply a DSS re–activation with all the losses in standby. Wiring the auxiliary winding with skip–cycle components can be a little tricky, especially if you target an extremely low standby power. Why? Because in standby, the pulses are not a continuous flow but a short burst whose recurrence can be as low as several tens of milli–seconds (skip cycle technique). Provided your auxiliary circuit exhibits some losses, you will not be able to maintain a self–supply above 11 V, re–activating the DSS again. Another problem takes place: the primary to secondary leakage inductance. This inductance generates a spike detected by the auxiliary diode which artificially raises the auxiliary voltage (Figure 4 with arbitrary levels). This effect can accidentally destroy the 1200 but also deteriorate the OCP detection point.

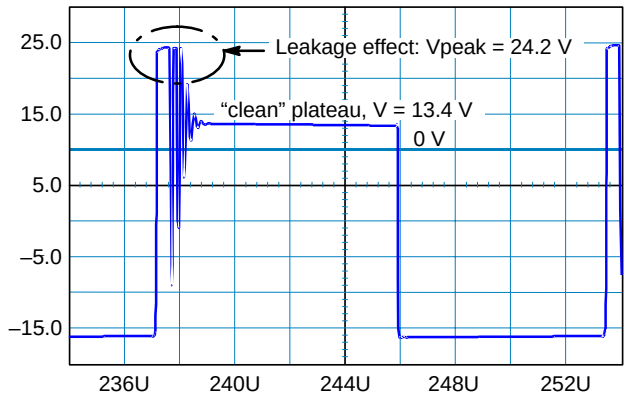

Figure 4. The Leakage Effect Seen on the Auxiliary Side Pulls–Up the Final Level Peak–Rectified by the Diode

As the NCP1200 Vcc cannot exceed 16 V, care must be taken at the design stage to limit the voltage excursion while running nominal load. A good solution would be to first integrate the leakage spike and then rectify the wave with a diode as Figure 5 suggests. Unfortunately, in standby, the auxiliary level would collapse because the burst energy is so low that the 22 Ω would dramatically limit the 22 µF re–fuelling current. We will exploit this feature in a later application.

The solution consists in splitting the rectifying section in two blocks, the second one clamping Vcc below 16 V. This solution is depicted by Figure 6. The BAT54 is only here to avoid hampering the startup time by charging two capacitors together. If this is not a problem, you can simply omit it. The zener voltage can be lowered but the maximum VccOFF (12.5 V) must be reached otherwise the 1200 won’t startup.

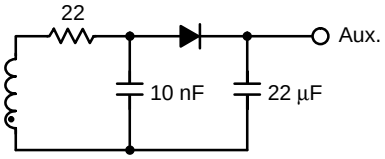

Figure 5. A Resistor and a Capacitor Can Integrate the Perfidious Leakage Inductance

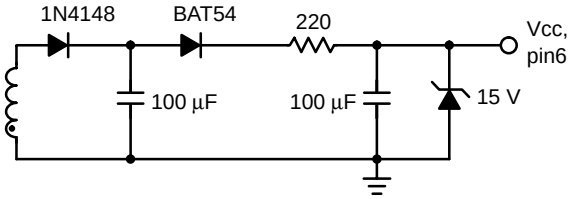

Figure 6. This Configuration Ensures Self–Supply in Standby and Prevents Vcc from Exceeding the 16 V Maximum Rating

Using an auxiliary winding as wired according to Figure 6 offers true short–circuit protection but the precise over load mode detection brought by the DSS is lost. This is imputed to the primary leakage inductance, which in some cases is so energetic, that a short on the secondary power winding cannot drop the auxiliary winding, preventing short–circuit detection. Reducing the primary clamp level (via the RCD network) represents a good solution, but to the detriment of the efficiency. If this is a problem in your application, below are other solutions keeping all the 1200 goodies with an auxiliary winding.

A 70 W demo board was built using an auxiliary supply and revealed less than 100 mW standby power at 350 VDC input level.

Using Auxiliary Winding Without Affecting the OCP Trip Point, but Disabling the DSS

One great aspect of the DSS, is the fact that the OCP circuitry is activated whatever the auxiliary voltage is, because it does not use any! In low standby power applications, you will need to wire an auxiliary winding to permanently disconnect the DSS. Unfortunately, the 1200 internal OCP circuitry activates when Vcc crosses VccON (≈ 10 V) while going down. This action naturally takes place with the DSS, but if you wire an auxiliary winding, it just disappears because you managed to keep Vaux above 10 V to invalidate the DSS. As a result, if you overload the output, NCP1200 will activate its burst only when the auxiliary Vcc collapses below 10 V. And what happens if you have a poor coupling between the windings and a large primary leakage inductance (see Figure 4)? You never detect the OCP.

We have seen that the leakage inductance generates an energetic spike that couples to the auxiliary winding. Why not sampling the auxiliary voltage on the plateau, a short time further to the leakage appearance? This is exactly what Figure 7 circuit does for you.

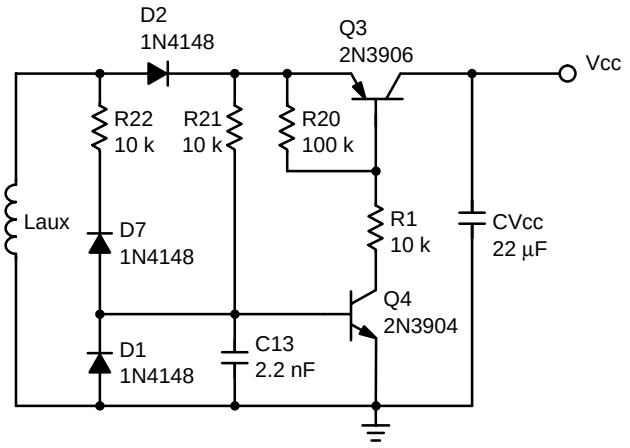

Figure 7. The Delay Introduced by Q4 Samples Right After the Leakage and You Obtain a Nice DC Voltage

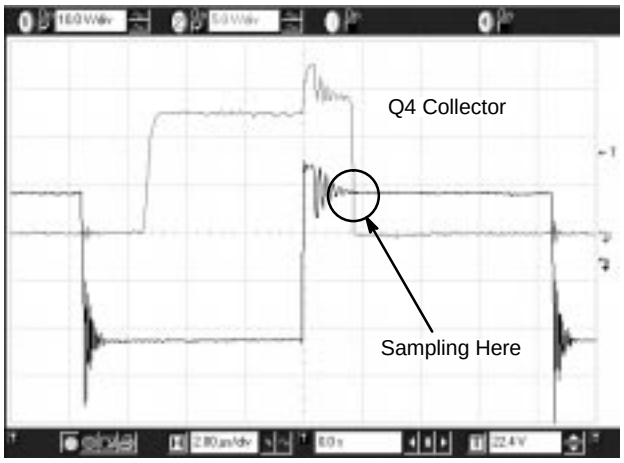

Figure 8. By Delaying the Sampling Time,You Obtain a Clean Auxiliary Level Without Any Leakage Effect

When the main power switch is ON, capacitor C13 is discharged through R22 and D7 whereas D1 avoids a deep reverse bias of Q4 base–emitter junction. When the main switch opens, the secondary voltage sharply rises and node 1 becomes positive. However, C13 being discharged, Q3 stays open and Vcc does not grow up. After a short period of time (adjustable through R21 or C13), Q4 closes and brings Q3's base closer to ground. Vcc now goes up and catches up node 2 level, minus Q3's Vce sat. If the time delay is correctly selected, Vcc is absolutely clean from any voltage spike because you have sampled the plateau.

Figure 8 details the scope shot obtained using this circuit. As you can see, the sampling time occurs right after the leakage and the auxiliary level extracted from this plateau is clean. This solution can also be very useful in application where precise primary regulation is needed.

With this solution, the off–time is truncated to avoid the leakage effect. In standby, when skip cycle takes over, this off–time is considerably reduced and our delay circuit loses quite a bit of precious energy: the auxiliary winding collapses and cannot self–supply anymore the 1200. To combine the advantages of a clean self–supply (remember, to get a precise overcurrent trip point or a good primary regulation level if any) together with excellent standby power performance, Figure 9 offers an interesting solution. The schematic becomes more complicated but has been tested fine.

Q1 and Q2 perform their duty as described above but when voltage is present over C2, Q3 is biased and keeps D8's anode low enough to block it. When the supply enters standby, C2's level goes low and unleashes Q3 which can now let the current flow through D8, keeping 1200 self–supplied in standby. As soon as the load comes back, Q3 closes again and C2 recovers its role.

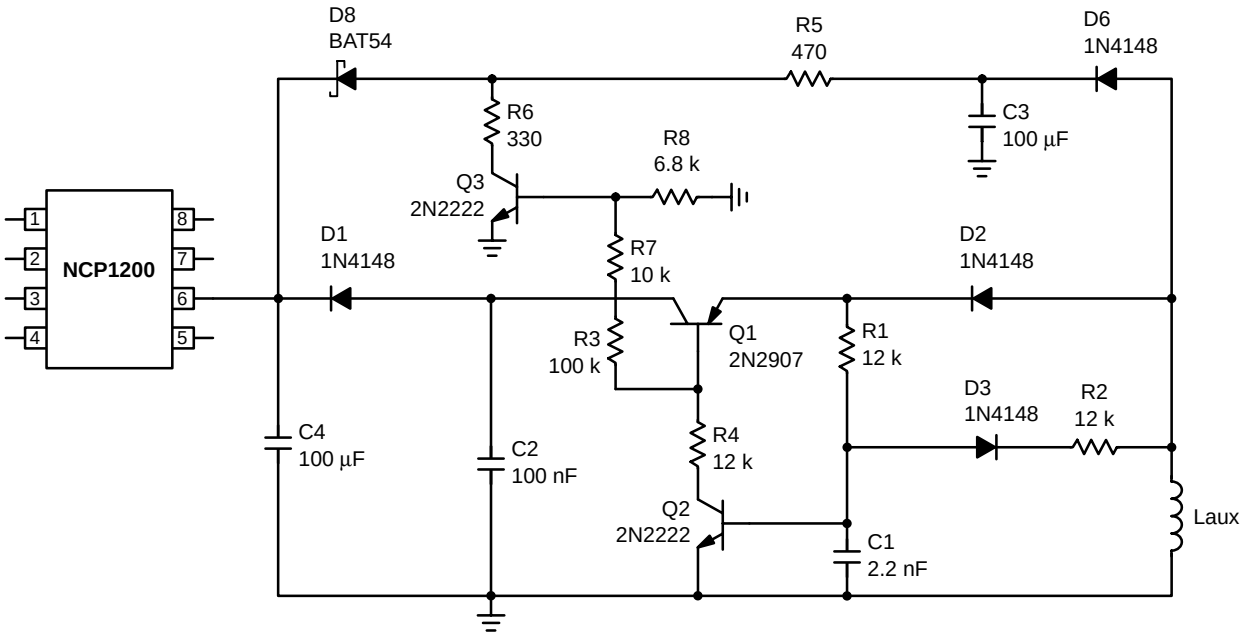

Figure 9. A Shunt Prevents the Auxiliary Level to Supply the 1200 in Normal Operation But Becomes Active in Standby

Using Auxiliary Winding Without Affecting the OCP Trip Point and Keeping the DSS Working

The DSS offers a very interesting feature which is the ability to implement true overload detection. Standard UC384X–based systems are usually built with an auxiliary winding but because of the poor cross–regulation between the windings, it is almost impossible to implement a precise over load protection. However, these systems can usually cope with short–circuit constraints because the auxiliary winding finally collapses when Vout equals zero. (See Figure 4 to see who is guilty.) As such, the DSS is a very desirable choice when true over load protection is required by the customer. Unfortunately, in no–load conditions, the DSS being connected to the high–voltage rail, you directly measure this power consumption on the input, despite the low current consumption of the 1200. In some very stringent standby power requirements, you simply cannot accept these losses. Figure 10 presents a solution built on top of that presented in Figure 3.

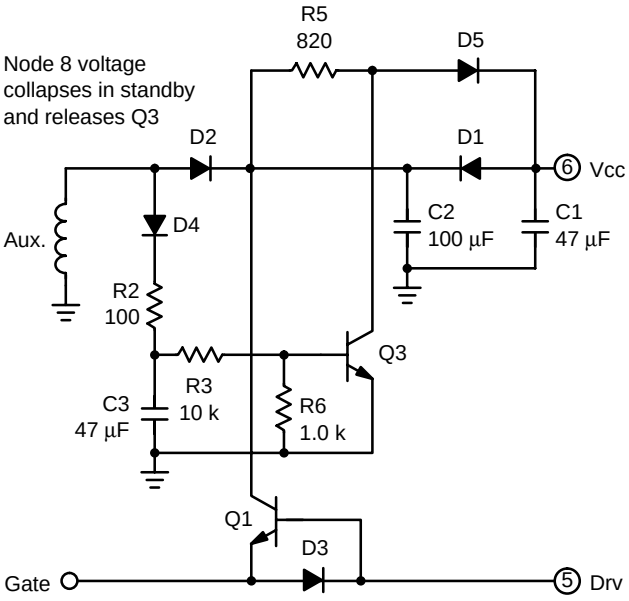

Figure 10. This Solution Upgrades Figure 3 Option by Disabling the DSS in Standby

The trick used to detect the standby or no–load condition, is to take benefit from the the weak energetic content of the burst pulses when the supply operates in standby. That is to say, if the refueling current circulating through D4 is diminished by a resistor (R2), then C3 will never be able to maintain a normal operating voltage (e.g. as the one at nominal load) and it we be severely reduced. In the example, we measured 15 V in normal load, and less than 3 V in standby. In normal operation, C3's voltage is high enough to forward bias Q3 via R3/R6. His collector pulling R5 terminal to ground, D5 is naturally blocked and the DSS plays its role: precise over load mode detection, and EMI jittering through its ripple. When the SMPS goes to standby, C3's level decreases until Q3 gets un–biased. Its collector no longer pulls R5 to the ground and D5 can pass all the auxiliary level developed across C2 to block the DSS. R5 value can be adjusted to avoid too much of wasted power as long as D5 stays blocked in nominal load operations. The standby power becomes as good as stated before: less than 100mW at high line. Thanks to this latest solution, you can:

- Drive the MOSFET of your choice: all the ON current is drawn from the auxiliary winding.
- Benefit from the DSS activity to build a precise over current detection and use its ripple for EMI jittering.
- Disable the DSS in no–load conditions and obtain one of the best standby power on the market.

Inserting a Resistor with Pin8 to Avoid Over–Dissipation of the Package

Some users like to use the SO–8 package mainly because of its small size. Unfortunately, the thermal resistance junction–to–ambient makes the exercise difficult because the DSS naturally dissipates heat (except if use some alternative solution as depicted below). The auxiliary winding option is still possible, but the best Over Current Protection (OCP) trip point is obtained with the DSS. The DSS being active, there is no other alternative than dissipating this heat through copper, or, move it to another component, e.g. a series resistor. By inserting a resistive element in series with pin8, every time the DSS turns on, you drop some voltage across the resistor (Figure 11) . You thus spread the total power between two components instead of one, lowering NCP1200 Tj inside the SO–8 package. The calculation is easy. You know by the data sheet that every time the DSS turns on, 4 mA flow inside pin8 at steady–state. If one keeps about 50 V minimum on pin8 to properly operate the DSS, the resistor value can be calculated through:

$$Rdrop \; - \; \frac{Vbulk\,min \times 50}{4\ m}$$

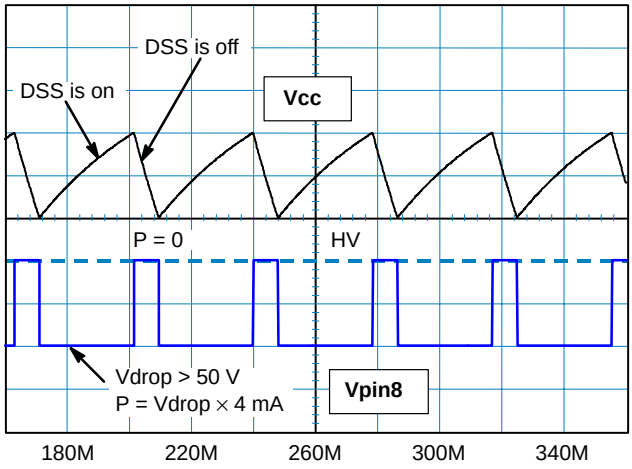

Figure 11. By Inserting a Resistor with Pin8, You Can Split the Power Between an Active and a Passive Component in Order to Keep Tj Lower

Below are two examples showing the benefits of inserting the resistor.

Case 1:

Single mains, 230 VAC ± 15%, NCP1200 average consumption is around 2.5 mA. DSS duty–cycle is 62%. Vbulk max = 374 VDC and Vbulk min = 276 VDC. Rseries = (276 – 50)/4 m = 56 kΩ.

1. Without the resistor, NCP1200 would dissipate (worse case): 374 x 2.5 m = 935 mW, incompatible with the SO–8. With an RtetaJA of 100°C/W, the maximum power the NCP1200D version can handle at an ambient of 40°C is: 125°C – 40°C/100 = 850 mW
2. By inserting the 56 kΩ resistor, we drop 56 k x 4 m = 224 V during the DSS activation. The power dissipated by the NCP1200 is therefore: Pinstant x DSS duty–cycle = (374 – 224) x 4 m x 0.62 = 372 mW. We can pass the limit and the resistor will dissipate 935 – 372 = 563 mW.

Case 2:

Universal mains, 90 – 27 5VAC, NCP1200 average consumption is around 2.5 mA. DSS duty–cycle is 62%. Vbulk max = 388 VDC and Vbulk min = 127 VDC. Rseries = (127 – 50)/4m = 19 kΩ.

1. Without the resistor, NCP1200 would dissipate (worse case): 388 x 2.5 m = 970 mW, incompatible with the SO–8.
2. By inserting the 19 kΩ resistor, we drop 19 k x 4 m = 76 V during the DSS activation. The power dissipated by the NCP1200 is therefore: Pinstant x DSS duty–cycle = (388 – 76) x 4 m x 0.62 = 773 mW. We can pass the limit and the resistor will dissipate 970 – 773 = 197 mW.

“When I Insert a Resistor in the Gate of My MOSFET, the Supply Becomes Instable”

The Leading Edge Blanking (LEB) circuitry has the role to clean the voltage appearing across the sense resistor. By discharging all the parasitic capacitors at turn–on, you create a current spike that can engender false tripping of the current comparator. To avoid this problem, NCP1200 includes a LEB calibrated at 250 ns. The LEB starts to blank the current sense information as soon as the driver goes high. Figure 12 displays the drive and gate signals when a resistor inserted between gate and driver is small. This represents a normal operating conditions where the gate follows the driver. However, inserting a larger resistor in series with the gate is a common practice when one wants to slow down the main switch, e.g. for EMI reasons. Unfortunately, the resistor delays the turn–on of the MOSFET and truncates the Leading Edge Blanking (LEB) which no longer plays its role (Figure 13). In that case, false triggers occur and instabilities takes place. The cure consists in adding an RC network between Rsense and the current sense pin (Figure 14).

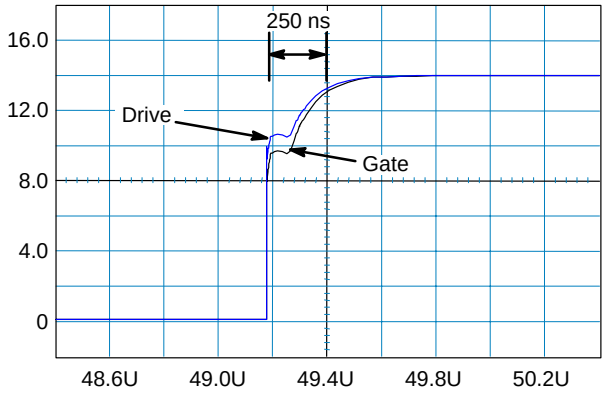

Figure 12. When the Gate Follows the Drive, the LEB Works Fine

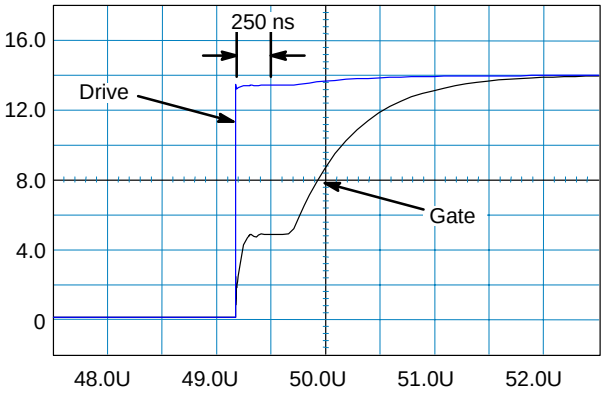

Figure 13. Delaying the Gate–Source Signal Produces the Effect of Truncating the LEB

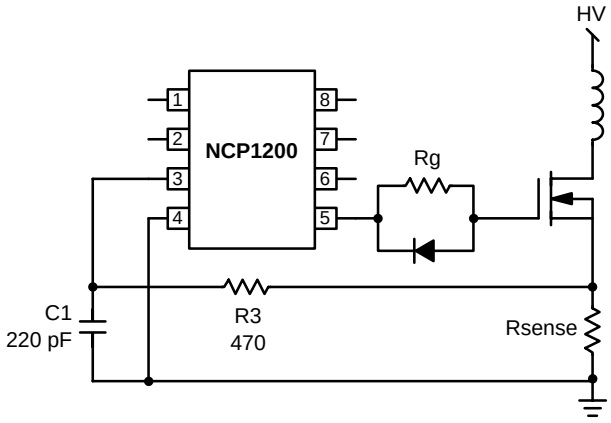

Figure 14. This Network Re–Enforces the LEB Action by Integrating the Sense Signal Whatever the Gate Delay

“What MOSFET’s Size Can I Drive in Half–Wave Configuration?”

In some of the available application notes, we propose to wire pin8 not to the bulk capacitor but to the rectifying half–wave. This solution is acceptable for low gate–charge MOSFETs only, because the DSS current capability is

divided by two in average (half–wave duty–cycle is around 50%). As a result, the DSS can only deliver 2 mA DC which divides between the controller (Icc1) and the driver consumption, utilized to charge up the MOSFET's Qg. If we take the very worse case that appears at high temperature, the DSS minimum current is 2.8 mA which divided by two makes 1.4 mA. Removing Icc1 (≈750 μA, this number goes down when Tj goes up), we have 650 μA with 100 μA left to charge the Vcc capacitor. As a result, with a 60 kHz version, the maximum Qg would be: 550 μA/60 k = 9 nC. This corresponds to a 1 A MOSFET or a 2 A MOSFET featuring low gate charge only. If you wire a bigger MOSFET, Vcc will collapse without the classical ripple 2 V due to the DSS operation. No ripple means no OCP because the 10 V error flag test has gone. (See application note AND8023/D for more detailed explanation.) In summary, we recommend half–wave operation only in configurations that guarantee proper DSS operation at any temperature.

"I Have Routed My 1200 with a Large Copper Area Around the Package. What Power Can I Dissipate?"

The maximum power accepted by the NCP1200 is given by:

$$Pmax + \frac{Tj\,max \times Tamb\,max}{R\theta J \times A}$$

As you can see, you could define yourself two parameters in the formula: Tj*max* given by the data sheet, or the maximum operating temperature your Quality Department fixes, and finally Tamb*max*, given by your application. Unfortunately, you cannot determine RθJ–A because the copper area you added has actually changed it from the original data sheet specification. The best is to measure it with a simple method that has proven to be accurate enough for our purposes. First, you need a bare PCB featuring the copper area you have routed. It can be your final board without anything soldered on it. Then, you solder the NCP1200 (DIP8 or SO, depending on your selection) directly on the copper (please, without a socket). Once this is done, we need to find a Temperature Sensitive Parameter (TSP) to evaluate the junction temperature inside the package. One of the internal ESD zener diode represents a good choice. Before using it, we must calibrate it. Several solutions exist but the easiest one is to take a multi–meter in diode position offering sufficient resolution (3 or 4 digits are ok) and current stability during the measurement. The Agilent HP34401A can be a possible selection. The ESD diode connected to pin1 can be used but another one could also be wired, e.g. the current sense pin. Now, bias it in forward mode by connecting probe + to the ground and probe – to pin 1. At an ambient of 25°C, you should read something like Vf ≈ 720 mV. The rest of the operation requires a precisely controlled heater to calibrate our junction. Put the NCP1200 under the heater's bell and measure the Vf at different points, e.g. every 10°C. At every step, wait at least a few minutes that the reading stabilizes before recording the point. If everything goes well, you should obtain a linear graph as Figure 15 shows.

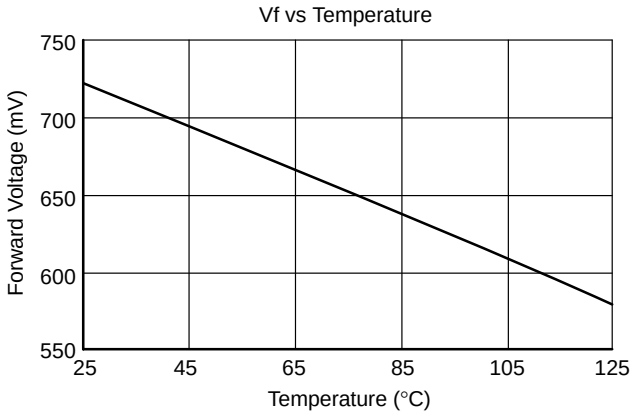

Figure 15. Collecting Data Points and Feeding a Spreadsheet Unveils the ESD Junction Temperature Behavior

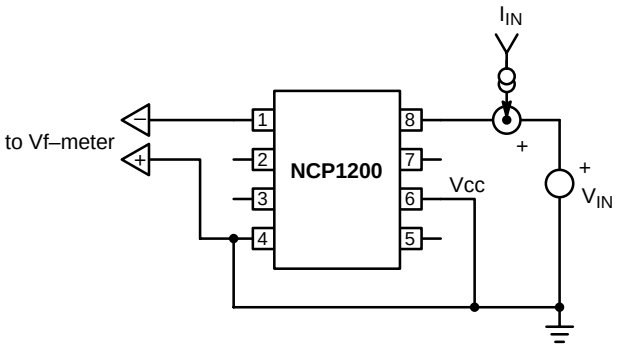

Figure 16. Next Step Is to Inject Power Into the Chip

With that graph on hand, we can now start measuring our RθJ–A. On the same PCB board, make a short between Vcc and ground, leave all the other pin open but keep the Vf–meter connected. Do not bring too much of solder on the joints to be in same final industrial conditions (for instance wave soldering). Now, bring a DC source to pin8, normal polarity, that is to say, pin8 positive by respect to ground. Figure 16 shows the wiring diagram for best understanding where an ampere–meter has been inserted. Immerse all the 1200 PCB test fixture into an hermetic oven and select the ambient temperature at let's say 40°C. Turn the DC power supply on and start to increase the voltage. At a certain moment, the DSS turns on and the ampere–meter indicates a current. Increase the voltage until you reach a power value of 300 mW roughly (V_in x I_in). Leave everything cooking for a while, until the Vf reading stabilizes. You will note that the current goes down a bit because of the DSS thermal effect (actually self–protective). After time has elapsed, suppose that you read Vf = 652 mV and Ptotal = 280 mW. From Figure 15, we extract the corresponding junction temperature given by our calibrated TSP: 652 mV → Tj ≈ 75°C. From these numbers, we are able to calculate our thermal resistance junction–to–ambient resistor by:

$$R\theta J \times A + \frac{Tj \times Tamb}{Ptotal}$$

which turns to be 125°C/W. A few remarks concerning the measure:

- Use a well temperature–controlled oven. Failure to stabilize the temperature in a quiet environment will engender large errors.
- Wait that the part has stopped its temperature excursion before taking the Vf point. DIP8 packages require longer time than SO–8.

“What Power Level Can I Expect from the NCP1200?”

The NCP1200 being a general purpose current–mode controller, you can virtually use it in any applications ranging from a few hundred of mW up to 100 W or more! The above design ideas will let you implement the solution best adapted to your application. The limiting factor is actually the power switch and the 1200 driving capability. In the simplest application schematic (no aux. winding) with the DSS working and a 3 A MOSFET featuring low gate charge, we have successfully built a 70 W universal mains application board exhibiting 81% efficiency at low line and 87% at high line. Associating an auxiliary winding and a single or dual bipolar stage (as described in the data sheet) will let you drive the MOSFET of your choice, e.g. a 10 A device, reducing the conduction losses and the heatsink size.

EBNCP1200/D

How to Use the Spreadsheet NCP1200 Discont.xls

By Hector NG
ON Semiconductor Singapore
Application Engineer
Email: hector.ng@onsemi.com

ON Semiconductor™

http://onsemi.com

ENGINEERING BULLETIN

This short note describes the necessary steps to efficiently use the NCP1200 design aid file: “NCP1200 Discont.xls”.

Symbol	Cell in Spreadsheet	Explanation	Remarks
V_{max}	B4	Maximum AC Input Voltage in volt	
V_{min}	B5	Minimum AC Input Voltage in volt	
F_{line}	B6	AC Line Frequency in Hz	
V_o	B11	Output Voltage in volt	
I_o	B12	Maximum Output Current in ampere	
h	B13	Efficiency in %	Assume 80% if unknown
V_{bd}	B14	Power MOSFET breakdown voltage in volt	
V_d	B16	Diode voltage drop in volt	Assume 1.0 V if an ultra–fast diode is used or 0.8 V if a Schottky diode is used

Step 1: Input System Parameters

The first step in power supply design is to understand the system requirements. The following parameters have to be entered into the spreadsheet.

Step 2: Enter Capacitance of Input Filter Capacitor C_{in}

Enter the capacitance value of the input filter capacitor into cell B39 in mF. A recommended capacitance value is shown in cell B38.

Step 3: Determine Primary Inductance

A list box is shown in the spreadsheet which labelled as “Selected Device” – Cell G12. Choose a device which you plan to use from the list. NCP1200 is offered in 40 KHz, 60 KHz and 100 KHz versions. Then the user can set the primary inductance by inputting a value in cell B32. A recommended L_p is shown in cell B31 for the user reference. Depending on the application, the choice of Lp can have a significant noise impact during NCP1200 skip cycle operation. Low Lp implies high peak currents (with possible noise problems in standby) while a high Lp implies low peak current (less noise problems) but possibly a higher leakage inductance. A trade–off has thus to be found between all the design requirements.

Step 4: Enter Current Density Allowed for the Transformer

The wire size of a transformer has to be chosen suitably to avoid excessive copper loss and heat dissipation. The current density of the wire selected should be in the range of 3 ~ 5 A/mm^2 for natural cooling system and current density can be increased to 4 ~ 7 A/mm^2 for fan cooled system. This value should be entered into cell B55.

Step 5: Determine Maximum Wire Size

Select the maximum wire size for the transformer in the list box in cell G53. The program will limit itself in choosing which wire size for primary and secondary winding with this information.

Step 6: Enter Flux Density Safety Factor

Flux density safety factor determines the magnetizing level of the transformer core, it should in the range from 0.3 to 0.5 Tesla. Enter this value in cell B58.

Step 7: Enter Bobbin Usage Factor

In a transformer bobbin, not all cross sectional area is available to accommodate the windings. A bobbin usage factor is introduced to account for area occupied by margin, insulation tape and waste space between wires. It should be in the range from 0.3 to 0.5. Enter this value in cell B59.

Step 8: Enter Magnetic Core and Bobbin Data

Before we can proceed further, we must have the information of different magnetic cores and bobbins ready. Recommended core types are EE, EI, EF and ETD made of material that can work in the selected switching frequency without excessive hysteresis loss, e.g. N67 from Epcos (Siemens) and PC40 from TDK. The worksheet allows user to input properties of 5 material simultaneously. From the data book of the magnetics, locate the following date and enter into cell B61 to F64.

Symbol	Cell in Spreadsheet	Explanation	Remarks
Core Name	B61–F61	Name of the magnetic core	Optional data, not for calculation For identification purpose only
Ae	B62–F62	Effective area of the magnetic core in mm^2	Property of the magnetic core
Bsat	B63–F63	Saturation magnetic flux density at 25^oC in Tesla	Property of the magnetic material
Aw	B64–F64	Bobbin window area in mm^2	Property of the bobbin, some vendors provide several bobbins for one magnetic core

Step 9: Enter $R_{DS(on)}$ of the Power MOSFET

The spreadsheet provides additional information on maximum conduction loss of the power MOSFET. Enter maximum $R_{DS(on)}$ (usually @T_j = 100°C) of the selected power MOSFET in cell B34, maximum conduction loss is shown in cell B35.

Step 10: Determine the Sensing Resistor

It is normal for a transformer to have 10% tolerance in its primary inductance. Enter the percentage tolerance in cell B82. The spreadsheet uses the lowest primary inductance and lowest switching frequency to compute worst case primary peak current. Maximum allowable sensing resistance is calculated based on this information and it is shown in cell B86. Select a sensing resistor with value lower than B86 and enter into B87. Please pick a value within the E24 series for easier selection: 0.56 Ω, 0.68 Ω, 0.82 Ω, 1.0 Ω, 1.2 Ω, 1.5 Ω, 1.8 Ω, 2.2 Ω, 2.7 Ω, 3.3 Ω, 3.9 Ω, 4.7 Ω.

Step 11: Final Review

Before finalizing on the design, one has to review the calculation results.

a. Maximum turn on duty, D_{max}:
   D_{max} (cell B25) should be kept below the maximum turn on duty of NCP1200. Referring to NCP1200 data sheet, typical $D_{(max)}$ is at 80%. However, it is not realistic to push D_{max} to the limit of the control IC because the secondary peak current will be very high and there is no room for transient response. Ideally D_{max} should be kept at 40% to 60% so that there is reasonable balance on primary and secondary ripple current. Decrease L_p if D_{max} is too high.
b. Maximum voltage across power switch circuit, $V_{pwr\_sw(max)}$:
   Make sure that this value (cell B23) does not exceed power MOSFET breakdown voltage. Decrease L_p if $V_{pwr\_sw(max)}$ is too high. In fact, we must have headroom to cater for voltage spike generated by the leakage inductance of the transformer.
c. Magnetic flux density during start–up, B_{init}:
   To avoid magnetic saturation during start–up, B_{init} (cell B88) should be kept below 70% of B_{sat}. If B_{init} is too high, first attempt to reduce B_{init} should be by increasing the value of the sensing resistor R_{sense}. If R_{sense} is already very close to its allowable maximum value, try lowering the value of flux density safety factor (cell B58). This may force you to change to a bigger magnetic core.

Step 12: Reading Results

Results are summarized in the Results page. Select magnetic core/bobbin set to use by list box in cell G6. User should take note whether cell C11 is showing “OK” or “not OK”. Cell showing “OK” implies that the corresponding magnetic core/bobbin set is big enough to accommodate all windings. The information is for reference only, consult your transformer vendor for a conclusive answer.

NCP1200 versus UC384X

Feature	NCP1200	UC384X
IC supply	**Thanks to the Dynamic Self Supply feature (DSS):** • **No need** of power resistors at startup • In operating mode: **No need** of auxiliary winding + rectifying diode ⇒ Cost effective ⇒ PCB space saving ⇒ Increase of Efficiency	• Need of Power resistors at startup. • In operating mode: need of auxiliary winding + rectifying diode + capacitor ⇒ Additional cost ⇒ PCB space consuming ⇒ Useless power dissipation ⇒ Reliability issues
Switching frequency	**Internally Fixed at 40 kHz, 60 kHz and 100 kHz** ⇒ Cost effective ⇒ PCB space saving	**Externally fixed by a resistor and a capacitor** ⇒ Additional cost ⇒ PCB space consuming ⇒ Reliability issues

NCP1200 versus UC384X

Feature	NCP1200	UC384X
EMI behavior	**Built–in Frequency Jittering for Lower EMI.** ⇒ Cost effective ⇒ PCB space saving ⇒ Increase of Efficiency	**External components (resistor + capacitor) needed to slow down MOSFET switching-on in order to lower EMI.** ⇒ Additional cost ⇒ PCB room consuming ⇒ Lower efficiency
Safety, Fault conditions	**Internal Output Short–Circuit Protection:** Dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty–cycle. ⇒ Cost effective ⇒ PCB space saving ⇒ Auto-recovery ⇒ Predictable behavior **Internal Temperature Shutdown** Fault condition will not destroy the IC	**Cycle-by-cycle current limiting:** With low voltage outputs, IC may not see the overload ⇒ extra components are needed: fuse or transistors to monitor feedback level. ⇒ Additional cost ⇒ PCB space consuming ⇒ No auto-recovery **No Internal Temperature Shutdown** Fault condition can destroy the IC

NCP1200 versus UC384X

Feature	NCP1200	UC384X
No load, Standby Mode behavior	**Skipping Cycle Mode (Automatic Standby Mode):** NCP1200 automatically skips switching cycles when output power demand drops below a given level. ⇒ **Energy Saving** ⇒ Cost effective ⇒ PCB space saving ⇒ High efficiency ⇒ Adjustable level ⇒ No acoustic noise (low peak current) ⇒ Predictable behavior	**No Skipping Cycle Mode (NO Standby Mode):** IC is not designed to work in Burst mode. Extra components are needed to achieve it. ⇒ **Energy waste** ⇒ Additional cost ⇒ PCB space consuming ⇒ Low efficiency (start-up resistors will always dissipate and waste power) ⇒ Possible acoustic noise ⇒ Reliability issues

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