V$_R$ Series™ 64-Bit Processors
Development Tools Catalog

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April 2000

Dear NEC VR Series™ Customer:

Welcome to the April 2000 edition of the VR Series Development Tools Catalog. In this new issue, we have added six new tools vendors and twenty-five new products. NEC Electronics is continuing to make sure that you are provided with a broad and highly efficient tools environment. Our alliance with many of the most popular vendors has assured you of multiple options for compilers, real-time operating systems, reference boards, and software support, among others.

We know today that time-to-market pressures and "getting it right—the first time" can mean the difference in marketing a competitive product to specification and within ever-shrinking market windows. Our approach is to provide comprehensive solutions: a full range of feature-rich processors, companion chipsets, vertical market expertise, and a seamless development environment to aid your design programs.

Please review the leading-edge tools described in the following sections. Our tools partners have worked hard to anticipate your needs, not just for today but for well into the future, so that the power of the VR Series MIPS® RISC architecture will grow with you. From the low-power VR4100™ family to the mid-range VR4300™ family (a version of which was introduced in the Nintendo™ Ultra 64™ game) to the high-end VR5000™ and VR5400™ family, NEC's VR Series offers the industry's widest selection of 64-bit processors today.

We would appreciate your suggestions as to how we may continue to improve our service to you and that of our tools partners.

Sincerely,

NEC VR Series RISC Products Group

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Vʀ Series Microprocessors

VR4121
64-Bit MIPS RISC
Microprocessor

Salient Features

◗ VR4120™ CPU running at 168 MHz (210 Dhrystone MIPS) with memory management unit

◗ MIPS I, II, III, and MIPS 16 instruction set compatible

◗ Single-cycle 32-bit MAC instruction for DSP operations

◗ 16 KB instruction cache, 8 KB data cache

◗ Power management unit with four modes

◗ Interrupt control unit and DMA controller

◗ Real-time clock with four built-in timers

◗ 16550 serial interface with separate debug port

◗ Fast infrared interface up to 4 Mbps

◗ Keyboard, touch-panel, and LED interface controller

◗ 10-bit D/A and A/D converters

◗ Host signal processing unit for software modem interface

◗ 385-mW typical power consumption at 168 MHz

◗ Operating voltage: 2.5 V core, 3.3 V I/O

◗ 224-pin FPBGA package

Product Overview

Designed around the popular MIPS RISC architecture, the VR4121™ (µPD30121) offers excellent power consumption and performance attributes in a highly integrated, low-cost system on a chip.

This processor is the first NEC device that uses the ultra-low-power-consuming VR4120 CPU core based on advanced 0.25-micron technology. The VR4121 is compatible with the MIPS I, II, III, and MIPS 16 instruction set architectures.

The VR4121 provides an easy choice for VR4111™ customers in terms of upgrade, since the VR4121 and VR4111 are fully pin compatible. The VR4121 microprocessor's high speed, compact size, and low power consumption make it ideal for use in battery-driven, portable handheld systems.

Applications

• Handheld PCs and PDAs

• Smart phones and Internet/e-mail phones

• Personal GPS

• Battery-powered consumer embedded controllers

Ordering Information

Part Number	Package	Operating Frequency
µPD30121S1-131	224-pin FPBGA	131 MHz
µPD30121S1-168	224-pin FPBGA	168 MHz

Features

VR4120 CPU Core

• MIPS I, II, and III ISAs without FPU, LL, LLD, SC, and SCD instructions

• MIPS 16 ASE compliant for compact code density

• Five-stage pipeline running at up to 168 MHz (210 Dhrystone MIPS)

• Single-cycle 32-bit MAC instruction for DSP operations

NEC

VR4121 Block Diagram
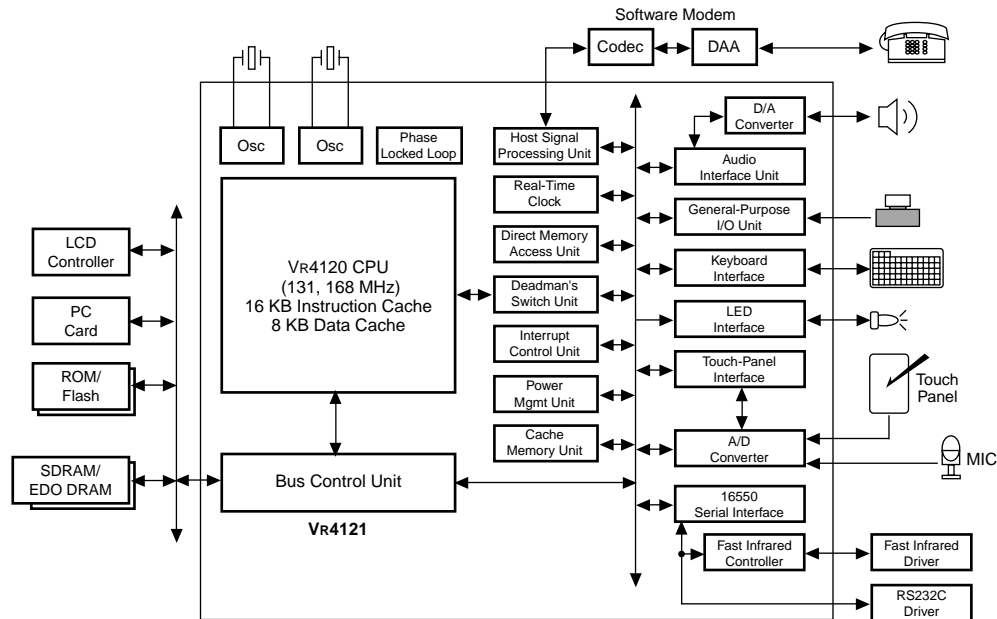
Memory Management Unit

- 32-bit physical addressing range of 4 GB with 40-bit virtual address space
- 32 double-entry TLBs supporting 1~256 KB page size
- Up to 64 MB of SDRAM/EDO/fast-page DRAM and 64 MB of SROM/flash memory/mask ROM

Cache Memory Unit

- 16 KB direct-mapped instruction cache
- 8 KB direct-mapped data cache

Bus Control Unit

- Supports 32-bit and 16-bit addressing modes
- Dynamic bus sizing supports a subset of the ISA bus

Power Management Unit

- Supports four power-saving modes: Fullspeed, Standby, Suspend, and Hibernate

Clock Generator Unit

- Built-in PLL for frequency multiplication
- External bus frequency of 16/33 MHz

Real-time Clock with Four Built-in Timers

Interrupt Control Unit

- Supports both internal and external interrupts

DMA Address Unit and DMA Control Unit

- Controls five different DMA channels

General-Purpose I/O Unit

- Controls 49 GPIO pins

Keyboard (96-key), Touch Panel, and LED Interface

10-bit A/D Converter for Touch-panel and Audio Input

Serial Interface Unit (16550 compliant)

- Supports up to 115 kbps
- Separate debugging serial port

Fast IR Unit

- Performs 0.5 to 4 Mbps IrDA 1.1 standard communication

Audio Interface Unit and 10-bit D/A Converter

- Supports audio output and microphone input sampling

Host Signal Processing Unit

- Supports data and fax software modem capabilities

AC/DC Specifications

- 168 MHz maximum frequency
- 2.5 V core and 3.3 V I/O operating voltage
- 385 mW power consumption (typical)

Sample Handheld PC Application with VRC4171A
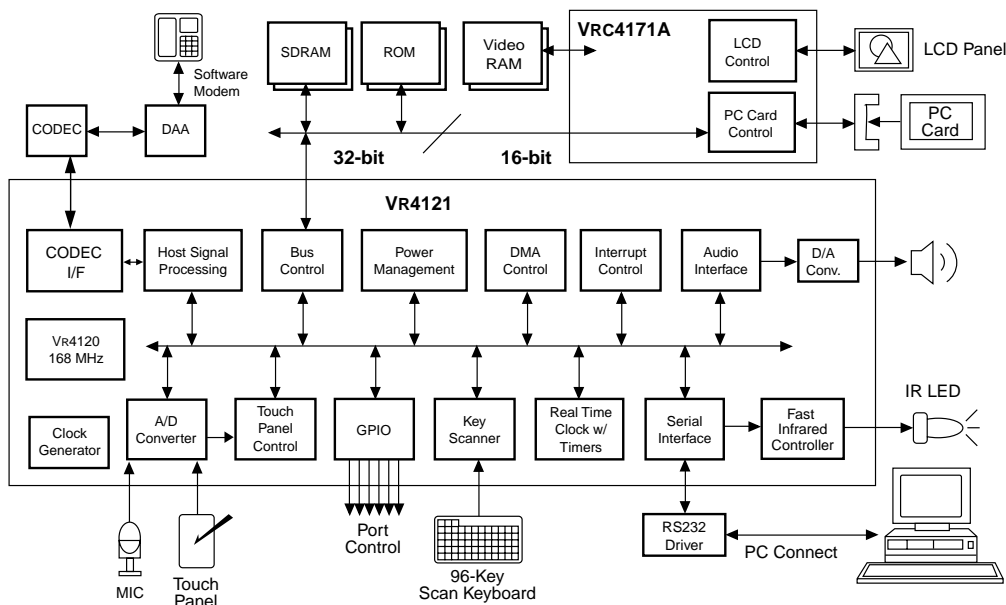
VR4111 and VR4121 Comparison

	VR4111	VR4121
CPU Core	VR4110	VR4120
Maximum Pipeline Clock	90 MHz	168 MHz
Cache Size	Inst: 16 KB/Data: 8 KB	Inst: 16 KB/Data: 8 KB
Instruction Set	MIPS III, MIPS 16	MIPS III, MIPS 16
MAC Instruction	Single cycle, 16-bit	Single cycle, 32-bit
Operating Voltage	2.5 V core; 3.3 V I/O	2.5 V core; 3.3 V I/O
Integrated Peripherals	Same	Same
Memory Interface	64 MB EDO DRAM 64 MB ROM	64 MB EDO DRAM/SDRAM 64 MB ROM
Power Consumption	200 mW	385 MW
Package	224-pin FPBGA	224-pin FPBGA
Process Technology	0.25 micron	0.25 micron

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VR4122
64-Bit MIPS RISC Microprocessor

Salient Features

◗ VR4120™ CPU running at 180 MHz (216 Dhrystone MIPS) with memory management unit

◗ MIPS I, II, III, and MIPS16 instruction set compatible

◗ Six-stage pipeline running at up to 180 MHz

◗ Single-cycle 32-bit MAC instruction for DSP operations

◗ 32 KB instruction cache, 16 KB data cache

◗ Power management unit with four modes

◗ Interrupt control unit and DMA controller

◗ Real-time clock with four built-in timers

◗ 16550 serial interface with separate debug port

◗ PCI bus interface unit supports 32-bit 33 MHz PCI bus

◗ Fast infrared interface up to 4 Mbps

◗ 270 mW typical power consumption at 180 MHz

◗ Operating voltage 1.8 V core, 3.3 V I/O

◗ 224-pin FPBGA package

Product Overview

Designed around the popular MIPS RISC architecture, the 64-bit VR4122™ (μPD30122) offers excellent power consumption and performance in a highly integrated, low-cost system on a chip.

This processor uses the ultra-low-power-consuming VR4120 CPU core based on advanced 0.18-micron technology. The VR4120 CPU has an optimized five-stage pipeline, 32 KB instruction cache, 16 KB data cache, multiply-and-accumulate (MAC) unit, and memory management unit (MMU) to enable high performance in a compact, low-cost chip.

The VR4122 is compliant with the MIPS I, II, III, and MIPS16 instruction set architectures. It provides an easy choice for VR4121™ customers in terms of upgrade, since the VR4121 and VR4122 are software compatible.

The VR4122 microprocessor's high speed, compact size, and low power consumption make it ideal for use in battery-driven, portable handheld systems.

Ordering Information

Part Number	Package	Operating Frequency
μPD30121F1-150-GA1	224-pin FPBGA	150 MHz
μPD30122F1-180-GA1	224-pin FPBGA	168 MHz

Features

VR4120 CPU Core

• MIPS I, II, III ISAs without FPU, LL, LLD, SC, and SCD instructions
• MIPS16 ASE compliant for compact code density
• Five-stage pipeline running at up to 168 MHz (216 Dhrystone MIPS)
• Single-cycle 32-bit MAC instruction for DSP operations

NEC

VR4122 Block Diagram
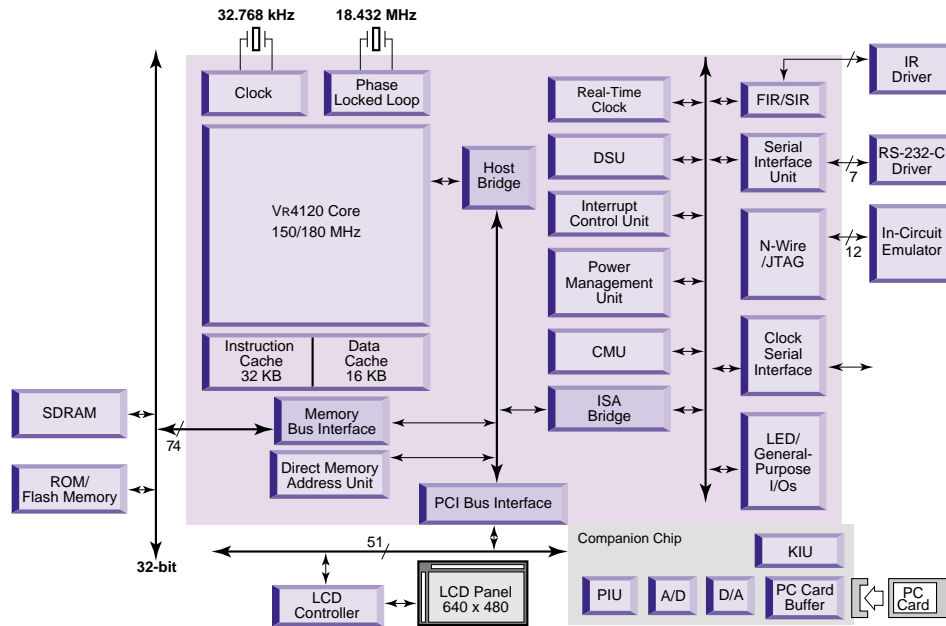
Memory Management Unit

- 32-bit physical addressing range of 4 GB with 40-bit virtual address space
- 32 double-entry TLBs supporting 1~256 KB page size
- Up to 128 MB of SDRAM/EDO/fast-page DRAM and 128 MB of SROM/flash memory/mask ROM

Cache Memory Unit

- 32 KB direct-mapped instruction cache
- 16 KB direct-mapped data cache

Bus Control Unit

- Supports 32-bit and 16-bit addressing modes
- Dynamic bus sizing supports a subset of the ISA bus
- Supports 32-bit 33 MHz PCI bus

Power Management Unit

- Supports four power-saving modes: Fullspeed, Standby, Suspend, and Hibernate

Clock Generator Unit

- Built-in PLL for frequency multiplication

Real-time Clock with Four Built-in Timers Interrupt Control Unit

- Supports both internal and external interrupts

DMA Address Unit and DMA Control Unit

- Controls three different types of DMA

General-Purpose I/O Unit

- Controls 31 GPIO pins

Serial Interface Unit (16550 compatible)

- RS-232-C compliant
- 1.5 Mbps data transfers
- Separate serial debugging port

PCI Bus Interface Unit

- Supports 32-bit 33 MHz PCI bus

Fast IR Unit

- Performs 0.5 to 4 Mbps IrDA 1.1 standard communication

AC/DC Specifications

- 180 MHz maximum frequency
- 1.8 V core and 3.3 V I/O operating voltage
- 270 mW power consumption (typical)

Sample Handheld PC Application with VRC4173 Companion Chip
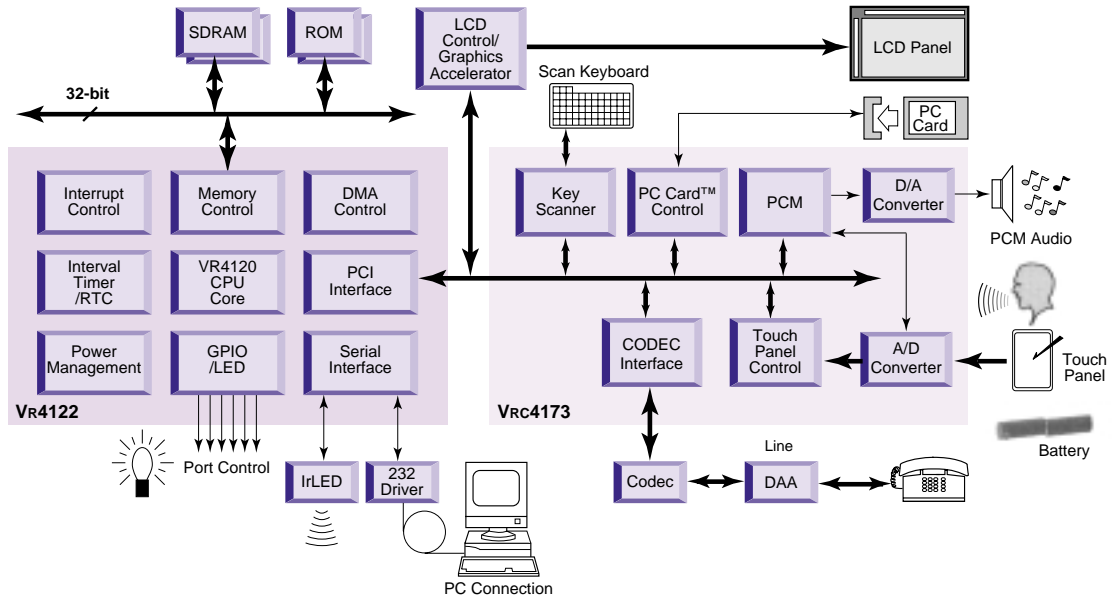
VR4100 Family Comparison

	VR4121	**VR4122**
CPU Core	VR4120	VR4120A
Max. Pipeline Clock	168 MHz	180 MHz
Cache Size	Instruction: 16 KB Data: 8 KB	Instruction: 32 KB Data: 16 KB
Performance	210 Dhrystone MIPS	216 Dhrystone MIPS
Instruction Set	MIPS I, II, III, MIPS16	MIPS I, II, III, MIPS16
MAC Instruction	Single-cycle, 32-bit	Single-cycle, 32-bit
Operating Voltage	2.5 V (core); 3.3 V (I/O)	1.8 V (core); 3.3 V (I/O)
Integrated Peripherals	Same, plus keyboard, touchscreen, HSP, A/D, D/A	Same, plus PCI bus controller
Bus Supported	Subset of ISA	PCI, Subset of ISA
Memory Interface	128 MB DRAM 128 MB ROM	128 MB DRAM 128 MB ROM
Power Consumption	350 mW	270 mW
Package	224-pin FPBGA	224-pin FPBGA
Temperature Range	-10~70º	-10~70º
Process Technology	0.25-micron UR2 process	0.18-micron UC3 process

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VR4181
64-Bit MIPS RISC
Microprocessor

Salient Features

◗ VR4110™ CPU running at 66 MHz
   (87 Dhrystone MIPS) with memory
   management unit

◗ MIPS I, II, III, and MIPS 16 instruction set
   compatible

◗ Single-cycle 32-bit MAC instruction for DSP
   operations

◗ 4 KB instruction cache, 4 KB data cache

◗ Power management unit with four modes

◗ Interrupt control unit and DMA controller

◗ Real-time clock with four built-in timers

◗ 16550 serial interface with separate debug port

◗ Fast infrared interface up to 4 Mbps

◗ Keyboard, touch-panel, and LED interface
   controller

◗ 10-bit D/A and A/D converters

◗ 250 mW typical power consumption

◗ Operating voltage: 2.5 V core, 3.3 V I/O

Product Overview

Designed around the popular MIPS RISC architecture, the
VR4181™ (mPD30181) offers excellent power consumption
and performance attributes in a highly integrated, low-cost
system on a chip.

This processor is the third NEC device to use the ultra-low-
power-consuming VR4110 CPU core based on advanced
0.25-micron technology. The VR4110 CPU has an optimized
five-stage pipeline, 4 KB instruction cache, 4 KB data cache,
multiply-and-accumulate (MAC) unit, and memory
management unit that enable high performance in a compact
low-cost chip. The VR4121 is compatible with the MIPS I, II,
III, and MIPS 16 instruction set architectures.

The VR4181's integrated peripherals include an LCD
controller, CompactFlash™ interface, power management
unit, DMA unit, interrupt control unit, timers, real-time clock,
two 16550-compatible serial interfaces, a fast IrDA®
interface, keyboard interface, touch-panel interface, universal
serial bus (USB) functional interface, host signal processing
unit (software modem), A/D converter, and D/A converter.

The VR4181 microprocessor complies with the MIPS III
instruction set architecture (ISA) and MIPS16 application-
specific extension (ASE). The MIPS16 ASE compliance
enables the VR4111 to incorporate 16-bit-long instructions
with conventional 32-bit-long instructions, which results in
compact code, smaller memory, and lower system cost.

Applications

• Handheld PCs and PDAs

• Smart phones and Internet/e-mail phones

• Personal GPS

• Battery-powered consumer embedded controllers

Ordering Information

Part Number	Package	Operating Frequency
μPD30181GM-66-8ED	160-pin LQFP	66 MHz

NEC

VR4181 Block Diagram
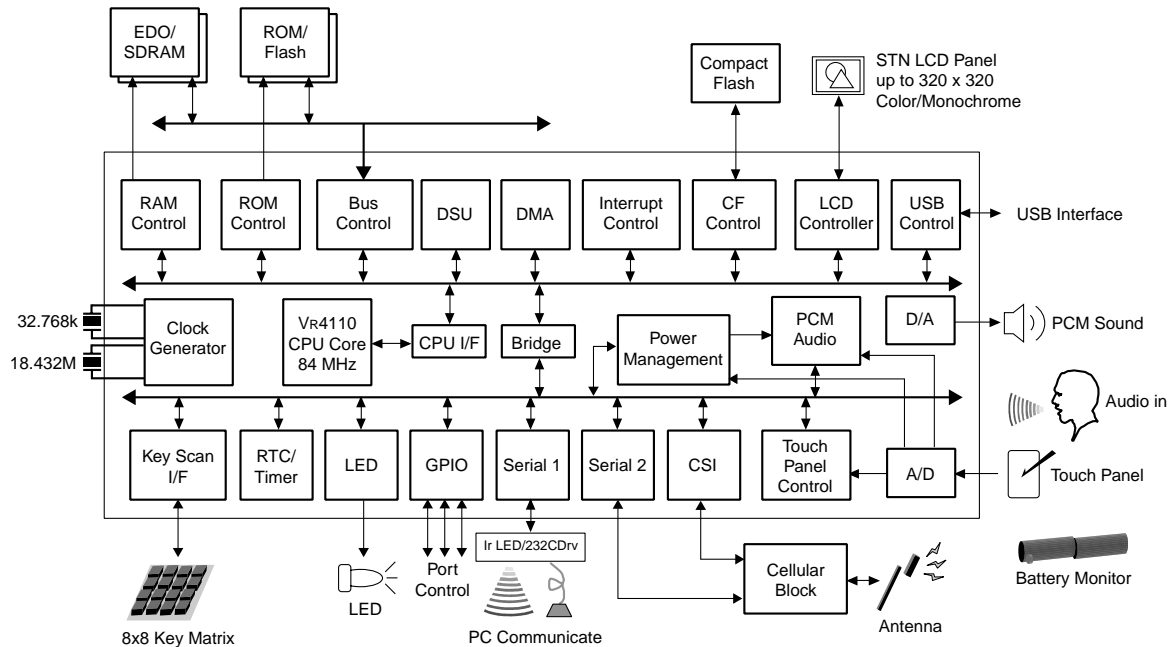
Features

VR4110 CPU Core

- MIPS I, II, and III ISA compliant
- MIPS 16 ASE compliant for compact code density
- Five-stage pipeline running at up to 66 MHz (87 Dhrystone MIPS)
- Single-cycle 32-bit MAC instruction for DSP operations

Memory Management Unit

- 32-bit physical addressing range of 4 GB with 40-bit virtual address space
- 32 double-entry TLBs supporting 1~256 KB page size
- Up to 64 MB of SDRAM/EDO/fast-page DRAM and 64 MB of SROM/flash memory/mask ROM
- Up to 66 MHz operation

Cache Memory Unit

- 4 KB direct-mapped instruction cache
- 4 KB direct-mapped data cache

Bus Control Unit

- Ultra-power-saving Modular Bus Architecture (MBA)
- Supports 32-bit and 16-bit addressing modes
- Dynamic bus sizing supports a subset of the ISA bus

Power Management Unit

- Supports four power-saving modes: Fullspeed, Standby, Suspend, and Hibernate

Clock Generator Unit

- Built-in PLL for frequency multiplication
- External bus frequency of 16 and 33 MHz

Real-time Clock with Four Built-in Timers

Interrupt Control Unit

- Supports both internal and external interrupts

DMA Address Unit and DMA Control Unit

- Controls five different DMA channels

General-Purpose I/O Unit

- Controls 49 GPIO pins

Keyboard (64-key), Touch-panel, and LED Interface

10-bit A/D Converter for Touch-panel and Audio Input

Two Serial Interface Unit (16550 compliant)

- Supports up to 115 kbps
- RS-232-C compliant

Fast IR Unit

• Performs 0.5 to 4 Mbps IrDA 1.1 standard communication

Audio Interface Unit and 10-bit D/A Converter

• Supports audio output and microphone input sampling

USB Function Interface

• File/data synchronization with a desktop/laptop system

AC/DC Specifications

• 66 MHz maximum frequency
• 2.5 V core and 3.3 V I/O operating voltage
• <250 mW power consumption (typical)

Sample Handheld PC Application with VR4181
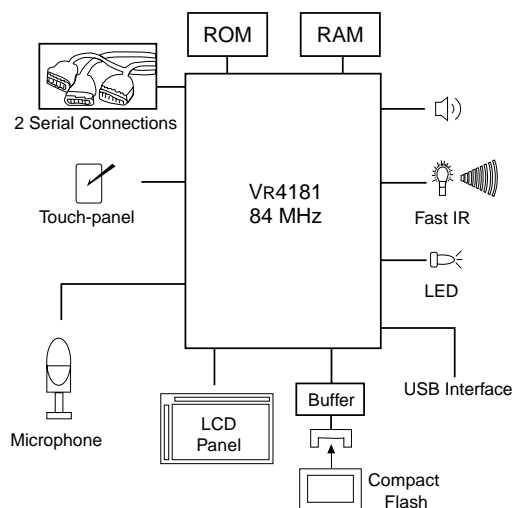
VR4111, VR4121, and VR4181 Comparison

	VR4111	VR4121	VR4181
CPU Core	VR4110	VR4120	VR4110
Maximum Pipeline Clock	84 MHz	168 MHz	66 MHz
Cache Size	Inst: 16 KB/Data: 8 KB	Inst: 16 KB/Data: 8 KB	Inst: 4 KB/Data: 4 KB
Performance	110 Dhrystone MIPS	216 Dhrystone MIPS	87 Dhrystone MIPS
Instruction Set	MIPS III, MIPS 16	MIPS III, MIPS 16	MIPS III, MIPS 16
MAC Instruction	Single-cycle, 16-bit	Single-cycle, 32-bit	Single-cycle, 16-bit
Operating Voltage	2.5 V core; 3.3 V I/O	2.5 V core; 3.3 V I/O	2.5 V core; 3.3 V I/O
Integrated Peripherals	Same	Same	Same plus: CompactFlash™ Interface LCD controller USB functional interface
Memory Interface	64 MB DRAM 64 MB ROM	64 MB DRAM (SDRAM) 64 MB ROM	64 MB DRAM 64 MB ROM
Power Consumption	185 mW	385 MW	250 MW
Package	224-pin FPBGA	224-pin FPBGA	160-pin LQFP
Process Technology	0.25 micron	0.25 micron	0.25 micron

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VR4300, VR4305, VR4310 64-Bit MIPS RISC Microprocessors

Salient Features

❫ 64-bit MIPS RISC architecture

❫ 167-MHz maximum internal operating frequency

❫ Conformance to MIPS I/II/III instruction set architecture

❫ Five-stage pipeline processing

❫ High-speed execution of integer and floating-point operations

❫ Maximum performance levels of 100 SPECint92 and 75 SPECfp92 at 167 MHz

❫ Same input clock as system bus frequency

❫ 16 KB instruction cache and 8 KB data cache

❫ Multiplexed 32-bit address/data bus

❫ Low power dissipation: 2.0 W typical and 2.4 W maximum

❫ Supply voltage of 3.3 volts

❫ 120-pin plastic QFP packaging

Product Overview

The VR4300™, VR4305™, and VR4310™ are high-performance, 64-bit microprocessors employing the RISC architecture developed by MIPS. They have a 32-bit system bus and are intended for use in high-performance embedded device applications.

Applications

- Embedded controllers
- Page printer controllers
- Amusement game machines

Ordering Information

Part Number	Package
µPD30200GD-100-MBB	120-pin plastic QFP (28 x 28 mm)
µPD30200GD-133-MBB	
µPD30205GD-80-LBB	
µPD30210GD-100-MBB	
µPD30210GD-133-MBB	
µPD30210GD-167-MBB	

Features

Execution Unit

- 64-bit register file
- 64-bit integer/mantissa data bus
- 12-bit exponent data bus

Coprocessor 0

- Exception processing unit with system control coprocessor registers
- Memory management unit that converts virtual addresses into physical addresses and verifies memory access of kernel, supervisor, and user memory segments
- Seven page sizes: 4 KB, 16 KB, 64 KB, 256 KB, 1 MB, 4 MB, and 16 MB (VSIZE = 40 and PSIZE = 32)
- Translation lookaside buffer with 32 entries, each mapped to an even or odd frame buffer page

Pipeline Control

- Occurrence of cache misses
- Flash buffer full
- Multicycle instructions
- Occurrence of system exceptions

NEC

VR4300, VR4305, VR4310 Block Diagram

Data Address   Control   Master Clock

System Interface   ←   Clock Generator

Instruction Cache   ↔   Data Cache

CP0   TLB

Instruction Address   Execution Unit

Pipeline Control
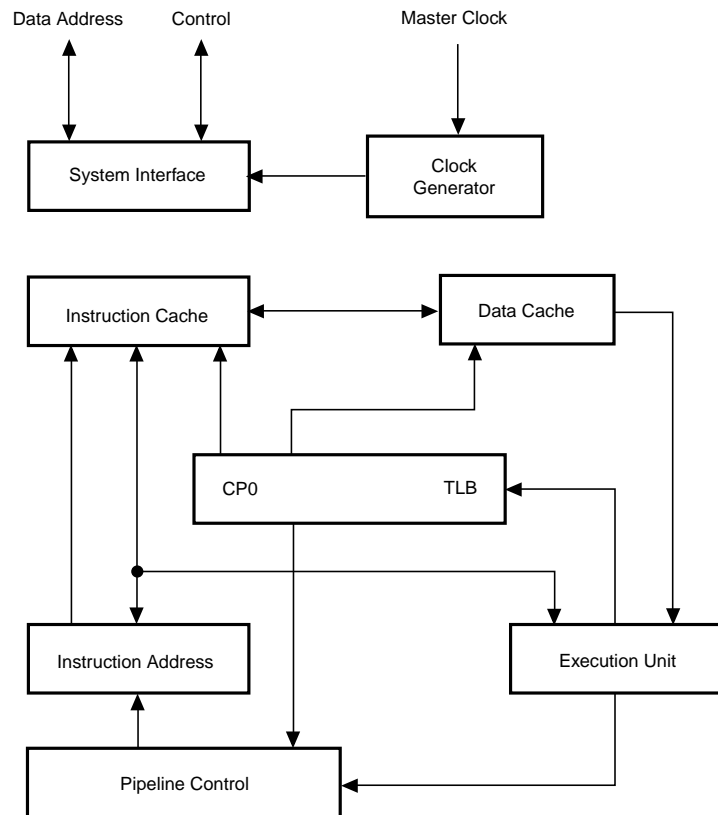
Instruction Address

- PC incrementer
- Branch address adder
- Conditional branch address selector

Instruction Cache

- Direct map
- Virtual index address
- Physical tag

No hardware is provided to check generation of a cache alias due to a virtual address. Each line consists of 8-word data, a 20-bit tag, and a valid line bit. The cache data interface is 64 bits wide. Cache parity is not supported.

Data Cache

- Direct map
- Virtual index address
- Physical tag write-back

Each cache line consists of 4-word data, a 20-bit tag and valid line bit, and a write-back bit and its bit parity. Two cache lines correspond to one physical line. Data is read from the cache in one cycle and written to the cache in two cycles. Cache parity is not supported.

System Interface

- Multiplexed 32-bit address/data bus
- Clock signal
- Interrupt request
- Control signal

Clock Generator

Generates four clocks from MasterClock input:

- PClock: frequency is set using DivMode(1.0) signals at cold reset
- SClock: system interface clock (internal)
- TClock: output clock reference for external agent; same frequency as MasterClock, except in low-power mode where operating frequency = one-fourth of normal (low-power mode is set using the status register RP bit; PClock and SClock frequencies are dynamically switched by this means)

The processor uses a phase-locked loop (PLL) to suppress skew between the input clock and the internal clock.

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VR5000
64-Bit MIPS RISC Microprocessor

Salient Features

◗ Two-way superscalar pipeline

◗ Built-in secondary cache controller configured as 512 KB, 1 MB, or 2 MB

◗ Separate 32 KB, two-way, set-associative instruction and data caches

◗ Separate integer and floating-point ALUs

◗ Performance levels of 6.6 SPECint95 and 6.6 SPECfp95 at 250 MHz

◗ Conformance to MIPS I/II/III/IV instruction set architecture

◗ 100 MHz system interface clock

◗ Translation lookaside buffer with 48 dual entries; variable page size (4 KB to 16 MB in x4 increments)

◗ Increased floating-point performance

◗ Single external clock signal

◗ 223-pin ceramic PGA and 272-pin cavity-down BGA packaging

Product Overview

The VR5000™ (µPD30500) is a high-performance microprocessor with 64-bit dual-issue superscalar architecture that offers enhanced point computing capabilities and scalable performance. Based on the MIPS IV instruction set architecture (ISA), the VR5000 is also binary compatible with the MIPS I, II, and III ISAs.

A two-way superscalar pipeline with high-speed, low-latency execution units enables the VR5000 to achieve high performance for low cost. At 250 MHz, the VR5000 is estimated to deliver performance levels of 6.6 SPECint95 and 6.6 SPECfp95 in optimal system configuration. The VR5000 achieves these high performance levels while maintaining a die area of less than 90 mm^2.

Other features include arithmetic logic units (ALUs) that are heavily pipelined for high throughput of floating-point instructions; on-chip, two-way, set-associative 32 KB instruction and data caches; and on-chip support for an external secondary cache.

Applications

• Personal workstations
• Network servers
• Imaging systems
• Copiers
• Laser printers
• Windows NT™ servers

NEC

VR5000 Block Diagram
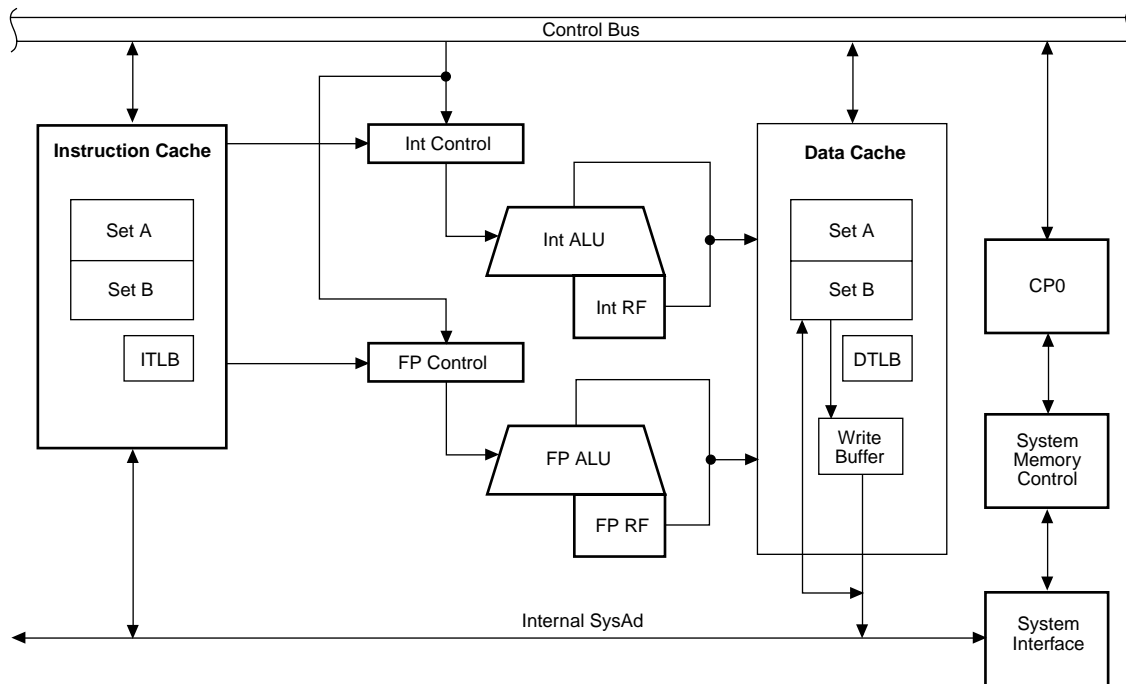
Ordering Information

Part Number	Package
μPD30500RJ-150	223-pin PGA
μPD30500RJ-180	
μPD30500RJ-200	
μPD30500S2-180	272-pin BGA
μPD30500S2-200	
μPD30500S2-250	

Features

Dual-Issue Instruction Mechanism

The dual-issue mechanism allows a floating-point arithmetic logic unit (ALU) instruction to be issued simultaneously with any non-floating-point ALU instruction, thereby boosting performance in applications that require both fixed- and floating-point mathematical calculations.

Pipelined ALUs

The VR5000 contains dedicated acceleration hardware for most floating-point ALU instructions for DIV/SQRT. This hardware allows long-latency operations, such as those for divide and square root, to be performed in a dedicated unit while other shorter-latency operations are performed simultaneously.

Separate Integer and Floating-Point ALUs

With separate integer and floating-point ALUs, integer instructions no longer have to wait for long-latency, floating-point operations to finish before being fetched. Load/store operations may also be issued simultaneously with floating-point ALU instructions to reduce load latencies and bandwidth.

Low-Latency Instructions

The MIPS IV instruction set supports four multiply-add-subtract instructions:

- Multiply-Add (MADD)
- Multiply-Subtract (MSUB)
- Negative Multiply-Add (NMADD)
- Negative Multiply-Subtract (NMSUB)

Two separate floating-point computations can be performed with one instruction.

Large On-Chip Primary Caches

The VR5000 contains separate 32 KB data and instruction caches. Each cache has a 32-byte fixed line size and is two-way set associative, which helps to increase the hit rate over a direct-mapped implementation. Cache lines may be classified as write-through or write-back on a per-page basis.

Both caches are virtually indexed and physically tagged. A virtually indexed cache allows the cache access to begin as soon as the virtual address is generated, as opposed to waiting for the virtual-to-physical translation. The cache is accessed at the same time as the address translation is performed.

Having large primary caches allows more of the application to be executed on chip, reducing accesses to slower secondary caches and main memory. This in turn reduces bus utilization and allows the application to run faster, since fewer off-chip accesses are required.

Secondary Cache Support

Large applications often use a secondary cache to reduce the number of accesses to slower main memory. The VR5000 contains a dedicated secondary cache interface with a complete set of signals (such as data enable, chip enable, output enable, address match, cache valid, line index, and word index) that provides an efficient interface with the processor, a secondary cache configured as 512 KB or 1 MB or 2 MB, and secondary cache tag RAM.

The secondary cache interface supports multiple cache sizes and the write-through data transfer protocol. Data transfers to the secondary cache share the 64-bit system bus. Uncached bus cycles are not evaluated by the secondary cache control logic as they travel to the external agent. Uncached operations such as video screen updates can be passed directly to the system logic responsible for routing the data to the screen without any delays from the secondary cache logic.

Contact List

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E-mail: vrsupport@el.nec.com

Japan

NEC Corporation
1753 Shimonumabe, Nakahara-Ku
Kawasaki, Kanagawa 211, Japan
Tel: +81-44-435-1485

VR5432
64-Bit MIPS RISC
Microprocessor

Salient Features

▶ Dual-issue superscalar pipeline with six independent execution units

▶ Separate 32 KB two-way set-associative instruction and data caches with cache line locking and parity

▶ Two unified 64-bit integer/floating-point units, each with 64-bit barrel shifters

▶ 316 Dhrystone MIPS at 167 MHz

▶ Conformance to MIPS IV instruction set architecture

▶ DSP and multimedia instruction extensions

▶ 100 MHz system interface clock

▶ On-chip debugging support: JTAG, N-wire and N-trace functions

▶ 64-bit architecture with a 32-bit multiplexed address/data bus interface

▶ Low power consumption: 2.5 watts at 167 MHz

Product Overview

The VR5432™ brings a new level of high-end performance to embedded design with 64-bit architecture, dual-issue superscalar pipeline and MIPS IV ISA support. This processor is ideally suited for digital television, set-top boxes, games, midrange printers, and network computers.

The VR5432 is supported by six independent execution units, 32 KB instruction, and 32 KB data caches. The processor also provides enhanced caching and bus protocols and DSP and multimedia instruction extensions.

The VR5432 implements a JTAG test interface with N-wire and N-trace enhancements that support comprehensive hardware and software breakpoints and trace functions. The N-wire and N-trace functions give microprocessor system development tools direct control over the CPU core and important information about its execution activity. These functions support access to all system resources, including the processor's user and debugging registers, program counter, register file, and caches.

Low Power Consumption

The VR5432 is designed specifically for low-power, low-cost embedded applications. It uses a 32-bit multiplexed address/data bus interface and consumes 2.5 watts at 167 MHz. The processor is fully static, including the register file, caches, and TLBs.

A gated clock, minimal switching techniques, and special circuit design techniques keep power consumption to only 2.5 watts maximum at 167 MHz. The pipeline issue logic examines issued instructions and turns off appropriate functional units dynamically on a per-clock basis. The VR5432's design eliminates self-timed circuits and other timing dependencies. Local clock drivers not only reduce power consumption, but also improve clock skew.

High Performance

The performance of the VR5432 embedded processor is largely due to the superscalar pipeline, a symmetric dual-issue pipeline (dual unified data paths) with six independent execution units. The dual data paths execute any combination of arithmetic logic unit (ALU), floating-point, or rotate instructions.

NEC

Both of the 32 KB caches implement cache line locking to keep critical code and data cached. Multiple outstanding read transactions allow both caches to be filled concurrently. These cache enhancements keep the processor supplied with a steady stream of instructions and data. Mapping of accesses to virtual memory addresses is optimized with a 48-double-entry joint instruction / data translation lookaside buffer (TLB) and two separate four-entry micro TLBs for instructions and data.

MIPS Architecture Extensions

- Integer multiply-accumulate instructions and other register-based multiply variations for fast DSP support
- Integer rotate instructions for fast 32-bit and 64-bit string operations
- Packed-data vector operations for fast 8 x 8-bit image and multimedia processing
- Cache line locking instructions (both caches) for better cache management

VR Series Family Comparison

Description	VR4300	VR5000	VR5432
Instruction set architecture	MIPS III	MIPS IV	MIPS IV Rotate instructions DSP (integer MAC) Multimedia
Pipeline	Scalar	Limited two-way superscalar issue	Symetric two-way superscalar issue
Execution units	Single issue Floating-point	Integer and floating point	(Two) Integer + FP + barrel shifter Multiply-accumulate Packed-data vector Load/store Branch
Load/store architecture	Blocking	Blocking	Nonblocking (hits under misses) Up to four outstanding data cache misses
Instruction cache size	16 KB	32 KB	32 KB
Data cache size	8 KB	32 KB	32 KB
Instruction TLB	2-entry 4 KB fixed page size	2-entry 4 KB fixed page size	4-entry Variable page sizes
Data TLB	None	2-entry 4 KB fixed page size	4-entry Variable page sizes
Hardware debugging features	JTAG	None	JTAG N-Wire N-Trace Hardware and software breakpoints, instruction jamming
Performance counters for software tuning	None	None	Two 32-bit counters; any 2 of 16 events selectable
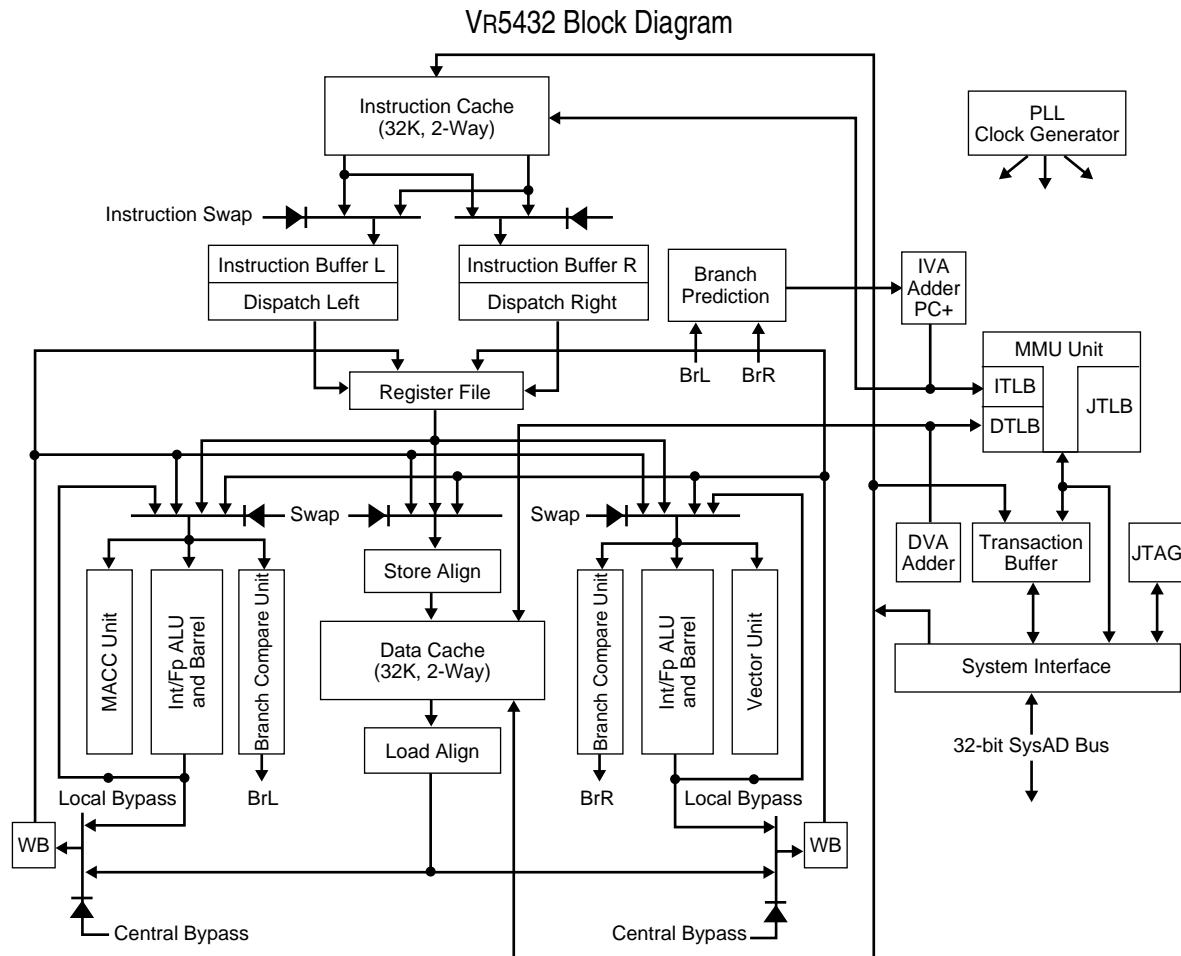
VR5432 Block Diagram

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VR10000/12000 64-Bit MIPS RISC Microprocessor

Salient Features

▶ Compatibility with MIPS I/II/III/IV instruction set architecture

▶ Architecture with Nonsequential Dynamic Execution Scheduling (ANDES) support

▶ Four-way superscalar pipeline

▶ 32 KB, two-way, set-associative instruction cache

▶ 32 KB, two-way, set-associative data cache

▶ 64-dual-entry translation lookaside buffer

▶ Five separate execution units

▶ 300 MHz internal clock rate (VR12000)

▶ Single external clock

▶ Performance levels of 17 SPECint95 and 27 SPECfp at 300 MHz (VR12000)

▶ Out-of-order instruction execution/register renaming

▶ On-chip integer, floating-point, and address queues

▶ Dedicated 128-bit secondary cache data bus

▶ Full MESI protocol support

▶ Compliant with ANSI/IEEE standard 754-1985 (binary floating-point arithmetic) and IEEE standard 1149.1/D6 (boundary scan architecture)

▶ Avalanche system bus interface (up to 1.6 GB per second)

▶ Split transaction support

▶ Programmable system interface

▶ 599-pin CLGA packaging

Product Overview

The VR10000™ (μPD30700) and VR12000™ are powerful, 64-bit microprocessors with a four-way superscalar pipeline that fetches and decodes four instructions per cycle. Each decoded instruction is appended to one of three instruction queues. Each queue can perform dynamic scheduling of the instructions. The queues determine execution order based on the availability of the required execution units.

Instructions are initially fetched and decoded in order, but can be executed and completed out of order, allowing the processor to have up to 32 instructions in various stages of execution. High throughput is achieved through the use of dedicated wide data paths and large on- and off-chip caches.

The VR10000 and VR12000 implement the MIPS IV instruction set architecture, a superset of MIPS III, which is backward compatible. At 200 MHz, the VR10000 delivers peak performance of 800 MIPS with a peak data transfer rate to a secondary cache of 3.2 GB per second.

Applications

• Windows NT™ servers
• Digital media network applications
• UNIX™ MP and MPP systems
• Engineering and scientific computing
• Three-dimensional graphics processing
• Database servers
• Multiuser systems

NEC

VR10000 Block Diagram
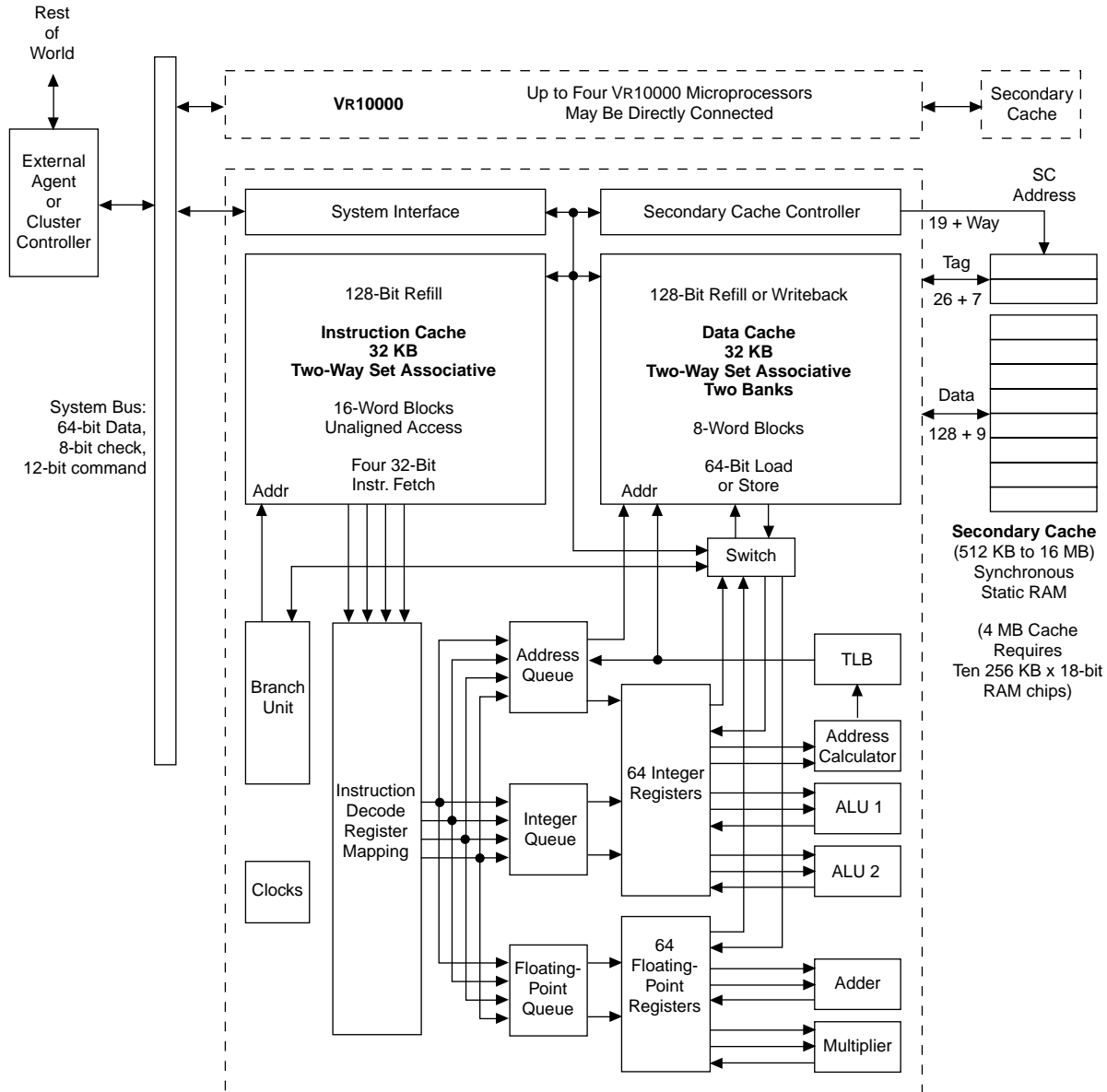
Ordering Information

Part Number	Package
µPD30700RS-200	599-pin CLGA
µPD30700RS-250	
µPD30700RS-300	

Queuing Structures

Features

Branch Prediction

The branch unit can decode and execute one Branch instruction per cycle. Since each branch is followed by a delay slot, a maximum of two Branch instructions can be fetched simultaneously, but only the earlier one will be decoded in a given cycle.

The VR10000/12000 contains three instruction queues: integer, floating-point, and address. These queues

dynamically issue instructions to five execution units that operate independently.

Integer Arithmetic Logic Units (ALUs)

The two integer ALUs in the VR10000/12000 are defined as ALU1 and ALU2. Integer ALU operations, with the exception of multiply and divide, execute with a one-cycle latency and one-cycle repeat rate.

Floating-Point Units (FPUs)

The VR10000/12000 contains two primary FPUs: one for add operations and another for multiply operations. Two secondary FPUs handle long-latency operations such as those for divide and square root.

Secondary Cache Interface

The VR10000/12000 contains an internal secondary cache controller with a dedicated secondary cache port. Data is transferred via a dedicated 128-bit transfer bus at the processor's internal operating frequency, yielding a maximum secondary cache data transfer rate of 3.2 GB per second. The VR10000/12000 also provides a 64-bit system interface data bus.

The secondary cache interface is implemented as two-way set associative. Maximum cache size is 16 MB and minimum size is 512 KB. The transfer rate is 128 bits or four 32-bit words. Consecutive cycles are used to transfer larger blocks of data.

System Interface

The system interface provides a gateway between the VR10000/12000 and its associated secondary cache and the rest of the computer system. The system interface operates at the SysClock frequency supplied to the processor.

In most microprocessor systems, only one system transaction can occur at any given time. The VR10000/12000 supports a split-level bus transaction protocol. Split-level transactions allow additional processor and external requests to be issued while waiting for a previous response. A maximum of four outstanding transactions at any given time are supported.

Multiprocessor Support

Two configurations of multiprocessor systems can be implemented using the VR10000 or VR12000. One uses a dedicated external agent interface to each processor. The external agent is typically an ASIC that provides a gateway to the memory and I/O subsystems. In this type of configuration, the processors do not interface directly but rather through each external agent. Although commonly used, this implementation increases cost as well as overall system

complexity because at least one external agent must accompany each processor.

The VR10000/12000 also provides pin support for a cluster bus configuration. Up to four CPUs may be connected via a cluster bus. Only one external agent is then required to interface to other system resources. Each processor interfaces to the same external agent. The cluster bus implementation reduces not only the complexity, but also the number of ASICs and, hence, the cost of the system by requiring only one external agent for every four processors.

In addition to the 64-bit multiplexed address/data bus, a two-bit state bus is used for issuing processor coherency state responses. Also, a five-bit system response bus is used by the external agent to issue external completion responses.

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Chipsets

BONITO MIPS System Controller Cores and Chips

Salient Features

▶ Decent clock rates: the ASIC is very conservatively targeted at 83 MHz, but we expect to see higher frequencies

▶ Supports variant MIPS CPUs: not all MIPS CPUs sharing the SysAD bus are the same, but BONITO supports all known 32-bit variants

▶ Configurable SDRAM port: runs synchronous to the CPU. Glueless for small systems, supporting 64-bit DIMMs. Accepts external isolating switches and/or registers/drivers for larger configurations.

▶ PCI 2.1, 33 MHz, 32 bits: basic PCI as is widely used throughout the industry. Suitable for "host" or "peripheral" applications. The PCI clock need not be related to the CPU clock.

▶ I/O buffer cache: provides efficient PCI master access to local memory (usually the key I/O performance characteristic)

▶ High integration: glueless support for MIPS CPU reset (including the infamous "configuration bitstream"), for example

▶ Reliable BGA packages: we know production engineers hate big QFPs, and we thought that in-system price/performance would get worse if we were short of pins

▶ Unique debug mode/port: there is a mode that makes all cycles visible to a probe board connected to the SDRAM interface, so that developers can easily watch addresses and data without loading the board with a special connector

▶ Core logic is synthesizable Verilog: the same source code is used to produce both a Xilinx FPGA implementation (using "Synplicity") and an ASIC (using Synopsys tools). Core logic users also get a test-bench using realistic models of connected devices. It's all Algorithmics-written or freely redistributable code.

▶ Programmer and development support: basic source code and a full bug list are freely available on line

CPUs Supported

All NEC VR Series processors

Product Overview

BONITO is a MIPS system controller that connects one of many different MIPS CPUs to a local SDRAM memory system, a PCI expansion bus, and a simple local I/O bus for ROM and 8-bit peripherals. BONITO is available now as reusable Verilog code configurable between 64-bit and 32-bit bus width at the CPU/SDRAM port. An ASIC for 32-bit systems is available now.

Why BONITO?

There are already several MIPS system controllers out there. BONITO is a cost-effective solution that will get you to market faster with a higher quality product.

• Algorithmics' MIPS system design experience goes back more than ten years

• Appropriate detailing: we included, for example, a PCI arbiter and interrupt controller; we omitted, for example, a UART, or fast/wide PCI. Why? see below.

algorithmics

- Technical features for development support: before the product there's development. BONITO's debug mode makes every cycle visible on a logic analyzer, via an SDRAM expansion connector.
- Human development support: Algorithmics' overall business is to provide products and services to companies building MIPS systems. BONITO is not an orphan from a customer-special project. The design engineers respond to your e-mails.

  Moreover, we do not believe that good marketing demands that we hide bugs until you fall over them. We're not proud that our designs have bugs in them, but we'll tell you all we know so that your development team won't have to pay the price. (Before you select another controller, ask the vendor for their bug list, and why it isn't on line.)

Important Details

BONITO won't fit into a 208-pin QFP package. But its BGA is more reliable—and you might as well get that extra product cost back again, and more, because our experience-based integration will save components and pins in every MIPS design. Here are some of our choices:

- Glueless CPU interface: you won't need to make any other connection to the CPU. That includes the whole reset sequence, and CPU interrupts. There's even a 6-output clock buffer for small systems.
- GPIO/GPIN pins: 9 bidirectional and 6 input uncommitted I/Os, easily programmable for direction. Ten can be interrupt inputs.
- Interrupt controller: 24-way controller is simple to program, but allows individual polarity and edge/level selection on GPIO inputs. Interrupts can be individually steered toward one of two CPU interrupts.
- The PCI arbiter: 6-way arbiter is built in (supports 7 bus masters, including BONITO itself. Its use is configurable.
- All registers are PCI and locally accessible: nothing is offered only to one side. PCI "mailbox" registers do act differently, of course.
- Can boot from PCI: a BONITO system can be completely initialized from the PCI side, with no ROM code installed for the MIPS CPU (you can either boot the MIPS CPU from local SDRAM or program the flash memory from PCI).
- 33 Mbyte/s UDMA IDE port: attaches to the I/O bus with one buffer component

Debug Interface

Low-level debug information about CPU and PCI cycles is made available using pseudo-DRAM cycles, and can be picked up by a board plugged into a suitable socket. Algorithmics has a debug board available, and design information is available free if you need to reshape it.

On-line Software/Design Information

At http://www.algor.co.uk/ftp/pub/bonito/ you'll find C header files for BONITO's registers and memory map, a downloadable manual, a bug list, package and pinout information, and other useful stuff.

OS Support

Algorithmics intends to have good support for a number of different embedded OSs available for BONITO-based systems. Currently we have a VxWorks BSP, but we intend to add a Windows CE OAL and support for free OS OpenBSD (Linux soon). Everyone makes these claims so you could be forgiven for being skeptical, but all the above except Linux (we're working on it) are shipping right now on Algorithmics' P-4032 and P-5064 board products.

What Did We Leave Out?

The fine art of product design involves stopping somewhere. What isn't in BONITO?

- Simple peripheral controllers: no UART, for example. 8-bit UARTS are very cheap, and we don't want the license complexities of bought-in IP.
- 64-bit or 66 MHz PCI: we guessed that low-cost embedded systems wouldn't actually use these options, only popular for servers. In any case, our 32-bit-wide SDRAM system can readily support 32-bit 33 MHz PCI while leaving cycles for the CPU, but would be swamped by fatter PCI.
- Support for memory interfaces other than SDRAM: DDRAM and RDRAM seem too exotic for embedded systems in the near future (and in the latter case, need a license). SDRAM seems likely to keep up with any plausible MIPS CPU bus. On the other hand, we started the design late enough that support of nonsynchronous DRAM did not look useful.

BONITO as Core IP

BONITO is written in synthesisable Verilog. It's already been compiled (using Synplicity) into a Xilinx FPGA

implementation and (using Synopsys tools) into an ASIC. The code is modular, though the division is not conventional - we observed that making a strict separation between the CPU interface and the SDRAM controller, for instance, leads to extra CPU cache refill latency and lower performance.

Along with the chip design we have a large test harness consisting of bus models of the devices to which BONITO attaches. The MIPS "CPU" bus model reads test scripts that exercise the virtual system, providing extensive test coverage even of difficult design points.

Algorithmics wrote all the synthesisable code, though the test harness does use a few freely redistributable files from other authors (special thanks to Micron for its SDRAM DIMM model, for instance). We will be very flexible about licensing.

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GT-64115

Universal PCI System Controller

Salient Features

▶ Integrates memory/device controller and PCI bridge in a single chip

▶ Supports NEC's VR43xx CPU

▶ Up to 75 MHz CPU and SDRAM bus frequencies

▶ Supports 16-, 64- and 128-Mbit SDRAM

▶ Parity support with read-modify-write cycles

▶ 32-bit, PCI 2.1 interface, up to 66 MHz

▶ Plug and play support

▶ Four Powerful DMA controllers

▶ Unified memory architecture (UMA) for shared memory applications

CPUs Supported

NEC VR43xx

Company Profile

Galileo Technology, the industry leader in system controllers for high-performance MIPS CPUs, offers the largest family of controllers for different CPU architectures and cost/performance targets. All devices are software-compatible, saving valuable development time.

Product Overview

The GT-64115 is designed to be cost-effective while maximizing total system performance. This device uses a three-bus architecture: CPU, memory and device, and PCI interface. These buses are decoupled from each other allowing simultaneous transactions, thus enhancing performance. Integrated powerful DMA controllers, 66 MHz PCI capability and a feature rich memory controller supporting address interleaving are just a few of the features that can be utilized to optimize data bandwidth throughout your system.

Galileo provides evaluation boards for the GT-64115 that can be used as a reference design to accelerate hardware development. Full schematics, manuals and sample code are available for each board. Board support packages for popular RTOSs, including

WindRiver's VxWorks, driver development tools and WindowsCE support tools, are also available to reduce software development time.

Memory
and
Devices

Embedded
MIPS CPUs

RM523x
RC4640
RC64474
VR4300

32-bit

Galileo
T E C H N O L O G Y
GT-64115

32-bit

SDRAM

ROM,
Flash
I/O

High Performance PCI Interface, Hot Swap Capable
32-bit, 66 MHz Supported
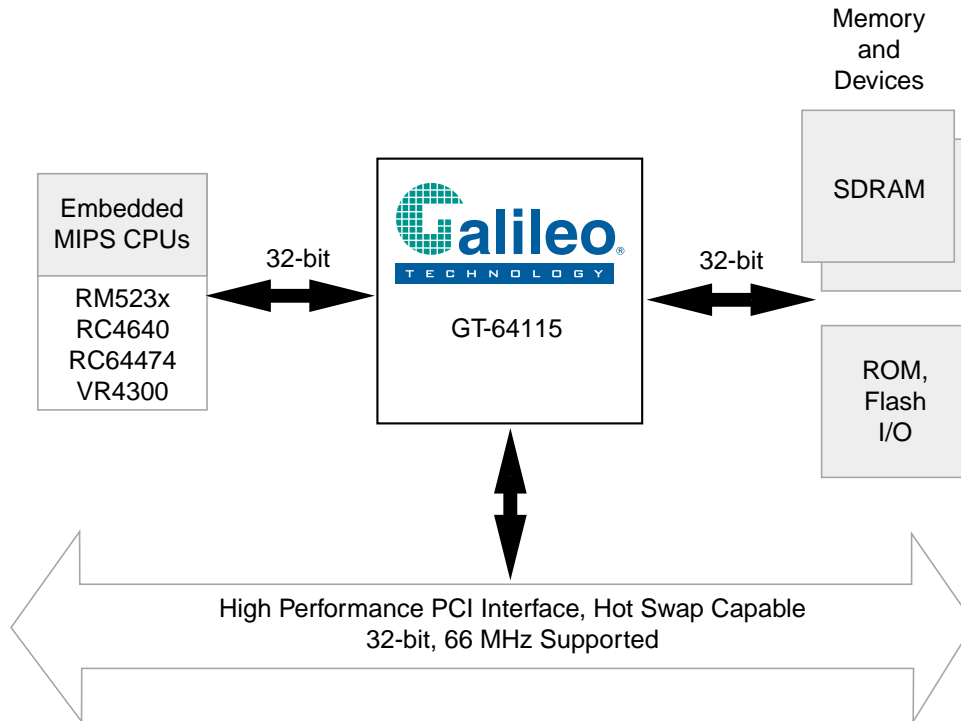
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Internet: http://www.galileoT.com

VRC4171A I/O and LCD Controller for the VR41xx Family

Product Overview

The VRC4171A™ is the companion chipset designed specifically for the VR4111/VR4121 and Microsoft Windows CE 2.0 specification. The VRC4171A incorporates an LCD graphic display controller, two PC Card controllers, and several general-purpose I/O (GPIO) pins. The combination of the VR4111/VR4121 and the VRC4171A is an excellent performance/cost solution for next-generation Windows CE applications. Together, they form the perfect engine for most, if not all, high-performance Windows CE-based handheld products.

Applications

- Handheld PC and PDA
- Smart phone and Internet/e-mail phone
- Personal GPS
- Battery-powered consumer embedded controller

Features

LCD Graphic Display Controller

- Supports color up to 64 KB shades (1, 2, 4, 5, 6, 8, 16 bits/pixel)
- Supports monochrome up to 16 gray-scale levels (1, 2, 4 bits per pixel)
- On-chip color palette RAM (256 x 18) and on-chip hardware cursor (32 x 32 x 2)
- Up to 640 x 480 resolution
- Supports single-scan and dual-scan STN and TFT LCD panels
- Supports analog TFT LCD and CRT interface (external D/A converter required)

Frame Buffer Memory

- Supports either 256 KB x 16, 1 MB x 16, or 2 x 256 KB x 16

Two PC Card Controllers

- Both controllers support ExCA and PCMCIA Ver. 2.1, Miniature Card (flash/ROM only), and CompactFlash Ver. 1.1

Salient Features

- Efficient color/monochrome LCD controller
- On-chip color palette RAM (256 KB x 18)
- On-chip hardware cursor (32 x 32 x 2)
- Both PC Card controllers support ExCA and PCMCIA version 2.1, Miniature Card, or CompactFlash™ specifications
- Up to four general-purpose I/O pins

CPUs Supported

NEC VR4111, VR4121

NEC

V$_{RC}$4171A Block Diagram

VR4111, VR4121

VRC4171A

16-Bit System Bus

XTAL Clock

Clock Divider

Config. Logic

PC Card, CompactFlash, Miniature Card Controller Slot B

PC Card, CompactFlash, Miniature Card Controller Slot A

Video DRAM

16

LCD Controller

Multifunction Pin Logic

GPIO

LCD Panel

PC Card, CompactFlash, Miniature Card

PC Card, CompactFlash, Miniature Card
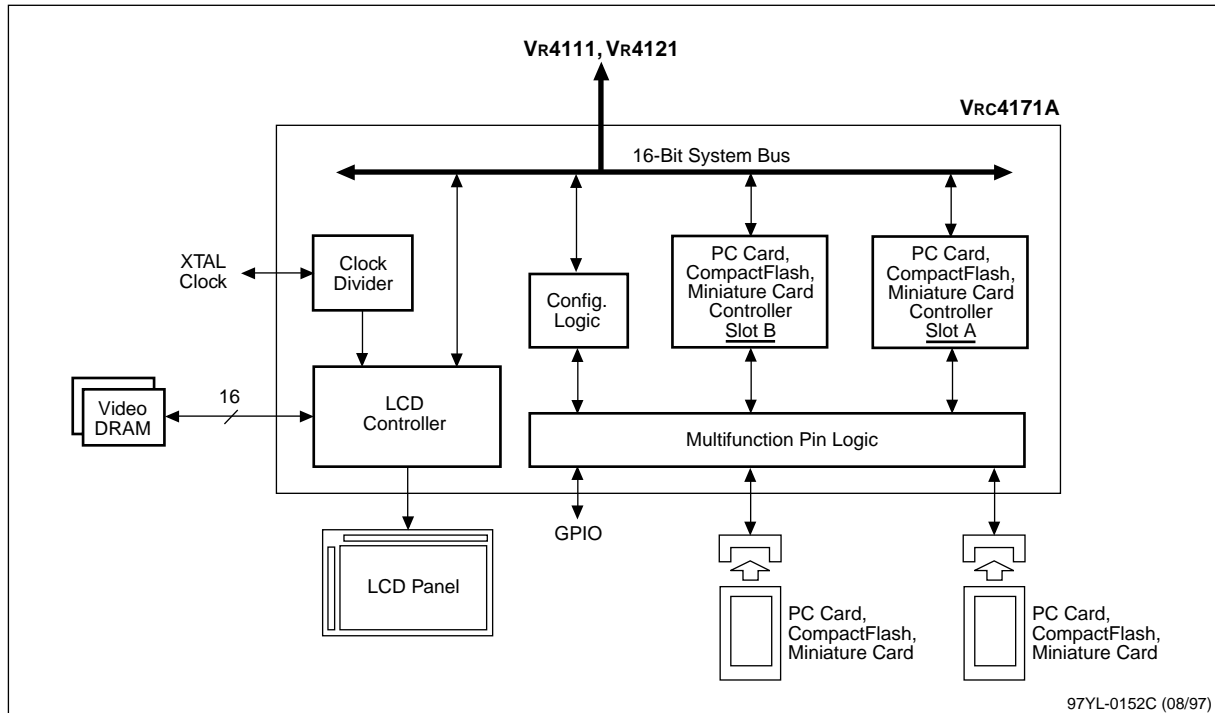
97YL-0152C (08/97)

General-Purpose I/O Pins

- Up to 4 GPIO pins are available for programming system inputs and/or outputs

208-Pin LQFP Package

AC/DC Specifications

- 3.0–3.6V operation
- 250 mW typical power consumption

Designed To Meet Windows CE 2.0 Specifications

Ordering Information

Part Number	Package
V$_{RC}$4171A	208-pin LQFP

Sample Windows CE Application Block Diagram
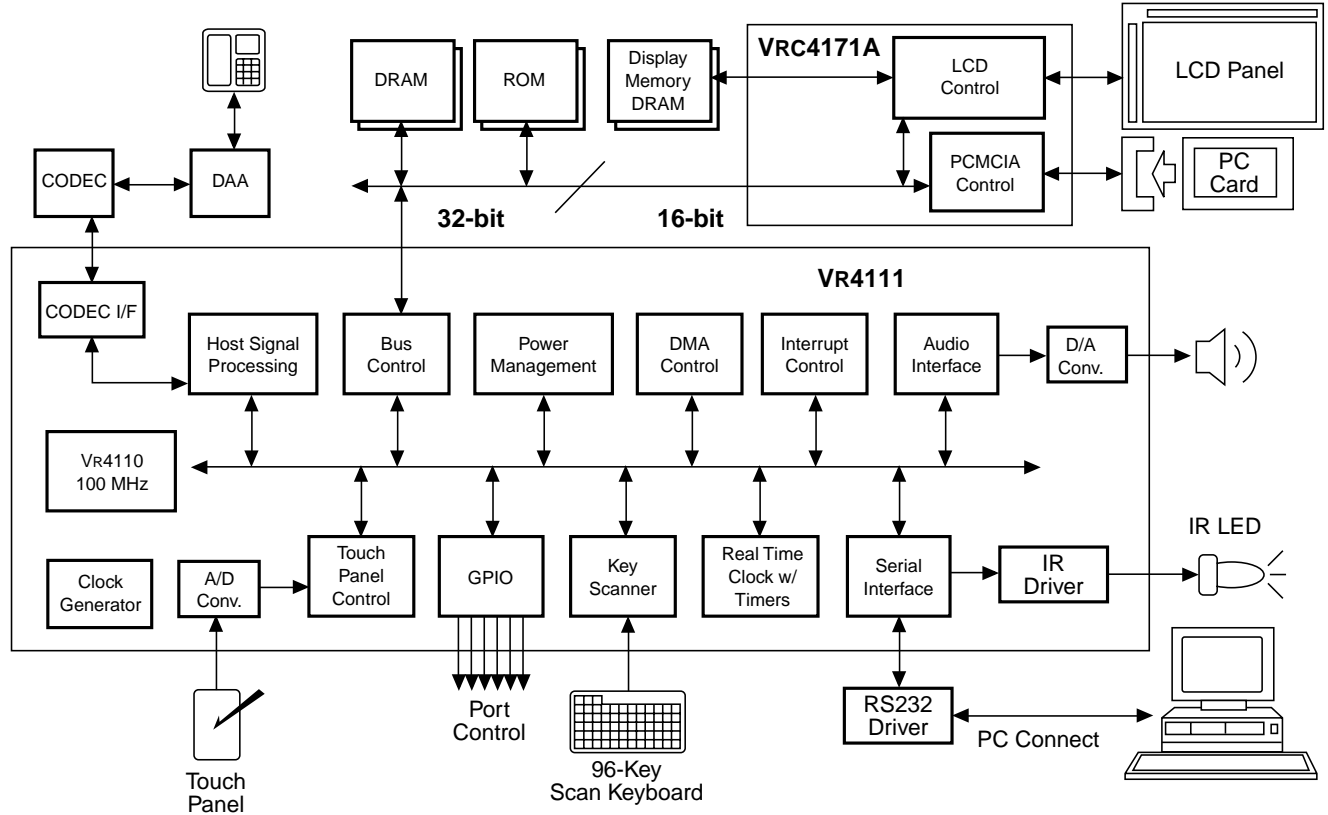
DRAM

ROM

Display Memory DRAM

VRC4171A

LCD Control

LCD Panel

CODEC

DAA

PCMCIA Control

PC Card

32-bit

16-bit

CODEC I/F

VR4111

Host Signal Processing

Bus Control

Power Management

DMA Control

Interrupt Control

Audio Interface

D/A Conv.

VR4110 100 MHz

Clock Generator

A/D Conv.

Touch Panel Control

GPIO

Key Scanner

Real Time Clock w/ Timers

Serial Interface

IR Driver

IR LED

Touch Panel

Port Control

96-Key Scan Keyboard

RS232 Driver

PC Connect

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VRC4172 Companion Chip for the VR4121

Salient Features

◗ Efficient 32-bit color/monochrome LCD controller

◗ Pulse width modulation for LCD backlight

◗ 16-bit mini-ISA bus interface

◗ DRAM interface and SDRAM controller

◗ USB host controller with 48 MHz system clock

◗ IEEE-1284 parallel port interface and two 16550-compatible serial port interface units

◗ Six programmable chip selects and 24 general-purpose I/O signals

◗ PS/2 keyboard and mouse support

CPUs Supported

NEC VR4121

Product Overview

The VRC4172™ companion chip to NEC's VR4121™ MIPS® RISC microprocessor is designed for high-end Windows® CE Handheld PC Professional applications.

The VR4121 microprocessor functions as the host CPU, while the VRC4172 supplies the SDRAM interface, USB interface, host- and peripheral-selectable IEEE-1284 parallel interface, 16550-compliant serial interface, PS/2 interface, general-purpose I/O ports, general-purpose chip-select signal, and pulse width modulation for the LCD backlight.

In combination, the VR4121 and VRC4172 offer an excellent performance/cost solution for next-generation Windows CE applications, forming a superior engine for most, if not all, high-performance Windows CE-based handheld products.

Applications

• Handheld PC and PDA

• Smart phone and Internet/e-mail phone

• Personal GPS

• Battery-powered consumer embedded controller

Features

Processor Interface

• 32-bit LCD interface

• 16-bit mini-ISA bus interface (as defined by VR4121)

• DRAM interface and SDRAM controller for DMA/master mode

USB Host Controller

• OpenHCI USB 1.0 compliant

• Standard communication with USB device; asynchronous communication with host CPU

• Full-speed (12 Mbps) and low-speed (1.5 Mbps) operation

• 48 MHz system clock

• On-chip FIFO
   — PCI read: 4 x 4 Dword
   — PCI write: 4 x 4 Dword
   — USB side: 64 x 1 byte

• Two downstream ports

• No support for legacy interface

IEEE-1284 Parallel Port Interface

• ECP, EPP, SPP, and P1284 host function with DMA operation

• Device function operation

NEC

VRC4172 Block Diagram
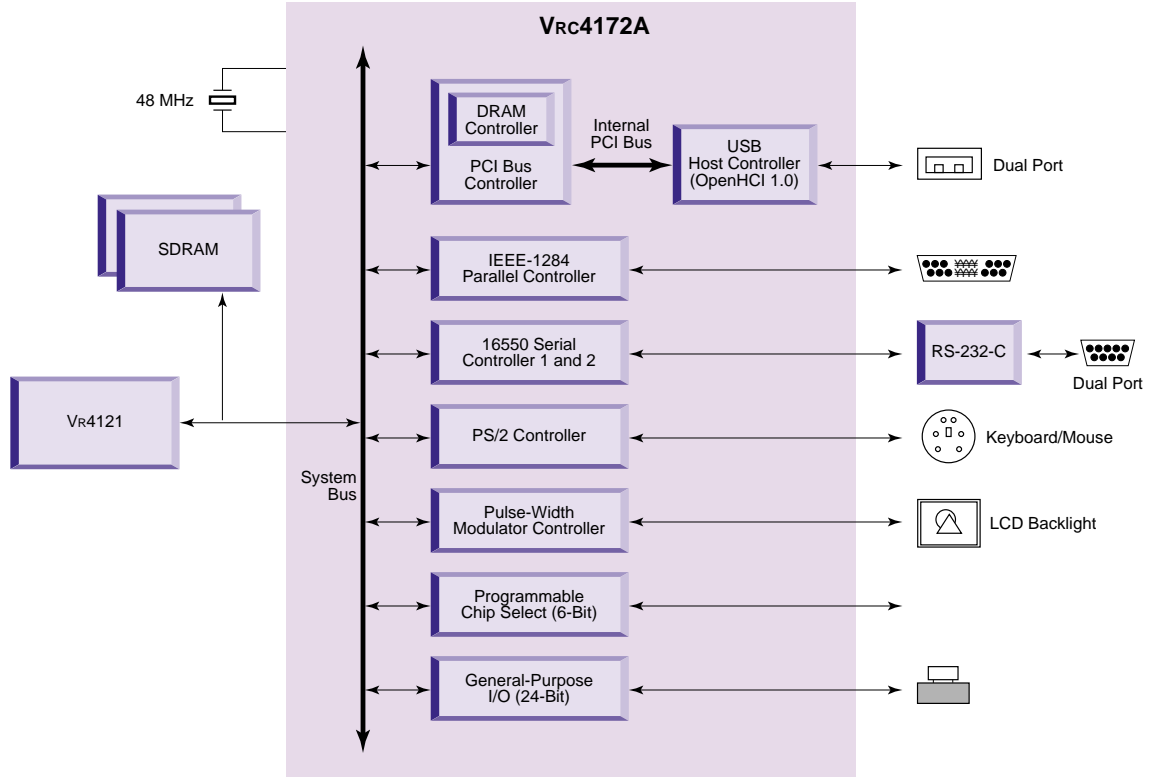
Serial Port Interface

- Two 16550-compatible serial interfaces

Programmable Chip Select and General-purpose I/O

- Six chip selects
- 24 general-purpose I/O (GPIO) signals

PS/2 Interface

- PS/2 keyboard and mouse support

Pulse-Width Modulation (PWW) for LCD Backlight

Package

- 256-pin TBGA (27 mm square)

Ordering Information

Part Number	Package
VRC4172	256-pin TBGA (27 mm square)

Example of Windows CE Handheld Professional Implementation
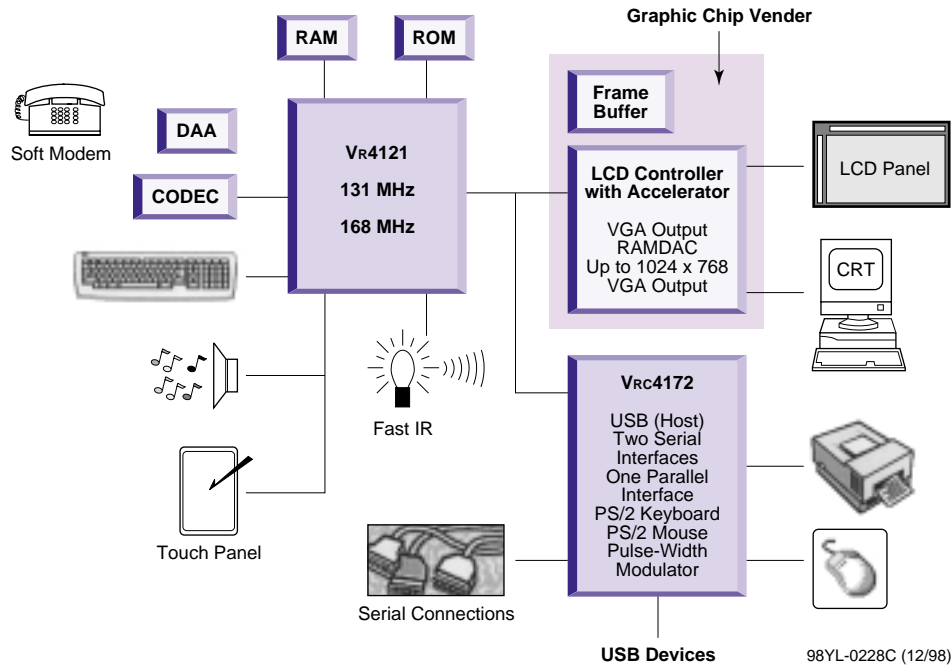
Graphic Chip Vender

RAM

ROM

Soft Modem

DAA

CODEC

VR4121

131 MHz

168 MHz

Frame Buffer

LCD Controller with Accelerator

VGA Output
RAMDAC
Up to 1024 x 768
VGA Output

LCD Panel

CRT

Fast IR

Touch Panel

VRC4172

USB (Host)
Two Serial
Interfaces
One Parallel
Interface
PS/2 Keyboard
PS/2 Mouse
Pulse-Width
Modulator

Serial Connections

USB Devices

98YL-0228C (12/98)

Contact List

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VRC4173 Companion Chip for the VR4122

Salient Features

▶ 32-bit PCI bus operating at 33 MHz

▶ Two-port, two-speed USB host controller

▶ Two-slot PC Card™ controller with built-in FIFO

▶ AC97 audio codec interface with DMA support

▶ Keyboard controller (96 key)

▶ 10-bit D/A converter and 12-bit A/D audio controller

▶ Touch-panel controller

CPUs Supported

NEC VR4122

Product Overview

The VRC4173™ is a companion chip designed to be used with NEC's VR4122™ 64-bit MIPS® RISC microprocessor. The VRC4173 incorporates the I/O macros necessary for a handheld PC running Microsoft® Windows® CE, and can also access design resources on a personal computer by means of the PCI bus interface. With the VR4122 acting as the host CPU, the VRC4173 functions include PCI bus interface, USB host controller, two-slot PCI Card™ controller, AC97 interface, keyboard controller, 10-bit D/A converter, 12-bit A/D audio controller, touch-panel controller, general-purpose I/O pins, and built-in 48 MHz oscillator.

The VR4122 and VRC4173 provide an excellent performance/cost solution for Windows CE handheld PC Pro applications. They also form an ideal engine for most high-performance Windows CE-based handheld products.

Features

Processor Interface

- 32-bit PCI bus operating at 33 MHz
- CLKRUN signal support

USB Host Controller

- Compliant with OpenHCI release 1.0 specification
- Two-port, two-speed (12 Mbps, 1.5 Mbps)
- Built-in FIFO
  — PCI read: 4 x 4 Dword
  — PCI write: 4 x 4 Dword
  — USB side: 64 x 1 byte
- Two downstream ports
- No support for legacy interface

PC Card Controller

- Compliant with the 1997 PC Card standard
- Two PC Card slots
- Buffer with a 5-volt withstand voltage
- Interface for an external power supply control IC

AC Link Interface

- AC link conforming to the audio codec (AC97) standard, Rev. 2.1
- DMA support

Keyboard Controller

- 96-key keyboard
- VR4121 keyboard interface unit compatible

Audio Controller

- Reproduction: 10-bit D/A converter
- Recording: 12-bit A/D converter
- VR4121 audio interface unit compatible

Touch-Panel Controller

- Touch-panel driver, coordinate detection (12-bit A/D converter)
- One general-purpose analog input port
- VR4121 panel interface unit compatible

NEC

VRC4173 Block Diagram
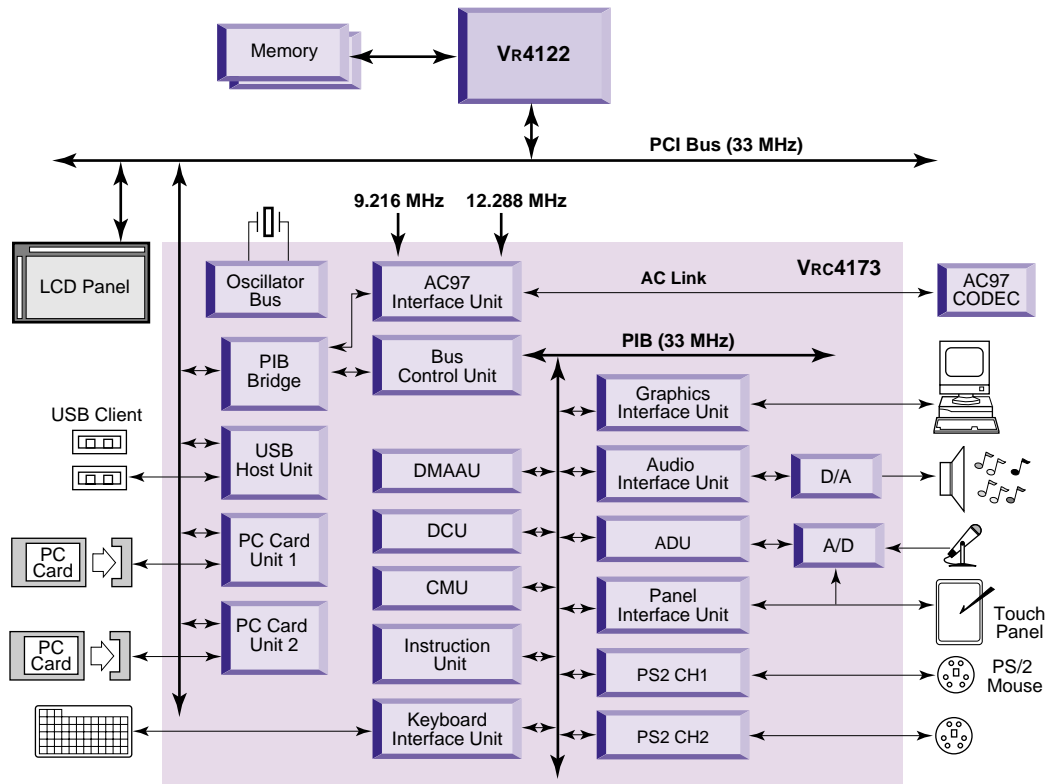
General-purpose I/O Pins

- Total of 21 pins
- VR4121 general-purpose I/O interface unit compatible

Miscellaneous

- Built-in 48 MHz oscillator with 48 MHz clock output
- CB-C9VX (UC1H) process
- 3.3-volt, single-voltage power supply (some internals with 5.0-volt withstand voltage)
- 304-pin FPBGA package (19 x 19 mm, 0.8-mm pitch)

Ordering Information

Part Number	Package
μPD31173F1-33-H/N	304-pin FPBGA (19 x 19 mm)

Example of Handheld PC Pro Application Using VR4122 with VRC4173
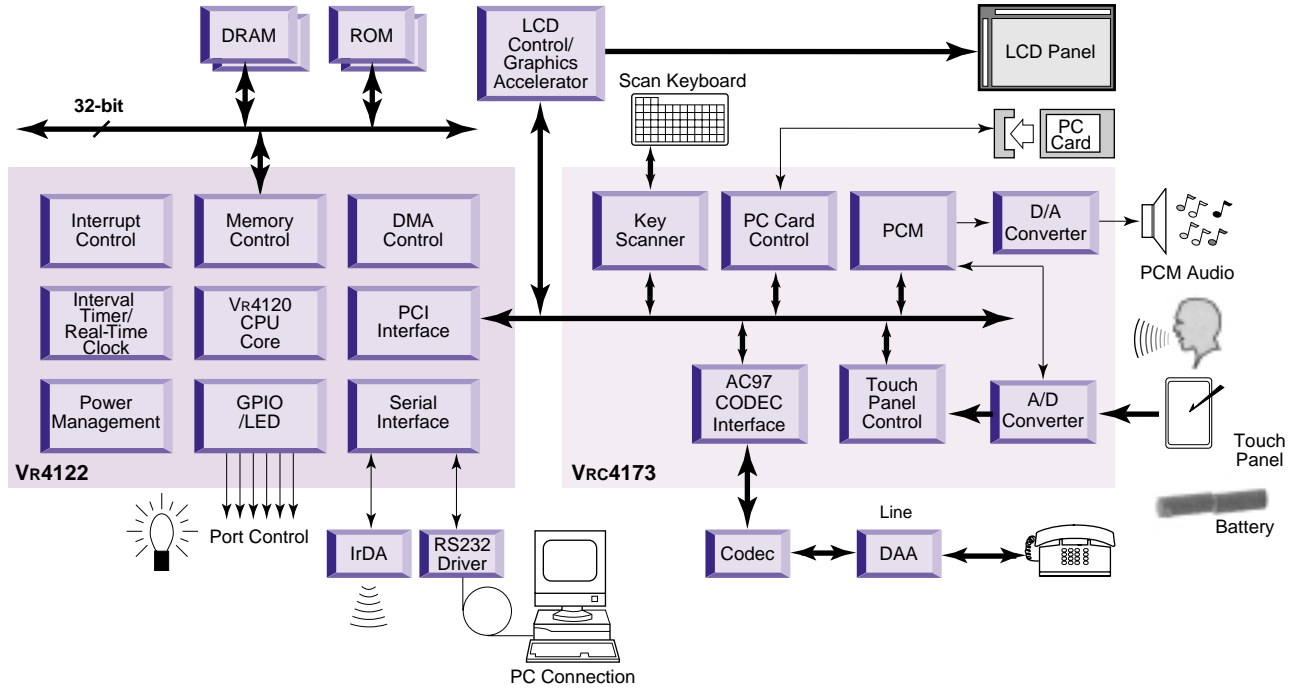
Contact List

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VRC4372
I/O Controller for the
VR43xx Family

Salient Features

▸ PCI arbitration for six external and one internal PCI masters

▸ Timer and beeper source

▸ ISA-like I/O bus

▸ Four independent DMA channels

▸ Ten chip selects

▸ N-to-3 interrupt controller

▸ Interrupts generated from 14 input pins and two internal timers

▸ Test port to place chip in scan mode

▸ 3.3-volt compliant and 5-volt tolerant

▸ 33 MHz bus frequency

CPUs Supported

NEC VR43xx

Product Overview

The VRC4372™ is a PCI-based I/O controller for a high-performance, low-cost system implementation based on the VR43xx microprocessor. The VRC4372 contains the functional blocks described below.

PCI Bus Interface Controller

• Compliance with 3.3-volt PCI interface standards (version 2.1)

• 5-volt PCI signaling in a controlled environment (with voltage spikes less than 7.6 volts and DC levels less than 6.6 volts)

• PCI bus arbitration for six external and one internal PCI masters

I/O Controller

• 16-bit ISA-like I/O bus and four independent DMA channels

• Chip-select and control signals for interfacing to external peripheral chips

• N-to-3 interrupt controller (interrupts from the keyboard and mouse, 14 input pins, two internal timers, and four DMA channels can be encoded onto one of three outgoing interrupt lines)

• Four programmable DMA channels
  — Unique TCn, EOP, DREQ, and DACKn signals on each channel
  — Block or single transfers
  — Read or write requests
  — I/O-device-demanded service requests via DREQx
  — Software-initiated requests
  — Channel suspend via the MASKn register bit
  — I/O device transfer termination via EOP
  — Channel reload notification and termination notification via an interrupt
  — Efficient PCI bus data packing mode
  — Byte/short scattering/gathering capabilities (one per PCI word)

Each channel has registers and status bits associated with its control and operation. A current address and current count register pair are used to address the current DMA buffer in PCI memory space. A reload start and reload count register pair provide a reload mechanism through which channel chaining can be accomplished. Fifth and sixth registers provide the channel with mode and status control.

A global control register specifies global DMA attributes such as arbitration scheme selection.

NEC

Miscellaneous I/O

- Timer and beeper source
- General-purpose control and I/O status signals
- Reserved pins for two USB interfaces (2 x 2 pins) and one P1394 interface (four pins)

PCI Arbitration

The VRC4372 has an internal PCI arbiter that can be configured by setting the ARB pin high to arbitrate among six requesters (five external and one internal) according to the bits programmed in the PAPC register.

Ordering Information

Part Number	Package
VRC4372-1	208-pin PQFP

Contact List

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VRC4373 PCI Interface Controller for the VR43xx Family

Description

The VRC4373™ is a single-chip device that provides a glueless interface between a VR43xx microprocessor, a DRAM memory system, and a standard PCI bus.   The VRC4373 interface controller connects directly to the VR43xx microprocessor and the PCI bus with no buffering required. The VRC4373 contains the interface logic necessary to drive several types of DRAMs at various speeds. The interface control logic is highly configurable by software and requires minimal hardware configuration for use in many different types of systems.

VR4300 Interface

- Glueless interface to the VR4300/VR4305/VR4310
- 3.3-volt I/O
- Compatible with all VR43xx bus cycle types and combinations
- Little-endian byte ordering

Programmable Memory Interface

- Base memory plus four SIMMs™
- Programmable address ranges for base memory and each SIMM
- Base memory range supports SDRAM and EDO DRAM
- SIMM memory range supports SDRAM, EDO, fast-page DRAM, and flash
- Flash memories and fast-page and EDO in each range
- Up to 4 MB of SDRAM supported in base memory

- Several speed grades
- 66 MHz little-endian memory bus
- Interleaved or noninterleaved base memory
- Interleaved or noninterleaved SIMMs
- Interleaving buffers internal to the VRC4373
- Open DRAM page in base memory
- Built-in refresh generation
- 3.3-volt inputs; 5-volt-tolerant outputs

PCI Interface

- Master and slave capability
- Host bridge and add-in card support
- PCI arbiter
- 133 Mbps burst cycles
- No interrupt support
- 3.3-volt PCI-compliant inputs and 5-volt-tolerant outputs
- 33 MHz PCI bus clock rate

DMA Controller

- Block transfers between memory and PCI
- 8-word (32-byte) bidirectional buffer
- Two sets of control registers for chained operation
- Unaligned transfers at maximum PCI bandwidth
- A maximum of 1 MB of data can be transferred

Boot ROM

- Up to 16 MB of boot ROM
- ROM address/data lines multiplexed on DRAM data lines
- Write protection
- VRC4373 can also boot from SIMM

Contact List

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NEC

VRC4375 PCI Interface Controller for the VR43xx Family

Description

The VRC4375™ system controller is a software-configurable chip that directly interfaces to the VR4300/VR4305/VR4310 CPU and PCI bus without external logic or buffering. It also interfaces memory (SDRAM, EDO, fast-page DRAM, and flash boot ROM) with minimal buffering. From the viewpoint of the VR43xx CPU, the VRC4375 acts as a memory controller, DMA controller, and PCI bridge. From the viewpoint of PCI agents, the VRC4375 acts as either a PCI bus master or a PCI bus target. Alternatively, the VRC4375 may be located on a PCI bus add-on board.

CPUs Supported

NEC VR43xx

CPU Interface

- Direct connection to the 66 MHz VR43xx CPU's buses
- 3.3 V I/O
- Support for all VR43xx bus cycles
- Little-endian or big-endian byte order

Memory Interface

- Support for boot ROM/flash memory, base memory, and up to two SIMMs
- Each SIMM can be up to 128 MB
- Programmable address ranges for base memory and SIMM memory
- Support for 4/16 Mb 2-bank devices, 64 Mb, 128 Mb, and 256 Mb 4-bank devices
- 66 MHz memory bus
- 64 MB base memory range: SDRAMs and EDO DRAMs
- 256 MB SIMM memory range: SDRAMs, EDO, and fast-page DRAMs
- Several speed grades supported within each memory range
- Single main memory bank supports up to 256 MB
- Open DRAM page maintained within base memory
- 8-word (32-byte) write FIFO (CPU to memory)
- 2-word (8-byte) prefetch FIFO (memory to CPU or memory to PCI)
- On-chip DRAM and SDRAM refresh generation
- Supports up to 64 MB of write-protectable boot ROM or up to 64 MB of flash memory
- Flash/boot ROM devices with 8/16/32-bit configuration support
- Boot ROM address and data signals multiplexed on memory data/address bus
- 3.3 V inputs; 5 V-tolerant outputs

PCI Interface

- Master and target capability
- Host bridge and add-on board modes
- PCI bus arbiter with programmable arbitration scheme
- Programmable arbitration scheme for PCI/CPU access to memory
- Big endian or little endian
- 4-word (16-byte) bidirectional PCI master FIFO (CPU is PCI bus master)
- 8-word (32-byte) bidirectional PCI target FIFO (memory is PCI bus target)
- 33 MHz PCI bus clock rate
- 132 MB/sec burst transfers
- Interrupt support for add-on board mode
- 3.3 V PCI-compliant inputs; 5 V-tolerant inputs/outputs

NEC

DMA Controller

- Four highly robust DMA channels
- CPU-initiated block transfers between memory and PCI bus
- 8-word (32-byte) bidirectional DMA FIFO
- Sophisticated DMA channels arbitration priority scheme, programmable
- Four sets of DMA control registers for chained transfers
- Next address pointer in each channel to support scatter/ gather operation
- Programmable DMA arbitration priority
- Bidirectional unaligned transfers
- Transfers at maximum PCI bandwidth of 132 MB/s

Interrupt Controller

- Generates NMI and INTR
- All interrupt-causing events maskable

UART

- NY16550L Universal Asynchronous Receiver/Transmitter
- Modem control functions
- Separate receiver and transmitter FIFOs, 16 bytes each
- Even, odd, or no parity bit generation
- Fully prioritized interrupt control

Timers

- One 32-bit loadable watchdog timer generating NMI*
- Two 32-bit loadable general purpose timers generating Int#
- All timers highly sophisticated with programmable clock frequency, start/stop, auto reload/restart, enable/disable interrupt bits

Testability

- Wiggle test to isolate disconnection between the I/O pin and corresponding PCB trace

Ordering Information

Part Number	Package
uPD65948S1-068	256-pin TGBA

Contact List

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VRC5074 PCI Interface Controller for the VR5000

Description

The VRC5074™ is a single-chip device that provides a glueless interface between a VR5000™ processor and an SDRAM memory system, a local I/O bus, and a standard PCI bus. The VRC5074 interface controller connects directly to the VR5000 microprocessor and PCI bus with no buffering required. The SDRAM memory interface contains the logic required to drive several types and speeds of SDRAM directly. The interface control logic is highly configurable by software and can be used with no or minimal hardware configuration in several different types of systems. The highly programmable local bus interface connecting to general-purpose I/O devices contains the interface logic necessary to drive several types and speeds of peripheral devices directly.

VR5000 Interface - 100 MHz SysAD

- Glueless interface to VR5000 microprocessor
- Can be configured to operate without the CPU as stand-alone PCI and memory controller
- Support for all VR5000 bus cycle types and combinations (pipelined write only supported for nonblock writes)
- Fifteen interrupt sources, individually enabled and individually assigned to one of the VR5000's seven interrupt pins
- Big-endian or little-endian operation
- Multiple VRC5074s supported with a single VR5000
- Sixteen-deep dedicated FIFOs
- Secondary cache controller support
- 3.3-volt I/O

Internal Registers

- Physical device address registers with flexible physical address decoding for local I/O devices, memory, and PCI devices
- VR5000 CPU control registers
- Main memory control registers
- PCI control registers
- Local bus interface control registers
- DMA controller registers
- Interrupt controller registers
- UART control registers
- Timer registers
- PCI configuration registers

Main Memory Interface - 100 MHz

- Up to 512 MB of total physical memory supported. Glueless to standard SDRAMs.
- Two physical banks of SDRAM supported
  — Programmable address ranges, device type for each bank
  — Interleaved or noninterleaved (interleaving buffers internal to the VRC5074)
- Four types of SDRAM: four-bank 256 MB and 64 MB; two-bank 64 MB and 16 MB
- Multiple open SDRAM pages
- ECC or parity check
- Built-in refresh operation
- 3.3-volt outputs; 5-volt tolerant inputs

PCI Interface 66/33 MHz @ 32/64 Bit

- Compatible with PCI Bus Specification (Rev. 2.1)
- Four possible configurations
  — 64-bit bus @ 66 MHz
  — 32-bit bus @ 66 MHz
  — 64 bit @ 33 MHz
  — 32 bit @ 33 MHz
- 3.3-volt compliant; 5-volt tolerant
- Initiator capability for CPU, DMA, and local bus master. Up to 5 external masters supported.
- Two programmable address windows
- Target capability for access to all VRC5074 resources
- Eleven programmable address windows controlled by BARs (base address registers)

NEC

- Four simultaneous delayed read cycle transactions
- 32-deep, 8-byte-wide output FIFOs with address/data from the VRC5074 initiator to the PCI
- 32-deep, 8-byte-wide input FIFOs with address/data from the PCI to the VRC5074 resources
- Full target and initiator burst support
- Burst lengths of up to 2 MB for both read and write cycles
- Optional PCI central resource services
  — Arbitration for five other PCI devices
  — Four PCI interrupt lines plus one sideband interrupt
- PCI clock buffered to five other PCI devices
- PCI clock derived from CPU clock or external source
- 64-bit addressing with dual address cycle (target and initiator)
- Semaphore operation (locked cycles) as target and initiator
- Full configuration space for stand-alone operation

Local I/O Interface (PCI Configured for 32 Bits)

- Full operation at 50 MHz or 25 MHz
- Seven programmable device chip selects and one boot ROM chip select
- Very flexible bus control signal relationships and duration
- Fixed internal timing or optional external ready/acknowledge signal
- External local bus master support
- Chip-select support for up to 4 GB of address space
- Local I/O available only if 32-bit PCI bus is used
- 3.3-volt outputs; 5-volt-tolerant inputs

DMA Controller - 2 Independent Controllers

- Block transfers from/to any physical address and from/to any bank
- 32-D word (256-byte) buffer
- Two sets of control registers for chained operation
- All combinations of aligned or unaligned transfers supported
- Transfers at maximum PCI bandwidth
- Each channel supports up to 1 megabyte of data transfer
- Hardware handshaking supported for transferring data to/from slow local I/O devices
- DMA can be suspended and restarted

UART

- NY16550L Universal Asynchronous Receiver/Transmitter (UART)
- Compatibility with National Semiconductor's NS16550D
- 16-byte receiver and transmitter FIFOs
- Fully programmable serial interface characteristics
  — 5-, 6-, 7-, and 8-bit characters
  — Even, odd, or non-parity bit generation and detection
  — 1, 1-1/2, or 2 stop-bit generation
  — Baud rate generation
  — Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Programmable baud rate generator controlled by input clock divided by 1 to $(2^{16}) - 1$
- Fully prioritized interrupt system controls

Timers

- 16-bit SDRAM refresh timer, programmable
- 64-bit bus read time-out timer
- 32-bit general-purpose timer
- 32-bit watchdog timer
- All timers cascadable

Multi-Controller Support

System can be configured as a single controller or multicontroller

Ordering Information

Part Number	Package
VRC5074	500-pin BGA

VRC5074 Block Diagram
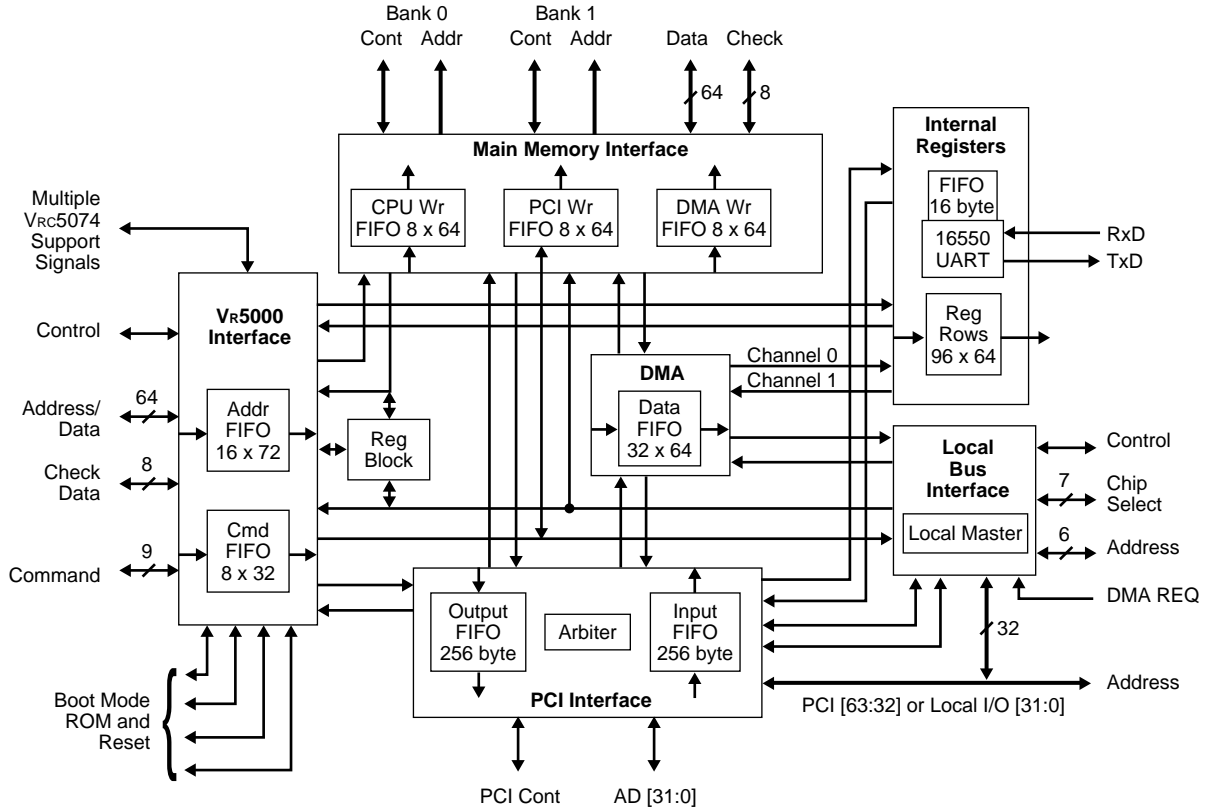
Bank 0 — Cont, Addr
Bank 1 — Cont, Addr
Data, Check

64, 8

Main Memory Interface

CPU Wr FIFO 8 x 64
PCI Wr FIFO 8 x 64
DMA Wr FIFO 8 x 64

Multiple VRC5074 Support Signals

Control

Address/Data — 64
Check Data — 8
Command — 9

VR5000 Interface

Addr FIFO 16 x 72

Cmd FIFO 8 x 32

Reg Block

DMA
Data FIFO 32 x 64

Channel 0
Channel 1

Output FIFO 256 byte
Arbiter
Input FIFO 256 byte

PCI Interface

Boot Mode ROM and Reset

PCI Cont   AD [31:0]

Internal Registers
FIFO 16 byte
16550 UART
Reg Rows 96 x 64

RxD
TxD

Local Bus Interface
Local Master

Control
Chip Select — 7
Address — 6
DMA REQ

32

Address

PCI [63:32] or Local I/O [31:0]

Contact List

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VRC5077
System Controller
for the VR5000

Description

The VRC5077™ is a single-chip device that provides a glue-less interface between a VR5000™ processor and an SDRAM memory system, a local I/O bus, and a standard PCI bus. The VRC5077 interface controller connects directly to the VR5000 microprocessor and PCI bus with no buffering required. The SDRAM memory interface contains the logic required to drive several types and speeds of SDRAM directly. The interface control logic is highly configurable by software and can be used with no or minimal hardware configuration in several different types of systems. The highly programmable local bus interface connecting to general-purpose I/O devices contains the interface logic necessary to drive several types and speeds of peripheral devices directly.

VR5000 Interface - 100 MHz SysAD

- Glueless interface to VR5000 microprocessor
- Can be configured to operate without the CPU as stand-alone PCI and memory controller
- Support for all VR5000 bus cycle types and combinations (pipelined write only supported for nonblock writes)
- Fifteen interrupt sources, individually enabled and individually assigned to one of the VR5000's seven interrupt pins
- Big-endian or little-endian operation
- Multiple VRC5077s supported with a single VR5000
- Sixteen-deep dedicated FIFOs
- Secondary cache controller support
- 3.3-volt I/O

Internal Registers

- Physical device address registers with flexible physical address decoding for local I/O devices, memory, and PCI devices
- VR5000 CPU control registers
- Main memory control registers
- PCI control registers
- Local bus interface control registers
- DMA controller registers
- Interrupt controller registers
- UART control registers
- Timer registers
- PCI configuration registers

Main Memory Interface - 100 MHz

- Up to 512 MB of total physical memory supported. Glue-less to standard SDRAMs.
- Two physical banks of SDRAM supported
  — Programmable address ranges, device type for each bank
  — Interleaved or noninterleaved (interleaving buffers internal to the VRC5077)
- Write protection from unauthorized writes to protected region in SDRAM. Up to 16 MB range.
- CPU interrupted and illegal address captured when write protection violation occurs
- Four types of SDRAM: four-bank 256 MB and 64 MB; two-bank 64 MB and 16 MB
- Multiple open SDRAM pages
- ECC or parity check
- Built-in refresh operation
- 3.3-volt outputs; 5-volt-tolerant inputs

PCI Interface 66/33 MHz @ 32/64 Bits

- Compatible with PCI Bus Specification (Rev. 2.1)
- PCI interface can be configured for native little-endian or big-endian data format
- Four possible configurations
  — 64-bit bus @ 66 MHz
  — 32-bit bus @ 66 MHz
  — 64 bit @ 33 MHz
  — 32 bit @ 33 MHz
- 3.3-volt compliant; 5-volt tolerant

NEC

- Initiator capability for CPU, DMA, and local bus master. Up-to 5 External masters supported
- Two programmable address windows
- Target capability for access to all VRC5077 resources
- Eleven programmable address windows controlled by BARs (base address registers)
- Four simultaneous delayed read cycle transactions
- 32-deep, 8-byte-wide output FIFOs with address/data from the VRC5077 initiator to the PCI
- 32-deep, 8-byte-wide input FIFOs with address/data from the PCI to the VRC5077 resources
- Full target and initiator burst support
- Burst lengths of up to 2 MB for both read and write cycles
- Optional PCI central resource services
  — Arbitration for five other PCI devices
  — Four PCI interrupt lines plus one sideband interrupt
- PCI clock buffered to five other PCI devices
- PCI clock derived from CPU clock or external source
- 64-bit addressing with dual address cycle (target and initiator)
- Semaphore operation (locked cycles) as target and initiator
- Full configuration space for stand-alone operation

Local I/O Interface (PCI Configured for 32 Bits)

- Full operation at 50 MHz or 25 MHz
- Seven programmable device chip selects and one boot ROM chip select
- Very flexible bus control signal relationships and duration
- Fixed internal timing or optional external ready/acknowledge signal
- External local bus master support
- Chip-select support for up to 4 GB of address space
- Local I/O available only if 32-bit PCI bus is used
- 3.3-volt outputs; 5-volt-tolerant inputs

DMA Controller - 2 Independent Controllers

- Block transfers from/to any physical address and from/to any bank
- 32-Dword (256-byte) buffer
- Two sets of control registers for chained operation
- All combinations of aligned or unaligned transfers supported
- Transfers at maximum PCI bandwidth

- Each channel supports up to 1 megabyte of data transfer
- Hardware handshaking supported for transferring data to/from slow local I/O devices
- DMA can be suspended and restarted

UART

- NY16550L Universal Asynchronous Receiver/Transmitter (UART)
- Compatibility with National Semiconductor's NS16550D
- 16-byte receiver and transmitter FIFOs
- Fully programmable serial interface characteristics
  — 5-, 6-, 7-, and 8-bit characters
  — Even, odd, or non-parity bit generation and detection
  — 1, 1-1/2, or 2 stop-bit generation
  — Baud rate generation
  — Modem control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Programmable baud rate generator controlled by input clock divided by 1 to (216) - 1
- Fully prioritized interrupt system controls

Timers

- 16-bit SDRAM refresh timer, programmable
- 64-bit bus read time-out timer
- 32-bit general-purpose timer
- 32-bit watchdog timer
- All timers cascadable

MultiController Support

- System can be configured as a single controller or multicontroller

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VRC5476 PCI Interface Controller for the VR5432

Description

The VRC5476™ system controller is a software-configurable chip that directly connects the VR5432 CPU to SDRAM memory, a PCI bus, and a local bus, without external logic or buffering. From the CPU's viewpoint, the controller acts as a memory controller, DMA controller, PCI bus host bridge, and local bus host bridge. From the viewpoint of PCI agents, the controller acts as master and target on the PCI bus. The controller also has one serial port and four timers.

CPU Interface

- Connects directly to 167/133 MHz VR5432 CPUs
- 83/66 MHz CPU bus
- Peak blocktransfer throughput of 332 Mbytes/sec, maximum sustained throughput of 266 Mbytes/sec
- Four word x 32 deep (128-byte) CPU-to-controller FIFO
- Little-endian or big-endian byte ordering on CPU interface
- Thirteen interrupt sources, individually enabled and assigned to one of the CPU's five interrupt inputs and one non-maskable interrupt
- Supports all CPU buscycle types. Parity generation and checking on CPU data cycles.
- 3.3 V I/O

Memory Interface

- 83/66 MHz memory bus
- Maximum sustained throughput of 332 Mbytes/sec
- Supports four physical loads per data bit: One SDRAM physican bank and one other (e.g., EPROM, Flash, or buffers bridging to a secondary memory bus)
- Supports four types of SDRAM with two to four on-chip virtual banks: 256 Mb four-bank, 64 Mb two-bank, 16 Mb two-bank
- Programmable address ranges for memory bank
- Memory may maintain multiple open SDRAM pages
- Read/write buffers:
  — 8-word (32-byte) CPU write FIFO
  — 8-word (32-byte) PCI write FIFO
- On-chip refresh generation
- 3.3 V I/O

PCI Bus

- Full compliance with *PCI Local Bus Specification, Revision 2.1*
  — 33 MHz, 32-bit bus (maximum sustained bandwidth 132 Mbytes/sec)
- PCI master support, allowing the CPU, DMA, and local bus masters to access targets on the PCI bus via two programmable PCI address windows
- PCI target support, allowing PCI bus masters to access all controller resources
  — Nine programmable Base Address register (BAR) windows
  — All reads are delayed transactions
  — Up to four simultaneous delayed transactions
- Master and target read/write bursts up to 2 Mbytes in length
- Master and target read/write buffers:
  — 32-entry x 4-byte (128-byte) PCI output FIFO
  — 32-entry x 4-byte (128-byte) PCI input FIFO
  — 8-entry x 4-byte (32-byte) CPU delayed read completion (DRC) buffer
  — 8-entry x 4-byte (32-byte) DMA delayed read completion (DRC) buffer
- Optional PCI central resource functions:
  — Buffered PCI clock to 4 other PCI devices
  — PCI clock can be external or derived from CPU clock
  — Arbitration for the controller and 4 other PCI devices
  — CPU interrupt control for 4 PCI devices

NEC

- Full PCI configuration space
- Locked cycle (exclusive access) support as master and target
- Parity generation and checking on address and data cycles
- Compliant with both 3.3 V and 5 V PCI signaling

Local Bus

- 42 MHz or 21 MHz bus (0.25 or 0.50 of system clock)
- Programmable chip selects for 5 devices plus boot ROM
  — Each chip select supports up to 4 GB address space
  — Devices may alternatively be located on the memory bus
  — Chip select may alternatively be used for DMA or UART control, or as general-purpose I/O signals
- Support for burst cycles on the local bus
- Support for local bus master control of the local bus, using 68000 or Intel arbitration protocols
- Programmable control-signal relationships and timing:
  — Timing can be fixed or use external Ready signal
  — 12-bit timer for external Ready signal
- 3.3 V outputs, 5 V-tolerant inputs

DMA

- Four DMA channels with link list capability
- Block transfers to or from any physical address
- Transfers initiated by the CPU, a PCI bus master, or a local bus master
- Peak block transfer throughput of 332 Mbytes/sec, maximum sustained throughput of 266 Mbytes/sec
- 64 x 4-byte (256-byte) DMA FIFO
- Four sets of DMA control registers. Other sets can be programmed while one performs a transfer.
- Chained transfers—when one transfer completes, another programmed transfer automatically begins
- Scatter/gather via link list of records. First set of records in registers, subsequent sets of records (control structures) are automatically fetched by hardware from memory.
- Supports bidirectional, unaligned transfers
- Optional hardware handshake signals (REQ#, ACK#, EOT#) if certain chip selects are not used

Serial Port (UART)

- Compatible with National Semiconductor's PC16550D UART
- Receiver and transmitter each have a 16-byte FIFO
- 5, 6, 7, or 8 bits per character
- Even, odd, or no parity-bit generation and detection
- 1, 1.5, or 2 stop-bit generation
- Baud-rate generator division of input clock by 1 to (2^{16}-1)
- Prioritized interrupt controls
- DSR and DTR control signals
- Optional hardware controls (CTS#, RTS#, DCD#, XIN#) if certain chip selects are not used

Timers

- 16-bit SDRAM refresh timer
- 24-bit CPU bus read timer
- 32-bit general-purpose timer
- 32-bit watchdog timer
- All timers are cascadable

Contact List

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QuickPrint® 1910 Coprocessor

High-Performance Integrated Embedded Imaging Coprocessor for Monochrome

QuickPrint ®

CPUs Supported

NEC VR Series processors

Product Overview

The QuickPrint®1910 is a scaleable coprocessor designed to provide unparalleled performance for a variety of embedded controllers for high-speed monochrome printers and multi-function devices. As part of Peerless' QuickPrint 1900 family of coprocessors, QP1910 is also cost effective for desktop monochrome systems.

Processor Support: A broad range of target applications is supported with direct interfaces to a variety of families of processors, including the NEC VR Series, and IBM PowerPC™ series.

Seventh-Generation Technology: The QuickPrint 1900 family is the seventh generation of the embedded Peerless coprocessor family. It provides a superset of the QuickPrint 1800 features and integrates key controller functions with graphics acceleration to support a wide range of devices.

Cost Reduction: The QuickPrint 1910 coprocessor reduces costs by integrating the required features of a high-performance printer controller into a single device.

Integrated components include Peerless' Graphics Execution Unit, Print Engine Video Controller (PVC), controllers for ROM, SDRAM, and I/O, a serial communications channel, and an IEEE-1284 parallel port with dedicated forward and reverse DMA channels.

Performance: QP1910 provides cost-effective monochrome printing up to 120 ppm at 600 dpi. Higher resolutions are supported at reduced performance.

Salient Features

◗ Peerless' seventh-generation graphics coprocessor for embedded imaging

◗ Designed for high-speed monochrome systems

◗ Single device with flexible support for a variety of engine types

◗ Multiple embedded processor support: MIPS™ and PowerPC™

◗ Monochrome throughput: Up to 120 ppm @ 600 dpi

PEERLESS
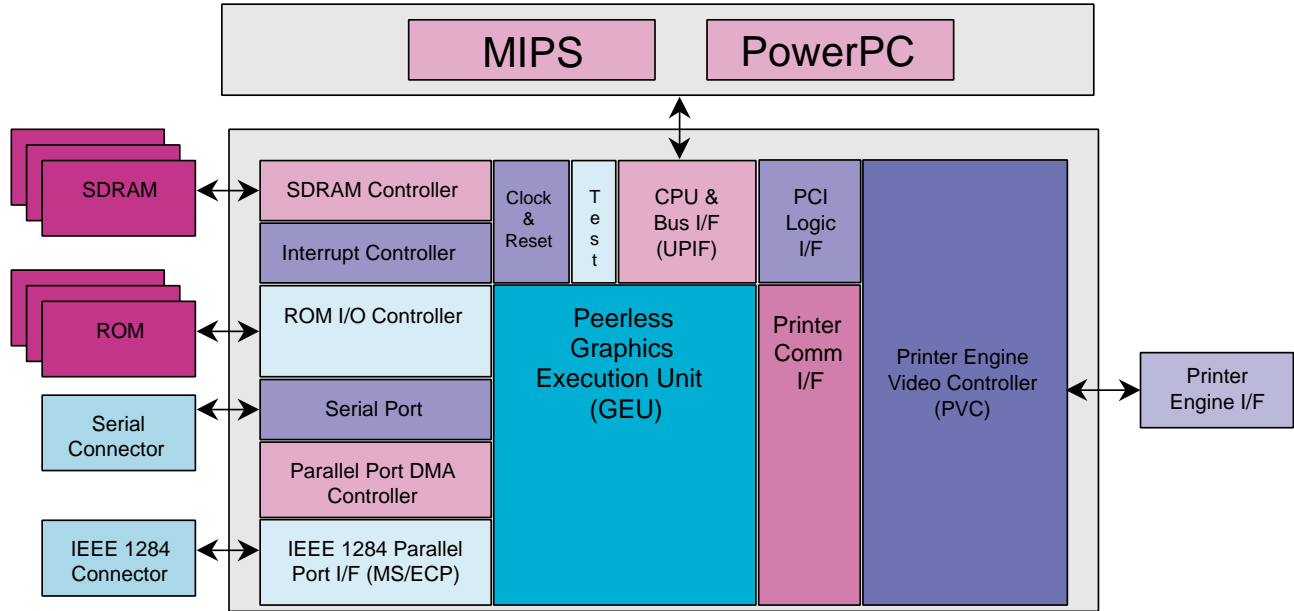
The high bandwidth QuickPrint video generation rate, high-throughput GEU, and dual bus architecture contribute to the high performance of the QuickPrint series. The clock rate allows use of high-speed processors, and the integrated rotation assist provides a further performance boost for complex graphics. The dual bus architecture enables parallel CPU, GEU, and PVC execution.

Extensibility: QP1910 provides a scalable solution for any OEM's needs as well as providing interfaces to PCI logic.

Peerless Memory Reduction Technology: Peerless' patented Memory Reduction Technology (MRT™) is supported by the seventh-generation Peerless Graphics Execution Unit (GEU). The GEU provides patented lossy and lossless compression and decompression, in addition to a compact display list page representation. MRT™ enables All-Pages-Print in very low memory configurations.

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Memory Reduction Technology (MRT) and QuickPrint are registered trademarks of Peerless Systems Corp.

QuickPrint® 1940 Coprocessor

High-Performance Integrated Embedded Imaging Coprocessor with Variable Color Depth and Single-Pass Tandem Engine Support

Salient Features

▶ Peerless' seventh-generation graphics coprocessor for embedded imaging

▶ Support for high-speed single-pass color tandem systems and multiple bits per-pixel

▶ Single device with flexible support for a variety of engine types

▶ Scaleable to support high-speed multilaser/LED color systems

▶ Multiple embedded processor support: MIPS™ and PowerPC™

▶ Multi processing support for up to four QP1940 units

▶ Color throughput: Up to 40 ppm @ 600 dpi

CPUs Supported

NEC VR Series processors

Product Overview

The QuickPrint®1940 is a scaleable coprocessor designed to provide unparalleled performance for a variety of embedded controllers for high-speed printers and multifunction devices. It provides support for high-speed single-drum tandem color systems with continuous tone capabilities, as well as multi-laser/LED color systems. As part of Peerless' QuickPrint 1900 family of coprocessors, QP1940 is also cost effective for desktop color systems.

Processor Support: A broad range of target applications is supported with direct interfaces to a variety of families of processors, including the NEC VR Series and IBM PowerPC™.

Seventh-Generation Technology: The QuickPrint 1900 family is the seventh generation of the embedded Peerless coprocessor family. It provides a superset of the QuickPrint 1800 features and integrates key controller functions with graphics acceleration to support a wide range of devices.

Cost Reduction: The QuickPrint 1940 coprocessor reduces costs by integrating the required features of a high-performance printer controller into a single device.

Integrated components include Peerless' Graphics Execution Unit, four independently operating Print Engine Video Controllers (PVCs), controllers for ROM, SDRAM, I/O, a serial communications channel, and an IEEE-1284 parallel port with dedicated forward and reverse DMA channels.

Performance: QP1940 provides cost-effective color printing up to 40 ppm. Higher resolutions and multi-bit per pixel are supported at reduced performance.
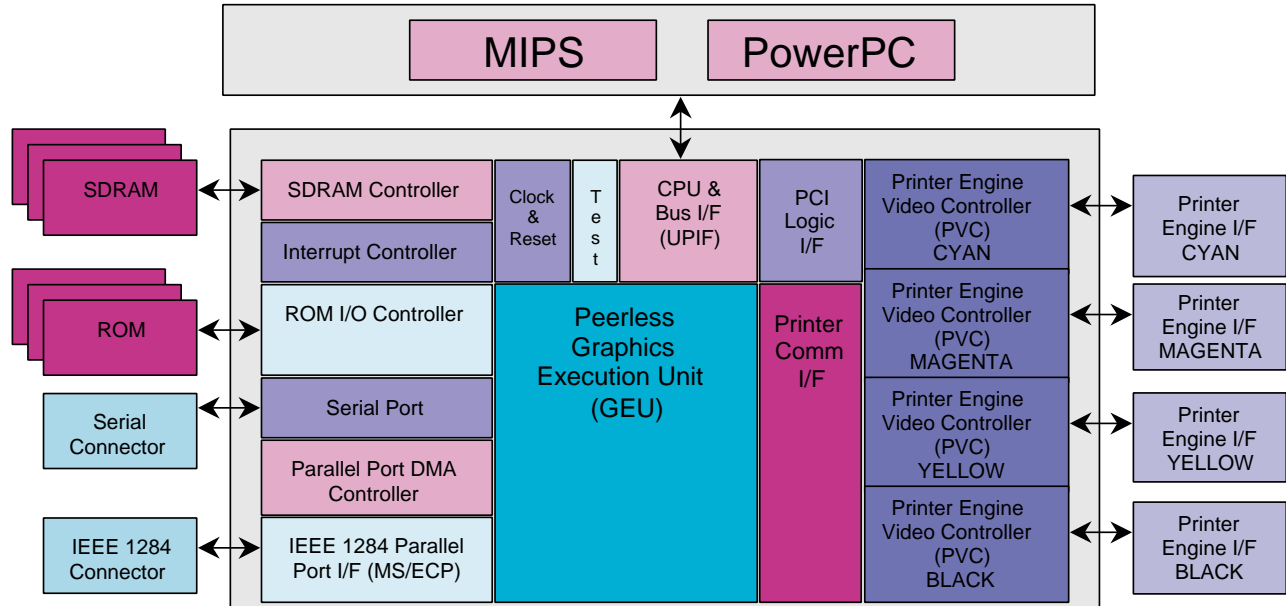
PEERLESS

The high-bandwidth QuickPrint video generation rate, high throughput GEU, and dual bus architecture contribute to the high performance of the QuickPrint series. The clock rate allows use of high-speed processors, and the integrated rotation-assist provides further performance boost for complex graphics. The dual bus architecture enables parallel CPU, GEU, and PVC execution.

Extensibility: QP1940 provides a scaleable solution for any OEM's needs. OEMs may choose to integrate up to four units of QP1940 with dedicated independent RAM channels for effective 128-bit data processing bandwidth for variable color output.

QP1940 also provides interfaces to PCI logic, as well as external compression/decompression ASICs for highly complex multiple-bit-per-pixel graphics processing.

Peerless Memory Reduction Technology®: Peerless' patented Memory Reduction Technology (MRT) is supported by the seventh-generation Peerless Graphics Execution Unit (GEU). The GEU provides patented lossy and lossless compression and decompression, in addition to a compact display list page representation. MRT enables All-Pages-Print in very low memory configurations.

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Memory Reduction Technology (MRT) and QuickPrint are registered trademarks of Peerless Systems Corp.

V320USC

High-Integration, Low-Cost PCI System Controller for 32-Bit MIPS Processors

Salient Features

◗ Simple interface to VR5432 and VR4310 processors

◗ Fully compliant with PCI 2.2 specification

◗ Configurable for PCI primary master, PCI master agent, or PCI target device operation

◗ Up to 75 MHz local bus clock with separate asynchronous PCI clock up to 50 MHz

◗ 640 bytes of on-chip FIFO using V3's unique Dynamic Bandwidth Allocation™ architecture

◗ On-the-fly byte order (endian) conversion, including automatic byte swapping

◗ Up to 1 KB of continuous burst access to (E)SDRAM from the PCI bus

◗ Two independent advanced DMA engines

◗ PCI Bus Power Management Interface Specification 1.0

◗ I$_2$O Ready ATU and messaging unit

◗ Hot Swap Ready implemented according to PICMG™ Hot Swap specification

◗ Up to 5 programmable chip selects/peripheral device strobe generation

◗ Initialization through local processor, PCI, or serial EEPROM

◗ PC plug and play compatible

◗ Integrated SDRAM controller
  • Support for up to 1 GB of (E)SDRAM
  • Supports 2 Mbit - 256 Mbit SDRAM devices in various organizations
  • Support for up to 4 banks of 168-pin SDRAM DIMM

◗ Two 32-bit general-purpose timers

◗ Watchdog, heartbeat, and bus watch timers

◗ 3.3 V operation with 5 V-tolerant I/O

◗ Industrial temperature range (-40°C to +85°C)

◗ 208-pin PQFP package

CPUs Supported

NEC VR43xx, VR5432

Product Overview

The V320USC is a third-generation PCI product that integrates many of the functions needed in typical embedded systems. Its high level of integration results in a very high-performance, low-cost system solution for some of the most popular 32-/64-bit processors available.

Three-Way Architecture

A three-bus architecture is employed by the V320USC so that the processor, PCI bus, and memory system can all operate independently. As a result, the USC is really three bridges in one package. With three concurrent buses, system performance is increased and deadlock conditions eliminated.

SEMICONDUCTOR
THE EMBEDDED INTELLIGENCE COMPANY

V320USC Block Diagram
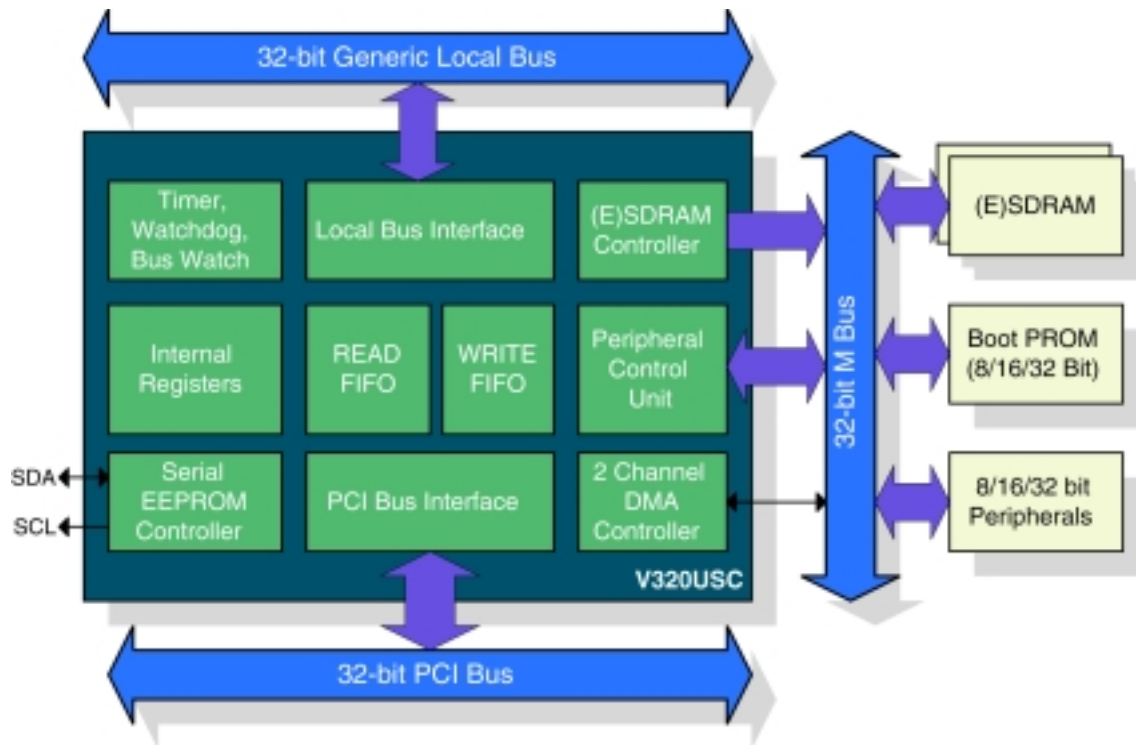
PCI Controller and More

The PCI bus is an important standard used in today's embedded systems. While the V320USC addresses this important requirement, it is far more than a PCI interface. It also controls the most essential components of an embedded system such as SDRAM memory, flash memory, and peripherals using a very flexible memory controller and peripheral control unit.

Direct Processor Interface

A VR5432 processor will connect directly to the V320USC. The interfaces are designed to provide low latency of access by employing large on-chip buffers that utilize the Dynamic Bandwidth Allocation™ feature. This feature allows the on-chip buffers to be more fully utilized.

Industrial-Strength PCI

CompactPCI applications will benefit from the Hot Swap features implemented by the V320USC according to the PICMG™ specification. The V320USC is a "Hot Swap Ready" silicon device as defined by the specification. For this, the V320USC employs custom-designed PCI buffers that

provide the necessary bias voltage. This eliminates the need for more than 40 external components that would be required by other solutions. Other PICMG requirements for Hot Swap, such as the ejector input, extended Configuration registers (HS_CSR and ECP), blue LED, and ENUM# output, are provided. V3 has established itself as a leader in industrial applications, with all components in the product line, including the V320USC, available as industrial temperature devices.

Mastering the PCI Bus

Throughput in real-world applications is what counts and that is exactly what the V320USC was designed to do. To achieve this, sustained bursting is the key. The PCI bus master interface on the V320USC guarantees the highest possible overall bus utilization by employing large on-chip buffers and never inserting wait states. The large on-chip memory (640 bytes total) ensures long bursts so that the overhead of starting a cycle is amortized over more data. When the USC can no longer handle more data, it will end the transfer rather than insert IRDY wait states, so that other masters can utilize the bus.

PCI Target Applications

The V320USC provides five independent slave interfaces: one internal register access, two SDRAM memory apertures (one of which also acts as an I2O ATU), a peripheral aperture, and a ROM aperture. Except for the internal register aperture, all other slave apertures are directed through FIFO buffers that are designed to maximize bus utilization. When a PCI master accesses the V320USC as a target, it either returns a target ready one cycle after FRAME or it issues a retry. A retry will be issued if the write FIFO is full (writes) or there is no prefetched read data (reads). This allows other PCI transactions to proceed and keep the bus occupied. When the V320USC is ready to deliver data, it will assert TRDY and keep it asserted as long as data can move. When data cannot move, the USC will terminate the transfer with the last data rather than insert target wait states.

Dual DMA Engine with Descriptor Processing

Two fully independent DMA engines provide one of the fastest methods of moving data in the system. Each engine is capable of processing descriptors in either PCI space or local memory. The unique Pooled Buffer™ architecture of the V320USC guarantees high bus utilization and long sustained bursts. Two FIFO buffers (128 bytes total) are dedicated to the DMA engines. The buffers can be dynamically allocated to the DMA engines on a priority basis. When a single or high-priority DMA engine is activated, then both buffers can be allocated to it to allow longer bursts. Burst length, however, is not limited to total buffer size, since simultaneous fill and drain can easily be achieved. When both DMA engines are activated together, they can be prioritized to allow fair and equal access to the buffers via either first-come first-served or fixed priority.

Tuning for Performance

The Dynamic Bandwidth Allocation architecture allows the application developer to fine-tune the 640 bytes of on-chip buffers to achieve the best overall system performance for a specific application. It also allows data to be packed into the on-chip buffers for higher utilization. For example, when the local processor writes data to the PCI, multiple sequential or nonsequential bursts or single cycles can be queued into the posting FIFO. Furthermore, sequential bursts or single cycles from the processor can be automatically combined into larger bursts on the PCI bus. Some examples of tunable features within the V320USC are:

- The write posting drain strategy can be programmed to determine how aggressively the local processor-to-PCI writes will be drained. Simultaneous filling and draining allows long bursts to be sustained—even longer than the write posting buffer size.
- Prefetched read data can be stored in either a single buffer or two buffers (64 bytes total) managed as a least recently used cache. With dual buffers, two sequential streams of data can be prefetched continuously without scrapping data.
- Thresholds for the prefetch buffers are programmable to determine how aggressively they will be filled.

Messaging Unit

- 32-byte bidirectional mailbox with interrupts
- Queue-based I2O messaging unit (which can also be used as a general-purpose messaging unit)

Dual-Ported SDRAM Interface

Memory is at the heart of most embedded systems and is a key factor in determining overall system performance. V3 Semiconductor was the first company to provide single-chip DRAM control solutions fine-tuned to the requirements of embedded RISC processors. The V320USC builds on that experience by tightly integrating SDRAM control functions into the PCI and processor interfaces. The result is a very low-latency memory system that actually behaves like two memory controllers: one optimized for PCI access and another optimized for the local processor.

The SDRAM controller uses a toggle burst order the same as the processor. However, for PCI access, linear bursts are used to provide the greatest PCI compatibility.

Peripheral Control Unit

A peripheral control unit (PCU) provides a simple way to interface 8-/16- or 32-bit peripherals to either a PCI bus or the local processor. A total of five chip-select strobes can be generated, each with separately controlled read/write timing characteristics and data width.

Integrated Peripherals

As a system controller, the V320USC provides additional peripheral functions that are required in a typical embedded system.

- Two 32-bit general-purpose timers can be individually configured as a pulse width modulator, rate generator, pulse counter, or hardware-/software-triggered pulse generator
- Watchdog timer for graceful recovery from catastrophic program failures
- Heartbeat interrupt timer for RTOS interrupt generation
- Bus watch timer to prevent system hangs during accesses to undecoded regions
- 4-channel interrupt controller to generate either PCI or local CPU interrupts and interrupt cross-routing

Ordering Information

Part Number: V320USC-75LPB1

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V340HPC

High Integration, Low-Cost PCI System Controller for 32-Bit MIPS Processors

Salient Features

◗ Direct interface to VR5000 MIPS processor

◗ 100 MHz local bus with support for external cache

◗ High-performance SDRAM controller with multichannel prefetch buffers

◗ Internal SRAM scratchpad for immediate access from the local processor

◗ Software- or hardware-controlled prefetching of PCI data

◗ Fully compliant with PCI 2.2 specification, including support for power management and 64-bit, 66 MHz operation

◗ Configurable to operate as system host or peripheral add-in application

◗ Configurable for single 64-bit PCI bus or dual 32-bit PCI buses

◗ Large bridging FIFOs

◗ Up to 2 KB burst access on both local and PCI interfaces

◗ On-the-fly byte order (endian) conversion

◗ Support for up to 2 GB of SDRAM with optional ECC protection

◗ Registered DIMM support

◗ Multiple DMA engines with chaining and multiprocessor support

◗ Flyby DMA support

◗ Programmable chip select/peripheral device strobe generation

◗ Hot Swap Ready implemented according to PICMGTM Hot Swap Specification

◗ Hardware support for I2O

◗ 8-bit watchdog timer

◗ 3.3V operation with 5V-tolerant input

◗ UART serial interface

◗ 456-pin BGA package

CPUs Supported

NEC VR5000

Product Overview

The V340HPC is the next generation of PCI controller: a full 64-bit-wide system controller for high-end embedded applications. Designed specifically for applications with performance levels unattainable by existing 32-bit solutions, the V340HPC's superior level of integration results in a powerful system solution for 64-bit MIPS processors.

Three-Way Architecture

The V340HPC can provide simultaneous connectivity to multiple PCI buses, high-performance MIPS processors, and commodity synchronous DRAM without the use of any external components. A three-bus architecture is used so that the MIPS processor, PCI bus, and memory system can all operate independently. Using three concurrent buses increases system performance and eliminates deadlock conditions.

V340HPC Block Diagram - Dual
32-bit PCI Buses
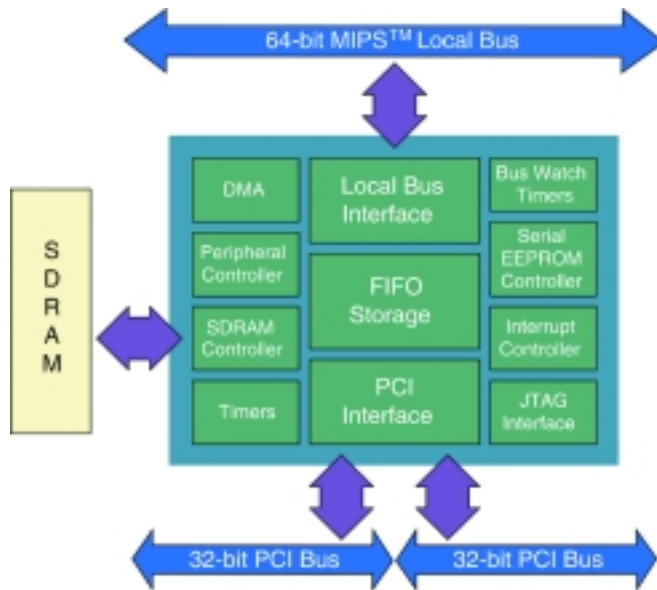
V340HPC Block Diagram - Single
64- or 32-bit PCI Buses
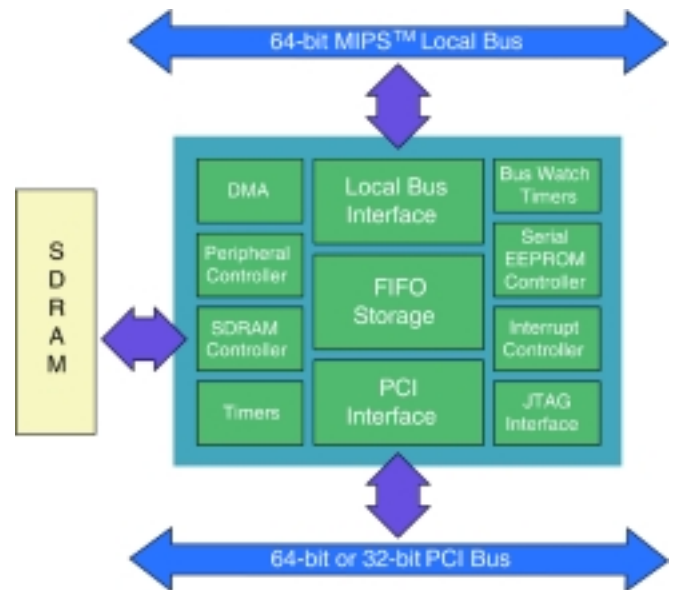
PCI Controller and More

The V340HPC offers designers the flexibility and power to
choose between a single 64-bit, 66 MHz PCI bus or dual 32-
bit, 66 MHz PCI buses. There is an internal, embedded PCI-
to-PCI bridge available when operating in dual PCI bus mode.
The V340HPC also includes interrupt management, a serial
port, I/O control logic, timers, multiple high-performance
DMA controllers, and I/O ports. All these features allow
system designers to build powerful, low-component systems
tailored to their embedded applications.

Processor Support

The V340HPC supports the MIPS 5000 series interface,
including an external cache for high-performance
applications. It supports the VR5000 processor directly. The
interfaces are designed to provide low latency of access by
employing large on-chip buffers that utilize the Dynamic
Bandwidth Allocation™ feature. This feature allows the on-
chip buffers to be more fully utilized.

Industrial-Strength PCI

CompactPCI applications will benefit from the Hot Swap
features implemented by the V340HPC according to the
PICMG™ specification. The V340HPC is a "Hot Swap
Ready" silicon device as defined by the specification. For this,
the V340HPC employs custom-designed PCI buffers that

provide the necessary bias voltage. This eliminates the need
for more than 40 external components that would be required
by other solutions. Other PICMG requirements for Hot Swap,
such as the ejector input, extended Configuration registers
(HS_CSR and ECP), blue LED, and ENUM# output, are
provided. V3 has been a leader in industrial applications, with
all components in the product line, including the V340HPC,
available as industrial temperature devices.

Additional Features

Fully independent DMA engines produce one of the fastest
methods of moving data in the system. Integrated flyby DMA
control logic allows further reduction in latencies. The
peripheral control unit furnishes a simple way to interface 8-,
16-, 32-, or 64-bit peripherals to either the PCI bus or the local
processor. A total of eight chip selects can be generated, each
with separately controlled read/write timing characteristics
and data width. The SDRAM controller's optional
multichannel prefetch buffers reduce effective read latency.
As a system controller, the V340HPC delivers additional
peripheral functions typically required in an embedded
system: general-purpose timers, a watchdog timer, a heartbeat
interrupt timer, a bus watch timer, a 4-channel interrupt
controller, and two 16550-compatible UART channels.

Ordering Information

Part Number: V340HPC-100LPA0

Contact List

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Internet: http://www.vcubed.com

Compilers/Debuggers/Linkers

Nucleus EDE Embedded Development Environment

Product Overview

Built on the firm foundation laid by Microsoft's Developer Studio™, we have constructed an Embedded Development Environment (EDE), Nucleus EDE. We began with the concept that Developer Studio™ is one of the most complete IDEs available, so we extended its capabilities to compile, link, and debug embedded applications using cross-development tools. The result is an environment that is easy to support, uses the latest technology, and is adaptable to any cross-development tool.

In addition to the edit, build, and debug features of Microsoft Developer Studio, it offers project management, a class manager, and browser features. Also, you can add other tools, such as a code management system or any tool that supports code development within Microsoft Developer Studio.

One of the greatest benefits of Microsoft Developer Studio is the ability to build and have any errors appear in a window so users can vector to any file that may need to be edited. We provide tools with Nucleus EDE so that you can use those same facilities for cross compilers. You build your system using cross-development tools; and, if any errors occur, they appear in the error window. Double-click on the error, and you are immediately placed in the edit window at the line where the error occurred. After editing and repairing it, you can rebuild your system. Also, Developer Studio will ensure that the edited file has been properly saved before the build starts.

Nucleus EDE is shipped preconfigured with an initialization file that is read into our configuration program. This file contains the common directories and paths for the tool set that you are using. Also, it contains Wizards to support the compiler, assembler, librarian, linker, and locator command lines and switches that we use when building the target Nucleus application.

Salient Features

◗ Embedded development environment

◗ Based on Microsoft's Developer Studio™

◗ Make files to build a system using any commercial development tools

◗ Errors appear in window for quick editing

◗ Preconfigured with initialization file when shipped

◗ Easy access to cross debuggers

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Accelerated Technology
INCORPORATED

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Nucleus
REAL-TIME SOFTWARE
By Accelerated Technology, Inc.

Nucleus MNT Windows NT-Based Prototyping Environment

Salient Features

◗ Executes as a native Windows NT or Windows 95 application

◗ Designed and developed with Microsoft's Visual C++ tool set

◗ PC hosted development and run-time environments

◗ Prototypes most C code that will be used in target system

◗ Provided with a prebuilt project file

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Product Overview

Nucleus MNT utilizes three modules ported to the Windows NT (or Windows 95) threads environment to perform initialization, scheduling, and timer management functions. The initialization module sets up interrupt vectors for the timer and the terminal interface. The scheduling module employs the Windows thread model to manage the switching of tasks, while the timer module processes a timer tick to facilitate the Nucleus PLUS task sleep, time-slicing, time-out, and timer-thread capabilities.

Development and Debugging

Nucleus MNT was designed and developed to work with Microsoft's Visual C++ tool set. The complete Visual C++ integrated development environment is available, including the editor, make/project capabilities, compiler, librarian, assembler, linker, and debugger.

By using the project file supplied with Nucleus MNT, you can be up and running almost immediately. The release files shipped with Nucleus MNT are loaded into a directory. You add the project to your Visual C++ environment and the "Build" menu selection is invoked to produce a Windows NT console application. The Executable contains a demonstration program that exercises almost all Nucleus PLUS capabilities. You can modify this program or replace it with tasks you create when you begin development of your project.

Because Nucleus MNT and the programs developed with it are true Windows NT applications, they can be debugged using the standard Visual C++ debugger. Other debugging aids supplied with Visual C++ (e.g., Spy) also can be used in the debugging process.

Accelerated Technology
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Contact: Mitsurou Nakajyo

Nucleus DBUG+ Multitasking Debugger for Nucleus PLUS

Host Platforms

PC

Product Overview

Nucleus DBUG+ was developed to assist users of Nucleus PLUS in debugging their multitasking applications. It installs as a task in any Nucleus PLUS system and provides a number of features not normally available within traditional debugging environments.

Because Nucleus DBUG+ is installed as a task, it can freely interact with the rest of the tasking environment. Additionally, tasking information can be viewed in both overview and detailed form. All user interaction with Nucleus DBUG+ is performed through a command-line prompt.

The user invokes Nucleus DBUG+ by either entering a status command or invoking Nucleus PLUS services by entering the C interface calls. Status commands have optional parameters which can indicate the specifics associated with the status (e.g., ts 1 - displays status of task number 1). C interface calls are entered and the user is prompted for the appropriate parameters.

As well as being delivered with complete source code and without royalties, Nucleus is provided with six months of free technical support. This includes phone, fax, Email, and new releases. For more information, contact Accelerated Technology.

Salient Features

‣ Displays task information

‣ Displays queue information

‣ Displays resource information

‣ Displays event group information

‣ Displays memory partition information

‣ Modify/display memory capability

‣ Invoke all Nucleus PLUS services from command line

‣ Documented source code provided

‣ Integrated with popular source debuggers

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Accelerated Technology
I N C O R P O R A T E D

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Contact: Mitsurou Nakajyo

Nucleus UDB Portable Source-Level Debugger

Salient Features

- Automatic tracing feature

- Kernel-aware debugging

- Configurable display windows for source, memory, variables, registers, etc.

- Intuitive button bar interface facilitates quick learning

- Complex breakpoints

- Console window capture-to-file capability

- Universal file viewer

- Stopwatch for timing functionality

- Improved source file tracking

- Advanced dynamic data exchange

- Advanced DLL interface

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Product Overview

The price/performance ratios among microprocessors are constantly changing. Processors appropriate for today's products may not be suitable for tomorrow's applications. For the embedded systems developer, this often means adjusting to a new set of development tools. To relieve some of that burden and speed development time, Nucleus UDB offers a consistent interface across various processor platforms. This enables developers to quickly adapt to new challenges and meet the demands of changing applications.

Nucleus UDB was designed from the ground up to take advantage of the facilities contained within the Windows operating system. Nucleus UDB offers an intuitive button-driven interface, as well as an event-driven sequencer system. In addition, UDB provides both task-specific and general breakpoint capabilities to help accelerate embedded system development. Combined, these features offer faster performance as well as the ability to run other applications while a debugging session is active.

Source-Level Debugging

Nucleus UDB is a powerful, GUI-based source-level debugger for embedded applications. Its three component configurations include the debugger front end, host communications module, and target monitor, which make for a powerful and portable debugging environment. Since the front end is standard across all target CPU platforms, developers need to learn only one debugging environment.

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INCORPORATED

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Nucleus FILE Full-Featured File System

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Product Overview

The need for mass storage takes many forms, including collecting data for later analysis and continued operation of the system. In both cases, it is helpful to be able to address the data outside the embedded environment. To support these requirements, Accelerated Technology provides Nucleus FILE.

Nucleus FILE is a robust, well-integrated tool for managing MS-DOS-compatible file formats which require that a driver only needs to be fully functional on the target system. Accelerated Technology supports drivers for a number of industry-standard devices. This support increases as new device drivers continue to be developed. In addition to supporting various device drivers, a RAM disk driver also is available. A limited version of this driver is provided in object form for testing on your target systems, which allows you to quickly see Nucleus FILE in operation after building and downloading.

Essential Capabilities

Nucleus FILE is written entirely in C and provides all necessary functions to manage MS-DOS-compatible disks. This includes the boot block, file allocation table (FAT), directory, file, and device driver management. Other than standard MS-DOS capabilities, Nucleus FILE allows multiple tasks to access the file system simultaneously by requiring all tasks to register as users of the file system.

Accelerated Technology provides demonstration programs that exercise the primary functions of the file system. With the demonstration program and a complete set of documentation, building a system with MS-DOS-compatible offline storage facilities is simple and straightforward.

Standard device drivers are available for floppy disks, IDE hard drives, and SCSI devices. PCMCIA support also is available for ATA-compatible drives.

Salient Features

◗ Support for FAT32, including long file names

◗ No royalties

◗ C source code provided

◗ Reentrant file access

◗ ROMable

◗ MS-DOS 4.0 and higher compatible

◗ Supports multiple floppy formats and fixed disks

◗ File system format facilities provided

◗ RAM disk available

◗ Transparent to CPU byte ordering

◗ Simple device driver interface

◗ Two entry points for date/time management

◗ Integrated with Nucleus PLUS

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Nucleus GRAFIX Portable Graphical User Interface

Salient Features

◗ First portable graphical user interface (GUI)

◗ Scalable development across multiple CPUs

◗ Full use of Windows features

◗ Pull-down menus, dialog boxes, radio buttons, scroll windows, icons, file views, and more

◗ Understands PCX and BMP file formats

◗ Other capabilities being developed for GIF, JPEG, and TIFF formats

◗ Accessible with AppStudio™

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Product Overview

In designing Nucleus GRAFIX, our goal was to create a GUI with the features that everyone needs. Other than portability, Nucleus GRAFIX includes pull-down menus, dialog boxes, radio buttons, scroll windows, icons, file views, and much more. Not only are these features powerful, but they're also exceptionally fast. That's why we have designed our software especially to combine multitasking technology with a detailed understanding of graphics hardware and how its capability can be harnessed.

Nucleus GRAFIX is highly portable due to its intelligently engineered and layered modules. We can take advantage of the varying capabilities of graphics devices so the processor can be relieved of computer-intensive tasks whenever possible. Nucleus GRAFIX is proven, its design is sound, and it provides all of the features you would expect from a full-featured windowing package.

By combining the portability of Nucleus GRAFIX with the capabilities of Nucleus EDE, you can develop your GUI using the best tools available.

Nucleus EDE gives you an integrated environment and access to AppStudio™ where you can design your GUI. It will produce an "RC" script that contains all the components you need to build a GUI for your target. The "RC" file is read and converted to a C source file that can be compiled and linked with your Nucleus GRAFIX application and executed on your target.

Nucleus GRAFIX supplies a full set of features for associating input to windows. When the mouse is clicked or dragged, or a key is pressed, the action is associated with a window so that your application is informed.

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SDE-MIPS Embedded Toolkit for 32- and 64-Bit MIPS Microprocessors

About SDE-MIPS

SDE-MIPS is a software developer's toolkit for any MIPS RISC target hosted on Windows 95, Windows NT, Sun SPARC, Linux/x86, and other standard platforms. SDE-MIPS v3 supports the latest instruction set additions—MIPS16, MIPS V, and MDMX, as well as MIPS I-IV, and features a "windowed" debugger.

The Free Software Foundation's GNU C (gcc) is probably the best multitarget compiler anyone ever made. All GNU source is free, but most of our customers buy the complete package for support and a wealth of useful software. SDE-MIPS is:

- Comprehensive: all the software you need to use C and C++, even on a "bare" target. Source-level "visual" debug, libc/libm, timing, profiling, soft floating-point, and FP emulation are all there. Ready-to-build sources for favorite evaluation boards include a simple ROM.

- A toolkit from a MIPS specialist: adds vital MIPS folklore, as well as bug fixes and enhancements to the whole toolchain—you get the best MIPS compiler going.

- Fast, compact code generation: on level terms with the respected, but UNIX-targeted, SGI/MIPS compiler; much faster than some other "embedded" products on the market.

- 64-bit and MIPS IV support: use 64-bit power, today. Our model (first offered by SDE-MIPS) gives you access to 64-bit speed without requiring you to re write your whole system.

- Affordable: £1450/$2500 for a single-seat license including 12 months support and upgrades, with substantial per-seat discounts for larger sites. No-quibble money-back guarantee.

- Reliable and easy to port to: gcc is refreshingly free from bugs and surprises - ask any established user. gcc is usually ANSI compliant in a relaxed way, but options are available from extreme paranoia to a laid-back mode suitable for the dustiest old sources. If your porting problem is really bad we'll even do you a special version to fit.

- Up to date: library functions to ANSI and POSIX standards. The default object format is SGI-compatible ELF/DWARF, with ECOFF interlinking.

Salient Features

- GNU C developed and supported by Algorithmics

- Largest range of host platforms

- Comprehensive run-time system kit

- Complete tool set includes debugger, profiler, etc.

- Wide range of targets supported by the kit

- All MIPS CPU variants in one compiler binary

- 64-bit and MIPS IV extensions

- Software examples build "out of the box" on many common targets

- E-mail support from expert compiler developers

CPUs Supported

All NEC VR Series microprocessors

Host Platforms

Windows 95, Windows NT, Sun SPARC, Linux/x86, and other standard platforms

SDE-MIPS v3 Features

- All current NEC VR Series CPU types supported: including VR41xx, VR43xx, VR5xxx, big or little endian. Support to MIPS IV; exploits floating-point and integer multiply-add instructions where available.

- 64-bit extensions: 64-bit MIPS CPUs have full 64-bit data paths (32-bit compatible, though). But 64-bit addresses are usually undesirable for non-UNIX applications. SDE-MIPS only generates 64-bit instructions for "long long" arithmetic/logic; accelerate your software without changing the world. Library routines and sample code quietly handle 64-bit register saves when required.

- Language standards: gcc provides rich and up-to-date language standard options; command-line options enable strictly-checked ANSI; old-fashioned K&R; and many useful points in between.

- Assembler: the assembler accepts all sources for existing (MIPS and USL) standards. It normally hides the pipeline, but can just warn you about any instruction sequence which may violate pipeline requirements.

- MIPS arcana: we support gp-relative addressing, the incomprehensibly complex varargs-compatible parameter passing, and all that stuff; not everybody does.

- Object code: uses ELF/stabs format. If you use ECOFF libraries or must produce ECOFF output, the linker will do it.

- Debugger: the gdb debugger provides symbolic, source-level debug of programs on the target machine in conjunction with a simple target monitor. Connect your target via serial port or Ethernet. There's a target machine "monitor" you can link with your program, but SDE-MIPS also works with the PMON PROM monitor.

- Debug/edit environment: we recommend UNIX-hosted programmers to use GNU Emacs functions to run the debugger from an editor window. Emacs' inexhaustible array of features makes this really productive.

- Profiling: The gprof profiler uses information collected by the SDE-MIPS run-time system during the actual execution of your program.

- Libraries: the package includes full POSIX- and ANSI-compliant "C" and "maths" libraries, with no license restrictions. The C library is reentrant and thread-safe.

- Floating-point support: the compiler will generate MIPS FPA instructions or calls to Emulation subroutines at choice. We include an IEEE-754-compliant FPA instruction emulator (essential to fix up FP calculations even when the MIPS CPU includes FP hardware).

- Embedded system kit: a collection of sources and library functions (including power-on initialization and cache/TLB functions); you need only write target-specific initialization and UART "putc/getc" functions to get simple programs up and running on a new target.

- Example programs: we provide a selection of complete example programs, from "hello world" to complex exception handlers. Each will build straight out of the box into a running program on any supported target.

- C++: now fully supported. C++ class libraries are subject to the GNU library license.

Other Software from Algorithmics

- PMON monitor: this excellent, freely reusable, PROM package runs on a variety of eval boards. Sources are available on our Internet node, and we can help you get it ported to your hardware.

- AlgPOST generic power-on test suite: if you need power-on tests on your hardware, AlgPOST can save you a lot of time and trouble. Ask Algorithmics about license terms.

Support

- Support by experts: by Internet e-mail to "sde@algor.co.uk", or fax. Your query will be handled by experienced, working MIPS programmers. We'll let you ask existing customers how they feel about us. Intensive service is an extra-cost option for big projects or busy sites.

If It's GNU Why Isn't It Free?

You're paying for support, installation, Algorithmics' own assembler and, most importantly, vital run-time code. All GNU-derived sources including our fixes and improvements are freely available.

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C/C++ Compiler Package for MIPS Embedded Systems

Salient Features

◗ Highly optimizing C/C++ cross-compiler hosted on popular development platforms and targeted at a wide range of MIPS embedded processors

◗ The C compilation mode supports ANSI/ISO standard C and "K&R" C, and also includes a mixed mode that accepts and highlights non-standard uses of C

◗ The C++ compilation mode supports ANSI/ISO standard C++, Microsoft's Visual C++, Cfront 2.1 and 3.0, and (by special request) the embedded subset of C++. It also provides a mixed mode that accepts and highlights non-standard uses of C++

◗ The compiler performs many advanced optimizations, including optimizations aimed at hardware features of each supported type of MIPS processor, that aggressively transform compiled programs to increase their run-time speed and minimize their run-time size. Most optimizations are applied locally (on basic blocks of code), globally (on entire C and C++ functions), and over all C/C++ functions submitted for compilation ("whole application" optimizations)

◗ The compiler allows a high degree of control over the compilation process. For example, a user can select individual optimizations (and specify the extent and scope of each) by a compiler option or by pragma statements inserted into the source code. A unique option allows the user to choose optimizations specifically aimed at a given type of target processor (NEC's VR5432, for example).

◗ The compiler generates MIPS assembler code that is fully compatible with the GNU-based assembler and, after assembly into binary code, is compatible with the Algorithmics Ltd. linker. Furthermore, the linker-produced binary code is fully compatible with Algorithmics' run-time libraries (libc, libm, etc.). When used in a debugging mode, the compiler produces debugging information that is fully acceptable to Algorithmics' GDB.

◗ The compiler comes with Algorithmics' MIPS-targeted assembler, linker, run-time libraries, and debugger, all integrated into a C/C++ compiler package that can be downloaded from Apogee's FTP server. The package also includes a basic C++ library licensed by Apogee from SCO and (optionally) the ANSI/ISO standard C++ library licensed from Modena Software, which has been performance tuned for use with the compiler. This library includes the full Standard Template Library and all standard-required class libraries.

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Starting in early 2000, MIPS embedded processors compliant with the MIPS32 and MIPS64 architecture definitions from MIPS Technologies

A P●G E E SOFTWARE INC.

The Compiler People

Host Platforms

Windows 95/98/NT, Sun SPARC/Solaris, MIPS/IRIX, PA-RISC/HP-UX

Other host platforms are available on request

Support for the Java™ Platform

Starting in 2Q2000, the C/C++ Compiler Package will be available as one of the major parts of a MIPS-specific version of Apogee JDE, a comprehensive programming environment for developing, performance tuning, and deploying high-performance Java™ and Java/C/C++ embedded system applications.

Apogee JDE includes: a powerful GUI, Java/C/C++ project manager, Java/C/C++ editor, Java and C++ browsers, various compilers (Java to bytecode, Java to native code, and bytecode to native code), bytecode-to-bytecode optimizers (speed and size optimizations), and the bytecode/native code debugger. It comes with Sun Microsystems' EmbeddedJava™ VM, PersonalJava™ VM, and (soon) K Virtual Machine (KVM), ported by Apogee to various types of MIPS embedded processors running VxWorks or (by special request) other popular RTOSs and tuned for high performance when used with JDE tools.

Apogee JDE allows deployment of Java and Java/C/C++ applications in optimized bytecode, optimized native code, or in a mixture of optimized bytecode and native code.

Company Profile

Apogee Software specializes in high-performance programming tools for developing, debugging, and performance tuning many types of embedded systems applications (including large and complex applications) written in C/C++, Java/C/C++, or Java.

Apogee tools are hosted on most popular development platforms and targeted at PowerPC, MIPS, SPARC, and (in 2Q2000) x86 embedded processors. Apogee also offers highly optimizing C/C++ and FORTRAN compilers for SPARC/Solaris and PA-RISC/HP-UX platforms.

Apogee provides technical solutions at several levels—from technology and source code licensing to software and hardware vendors to distribution and support of binary forms of various tools to end users and resellers.

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CodeTEST

Embedded Software Verification Tools

Performance Analysis

- Measures function and task execution times
- Counts call-pair linkages to identify thrashing
- Non-sampled measurements of 32,000 functions at one time

Coverage Analysis

- MC/DC, Decision Coverage or Statement Coverage
- Displays coverage at program, function, or source levels
- Plots coverage over time
- Completely interactive measurements simplify test creation and refinement

Memory Allocation Analysis

- Dynamic display shows memory leaks in progress before the system crashes
- Pinpoints memory allocation and free errors to offending source line
- Measures true worst-case allocation

Trace Analysis

- Traces embedded programs at source, control-flow, or high level
- Deep trace captures over 100,000 source lines of execution
- Powerful triggering and trace display options zero in on problems
- Designed for software engineers

CPUs Supported

Call for supported processors

Host Platforms

Sun, Windows, HP 9000

Product Overview

The CodeTEST® family of native and in-circuit software verification tools is the first software verification tool suite specifically designed for embedded systems software. CodeTEST tools provide an easy-to-use, cost-effective solution for tracing embedded programs and verifying software performance, test coverage, and memory allocation. Using CodeTEST modules as shared network tools results in higher quality software for a development and testing team.

You can monitor the entire program at once, eliminating the difficulty of deciding which part of the program to watch and how to set up the tool for each measurement. You get reliable trace and measurements, even when programs are executed out of cache or are dynamically relocated.

Performance Analysis

CodeTEST Performance tools monitor thousands of program functions at one time, measuring function and task execution times and intervals. The displays present a sorted list of functions or tasks based upon the cumulative CPU time they have consumed. Tabular data showing true minimum and maximum execution times is also presented. Without guesswork, you can optimize routines that will truly affect system performance.

Applied Microsystems
C O R P O R A T I O N
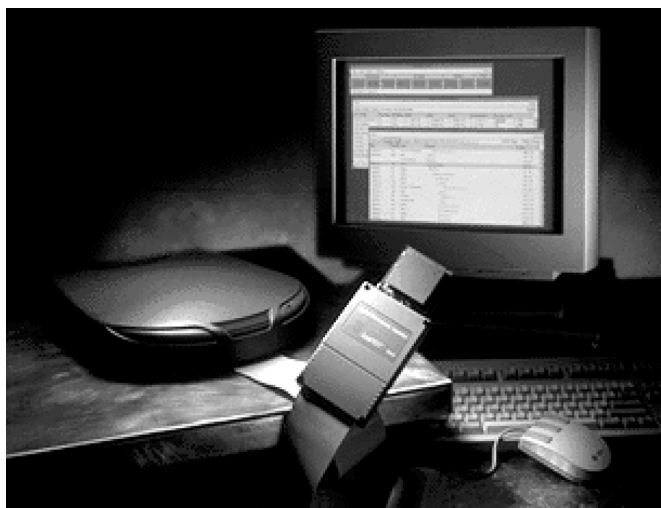
Coverage Testing

CodeTEST Advanced Coverage tools offer several views of program coverage, including a program-wide coverage summary and source-level coverage trends. Because the process is completely interactive, you can track coverage while you exercise your system. You can produce composite reports that merge the results of multiple test runs so as to see the effectiveness of a suite of tests.

Now engineers who are mandated to test software applications to RTCA/DO-178B levels can rely on CodeTEST Advanced Coverage tools for accurate measurement analysis for MC/DC, DC, and SC.

Dynamic Memory Allocation Analysis

Dynamic memory allocation was very difficult to track until CodeTEST tools became available. The allocation display shows how many bytes of memory have been allocated by each function in the program. It's easy to see which functions are consuming the most memory. Users can watch the memory allocation bars dynamically shrink and grow as the program runs.

While the program runs, CodeTEST Memory Analysis pinpoints discrete allocation errors such as corrupt pointers. Users can navigate directly to the source to see the context of each allocation statement.

Trace Display

CodeTEST Trace tools enable you to trace the execution history of your program and set versatile triggering conditions. Trace can be displayed at three levels of detail: "high-level trace," "control flow trace," and "source trace."

High-level trace shows RTOS events and function executions to give you "the big picture" of program flow. Control flow trace adds the dimension of displaying each executed decision statement within the executed function. Source trace adds all executed source statements to the display, revealing the complete execution history.

The CodeTEST Trace display collapses loops, so that instead of countless recurrences of the same statement in the trace, there is one statement with a count displayed. And since each captured statement is time-stamped, you can easily measure loop times, path execution times, etc.

Eliminate Prefetch and Cache Confusion

The CodeTEST approach eliminates all confusion surrounding prefetched instructions and cache-based program execution. The elaborate hardware schemes used by other tools often are not adequate to track software executing out of cache or to differentiate prefetched instructions from those executed. The CodeTEST approach works reliably under these demanding circumstances. In fact, CodeTEST tools can even monitor programs that are dynamically relocated.

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Cygnus GNUPro™ Embedded ToolSuite

ToolChain Components

▶ **gcc**   Highly optimized ANSI-C compiler

▶ **g++**   ANSI-tracking C++ compiler

▶ **gdb**   Source and assembly-level debugger

▶ **gas**   GNU assembler

▶ **ld**   GNU linker

▶ **insight** Graphical user interface for GDB

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Object Formats Supported

ELF

Host Platforms

Windows 95/98/NT, Solaris 2.5.1 or greater

Product Overview

GNUPro™ ETS is a completely integrated, commercial grade tool suite based on the popular GNU standard. The tool suite includes source and pre-built binaries that have been run through Cygnus's suite of over 200,000 unique test cases.

GNUPro ETS contains the latest technology developed by expert Cygnus engineers as well as enhancements and extensions contributed by hundreds of developers worldwide. Developer support is available for large enterprises or small workgroup development teams.

GCC Optimizations

• Full ANSI compliance

• Single source

• K+R mode implementation

• In-line assembly code

• Over 100 switches available, including specific optimizations for code size and for code execution speed such as
  — Loop unrolling
  — Constant folding
  — Tail recursion elimination
  — Dead code elimination
  — Inlining

GDB Features

• Set and disable watchpoints, catchpoints, breakpoints

• Register display

• Stack frame analysis and back trace

CYGNUS

Insight (GDB GUI)

- Local variables window
- Threads window
- Memory window

G++ Features/Optimizations

- ISO standard tracking
- Thread-safe library (selected platforms)
- Exception handling
- Namespace support
- Many template optimizations
- Koenig lookup on operators and functions
- Nested exceptions
- Inheritance protection

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Model CCES-MIPS Software Cross-Development Tools for NEC VR Series Processors

Salient Features

◗ Complete C development toolkit

◗ C/C++ compiler generates high-performance code

◗ Fast, flexible, locating linker handles large files, arbitrarily named sections

◗ Source-level debug for ICE, JTAG emulators, target-resident debug kernel, and instruction set simulator

◗ Fast instruction set simulator

◗ Sample processor initialization and exception handler code

◗ Fast floating-point emulation library

◗ Automatic ROM image building

CPUs Supported

VR41xx, VR43xx, VR5000, VR54xx

Host Platforms

Sun-4: SunOS, Solaris

PC: Windows 95/NT

HP 9000: HP-UX

Product Overview

The CCES-MIPS Software Tool kit offers a complete solution to developers using any NEC VR4xxx or VR5xxx microprocessor. The toolkit consists of tightly integrated programs to generate code and to debug your embedded application.

The toolkit includes an optimizing C/C++ compiler, a macro assembler, a locating linker, a librarian, a C source-level debugger, a symbolic assembly-level debugger, an instruction set simulator, and RSS. RSS is a small, powerful, target-resident debug kernel. In-circuit emulators from EPI are fully compatible with the code generated by this tool kit and with the debuggers provided.

Compiler

The EPI compiler is a globally optimizing C/C++ cross-compiler that supports MIPS 3000, 4000, and 5000 processor variants. The compiler generates quality code tuned to these processors using the most effective optimization techniques available.

Assembler

The EPI assembler is fully compatible with the language requirements of the MIPS assembler, and adds built-in macro and conditional assembly capability.

Linker

The EPI linker handles very large applications quickly while making efficient use of memory. It offers full control over the placement of code and data sections. In addition to handling multiple text and data sections, it will generate ROM images complete with code to copy instructions and initialized data into RAM.

Debugger

EDB is an exceptional source-level debugger for C. You can follow execution in the source window, view formatted data in the value window, and track the nesting of routines in the Call Stack Summary window.

```
                                    wcdbrssw
 File  Edit  Windows  Misc  Brkpts  Exec  Config                              F1=Help
         wcdbrssw - Session                          wcdbrssw - Value Watch
 WCDBICEW> (closing CDBDEMO.rc)           precord         precord = 0
 Reading commands from stdin              message         COMM ERR: serial port timed out on +
                                                          message = "A good message"
 WCDBRSSW>                                string_array[2]  0x80004ee8    "2"

           cdbdemo.c                             wcdbrssw - Target Memory
 .      97:    return((char *) 0);        pc
 .      98: } /* Second */                cdbdemo.c#110:    precord = &a_record;
        99:                               800021b4:  lui    v0,0x8000
       100:                               800021b8:  addiu  v0,v0,20024
       101: /* T H I R D */               800021bc:  sw     v0,-31579(gp)
       102:                               cdbdemo.c#112:    if (select != 0) {
       103: Third(select, random, message) 800021c0:  lw     v1,32(sp)
       104: register long    select;      800021c4:  nop
       105: register int     random;      800021c8:  beq    v1,zero,0x8000228c  # Third+0xec
       106: char    *message;             800021cc:  nop
       107: {                             cdbdemo.c#116:    random = -9;
       108:    static struct RECS *precord; 800021d0:  li    v0,-9
       109:                               800021d4:  sw     v0,28(sp)
 E  → 110:    precord = &a_record;        cdbdemo.c#117:    switch (select % 7) {
       111:                               800021d8:  lw     v1,32(sp)
       112:    if (select != 0) {         800021dc:  li     v0,7
       113:                               800021e0:  div    v1,v0
       114:    int random;                800021e4:  bne    v0,zero,0x800021f0  # Third+0x50
       115:                               800021e8:  nop
       116:    random = -9;               800021ec:  break  0x7
       117:    switch (select % 7) {      800021f0:  mfhi   v0
 .     118:       case 1: printf("1\n");  break;  800021f4:  addiu  v0,v0,-1
 .     119:       case 2: printf("2\n");  break;  800021f8:  sltiu  at,v0,4
 .     120:       case 3: printf("3\n");  break;  800021fc:  beq    at,zero,0x8000225c  # Third+0xbc
 .     121:       case 4: printf("4\n");  break;  80002200:  nop
 [OVER] [INTO] [INSTR] [UP] [GO] [LOAD] [STOP] [SNAP]  80002204:  b    0x80002270          # Third+0xd0
                                          [INSTR] [BYTE] [HALF] [WORD] [ASCII] [SNAP]
      wcdbrssw - Special Registers                     wcdbrssw - Calls
   badv: 00000001                         0 Third(select=1, random=-1, message=0x80004f8c)  +
     sr: 3028a001  (cu=3 bev TS pe CM pz swc isc imsk+  1 Second(aaa=1, bbb=2, ccc=3)       [cdbdemo.c:97]
  cause: 00000024  (bd ce=0 ip=00 sw=0 exccode=bp)     2 First(i=1, j=1, k=1)              [cdbdemo.c:138]
    epc: 800021b4                         3 main(argc=1, argv=0x80005d34)      [cdbdemo.c:79]
   prid: 00000230  (imp=02 rev=30)
```

"Point and click" entry of common commands gives fast, flexible control over the behavior of your application. EDB also accepts a rich set of command-line directives.

EDB displays variables in their declared type. It displays C structures in the same format you might code them yet allows custom formatting.

The debugger is compatible with RSS, the target-resident debug kernel, with the ISS instruction set simulator, with the SYS4K in-circuit emulator, and with the MAJIC EJTAG emulator.

Instruction Set Simulator

ISS is a feature-rich simulator and is highly configurable at run time. Every run of the simulator may be different, and as your requirements change you may enable and disable features as needed for a particular run, thus gaining the benefit of reduced simulation time.

Target-Resident Debug Kernel

RSS is a target-resident kernel that communicates with the EPI debuggers through a serial interface. Easily configured to your target board, it turns your product into a low-cost and highly capable software debug station.

Utilities

The CCES-MIPS software tool kit includes an array of utilities to streamline the task of software development for embedded RISC applications.

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Model ISS-MIPS Instruction Set Simulator

Salient Features

◗ Low-cost, source-level debug environment

◗ High-speed simulation

◗ Cache simulation with breakpoints

◗ TLB simulation

◗ User-selectable simulation features

◗ Supports MIPS ISA I, II, III, IV

CPUs Supported

VR43xx, VR5xxx

Host Platforms

Sun-4: SunOS, Solaris

PC: Windows 95/98/NT

Product Overview

EPI's instruction set simulator, ISS, runs on personal computers as easily as on UNIX workstations, and simulates big- and little-endian targets.

ISS is a feature-rich simulator and is highly configurable at run time. Every run of the simulator may be different, and as your requirements change you may enable and disable features as needed for a particular run, thus gaining the benefit of reduced simulation time.

The ISS memory model includes tag bits for each memory location. These are used to maintain information about which locations have been accessed and how. They are also used for setting breakpoints. Breakpoints may be set on instruction fetch, read, or write cycles, or any combination of the above.

Simulation Advantages

For embedded applications, there are a number of problems that arise for which ISS is ideally suited.

Nested exceptions: Your embedded application must be able to handle nested interrupts and interrupt service routines properly. It is nearly impossible to produce the test conditions needed to evaluate proper interrupt processing in any other environment but simulation. With ISS, you can cause exceptions to occur on demand, allowing you to test all the possibilities.

Stack usage: With ISS, you can monitor system memory usage and see how deep memory allocation stacks actually get at run time, making the most efficient use of often limited resources in your embedded system.

Quality validation: With ISS, it is a simple matter to tag all locations that were executed. After a test run, you can then examine the results and see if you have achieved the desired code coverage. This ensures that all the code has been exercised and prevents untested code from being executed for the first time "in the field."

Performance analysis: ISS lets you tune your application for performance and get immediate feedback as to how many hits and misses occurred in both instruction and data caches. Take advantage of on-chip cache and achieve significant performance improvements by properly tuning how the code is allocated at link time.

Trace: With ISS you can use the built-in trace capability to solve "How did I get here?" problems when debugging embedded system software. Trace data may be collected to a file for post-run analysis, or collected in a buffer for immediate viewing. The trace data is annotated with register contents for all instructions that use register operands as well as symbolic and source information.

Another powerful feature is cache simulation. While some simulators do not even model cache, ISS accurately reflects the behavior of the actual cache systems.

The behavior of on-chip memory management, for those processors that include such facilities, is also modeled. This simulation supports mapping of virtual to physical addresses, and because it also indicates whether a mapped physical address is cached or uncached, the memory model and cache model are tightly integrated.

```
                                    wcdbrssw
 File  Edit  Windows  Misc  Brkpts  Exec  Config                          F1=Help
┌──────── wcdbrssw - Session ────────┐ ┌──────── wcdbrssw - Value Watch ──────────┐
 WCDBICEW> (closing CDBDEMO.rc)         precord        precord = 0
 Reading commands from stdin            message        COMM ERR: serial port timed out on +
                                                       message = "A good message"
 WCDBRSSW>                              string_array[2]  0x80004ee8      "2"

┌──────── cdbdemo.c ─────────────────┐ ┌──────── wcdbrssw - Target Memory ────────┐
 .      97:    return((char *) 0);      pc
 .      98: } /* Second */              cdbdemo.c#110:    precord = &a_record;
        99:                             800021b4:  lui    v0,0x8000
       100:                             800021b8:  addiu  v0,v0,20024
       101: /* T H I R D */             800021bc:  sw     v0,-31579(gp)
       102:                             cdbdemo.c#112:    if (select != 0) {
       103: Third(select, random, message)  800021c0:  lw   v1,32(sp)
       104: register long    select;    800021c4:  nop
       105: register int     random;    800021c8:  beq    v1,zero,0x8000228c  # Third+0xec
       106: char    *message;           800021cc:  nop
       107: {                           cdbdemo.c#116:    random = -9;
       108:     static struct RECS *precord;  800021d0:  li   v0,-9
       109:                             800021d4:  sw     v0,28(sp)
 E →   110:     precord = &a_record;    cdbdemo.c#117:    switch (select % 7) {
       111:                             800021d8:  lw     v1,32(sp)
       112:     if (select != 0) {      800021dc:  li     v0,7
       113:                             800021e0:  div    v1,v0
       114:         int random;         800021e4:  bne    v0,zero,0x800021f0  # Third+0x50
       115:                             800021e8:  nop
       116:         random = -9;        800021ec:  break  0x7
       117:     switch (select % 7) {   800021f0:  mfhi   v0
 .     118:         case 1: printf("1\n");  break;  800021f4:  addiu  v0,v0,-1
 .     119:         case 2: printf("2\n");  break;  800021f8:  sltiu  at,v0,4
 .     120:         case 3: printf("3\n");  break;  800021fc:  beq    at,zero,0x8000225c  # Third+0xbc
 .     121:         case 4: printf("4\n");  break;  80002200:  nop
                                         80002204:  b             0x80002270          # Third+0xd0
 [OVER] [INTO] [INSTR] [UP] [GO] [LOAD] [STOP] [SNAP]   [INSTR] [BYTE] [HALF] [WORD] [ASCII] [SNAP]

┌──────── wcdbrssw - Special Registers ──┐ ┌──────── wcdbrssw - Calls ──────────────┐
   badv: 00000001                         0 Third(select=1, random=-1, message=0x80004f8c)
     sr: 3028a001  (cu=3 bev TS pe CM pz swc isc imsk+  1 Second(aaa=1, bbb=2, ccc=3)        [cdbdemo.c:97]
  cause: 00000024  (bd ce=0 ip=00 sw=0 exccode=bp)    2 First(i=1, j=1, k=1)                [cdbdemo.c:138]
    epc: 800021b4                         3 main(argc=1, argv=0x80005d34)      [cdbdemo.c:79]
   prid: 00000230  (imp=02 rev=30)
```

Debuggers

There are two debuggers that communicate with RSS. Both debuggers utilize the host computer to manage the user interface, symbol tables, file systems, etc. The RSS-MIPS serves as a target-resident server kernel for the debuggers.

These debuggers work with the RSS-MIPS target-resident debug kernel to provide very low-cost debug stations. The same debuggers work with the EPI instruction set simulator and the in-circuit emulators for more difficult debugging situations.

Symbolic Assembly-Level Debugger

MON, a symbolic assembly-level debugger, offers features especially useful to hardware engineers for prototype debug, automated testing, and manufacturing test. It is source-language independent, making it equally useful debugging code written in assembly, C, A, or other languages.

Source-Level Debugger

EDB is an exceptional source-level debugger for C/C++. You can follow execution in the source window, view formatted data in the value window, and track the nesting of routines in the Call Stack Summary window. EDB also accepts a rich set of command-line directives while "point and click" entry of common commands gives fast, flexible control over the behavior of your application.

EDB displays variables in their declared type. It displays C structures in the same format you might code them yet, allows custom formatting.

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Model RSS-MIPS Target-Resident Kernel

Salient Features

▶ Low-cost, source-level debug environment

▶ Fast binary communications interface

▶ Preconfigured ROMs for NEC evaluation boards

▶ High-speed serial or optional Ethernet communications driver

▶ Uses minimal target resources

▶ Callout interface for FLASH EPROM breakpoints

▶ Sample start-up and exception handler code

CPUs Supported

VR43xx, VR5000, VR54xx

Host Platforms

Sun-4: SunOS, Solaris

PC: Windows 95/NT

HP 9000: HP-UX

Product Overview

RSS is a target-resident kernel which runs on any VR43xx or VR5xxx target board. It implements the functions that enable host-resident debuggers to download application programs, read and write memory and registers, set and clear software breakpoints, and perform processor control, such as start and stop execution and single stepping.

RSS communicates with the host computer using a standardized packet protocol and can be configured for serial or Ethernet communications interface. The target-resident portion of RSS is a debug "kernel" that is supplied in linkable object form. It is designed to use minimal target resources, needing only 25 KB of memory, and is structured for easy porting to new target designs. Sample source code is provided for processor initialization and startup, exception handling, and for the host communications interface. Binary ROM images for NEC evaluation boards are included.

RSS features a powerful background mode that allows you to interactively debug your application program while it is still running. This is especially important for real-time designs where stopping the processor invalidates a particular test.

Full source for RSS is available at low cost for customization purposes. The standard RSS product is licensed for unlimited use and production distribution for a single project. You can ship RSS embedded into your final product for field testing or remote debugging.

RSS turns your product into a low-cost and highly capable software debug station.

Debuggers

There are two debuggers that communicate with RSS.

EDB is a powerful windowed source-level debugger for C and assembly language programs. For rapid debug of your C code, EDB fully integrates C source-level debugging with the capabilities of the emulator, including synchronizing the source window with the trace display.

MON-MIPS, a symbolic assembly-level debugger, offers features especially useful for testing board-level resources, automated testing, and manufacturing test. It is source-language independent, making it equally useful debugging code written in assembly, C, ADA, or other languages.

EPI

Target Resident Debug Kernel

HOST   TARGET

```
  ┌─────────┬─────────┐                    ┌─────────┬─────────┐
  │ MON or  │  COMM   │   ◄──────────►     │  COMM   │ KERNEL  │
  │  EDB    │         │                    │  <1 KB  │ <24 KB  │
  └─────────┴─────────┘                    └─────────┴─────────┘
              Ethernet or RS-232-C
```
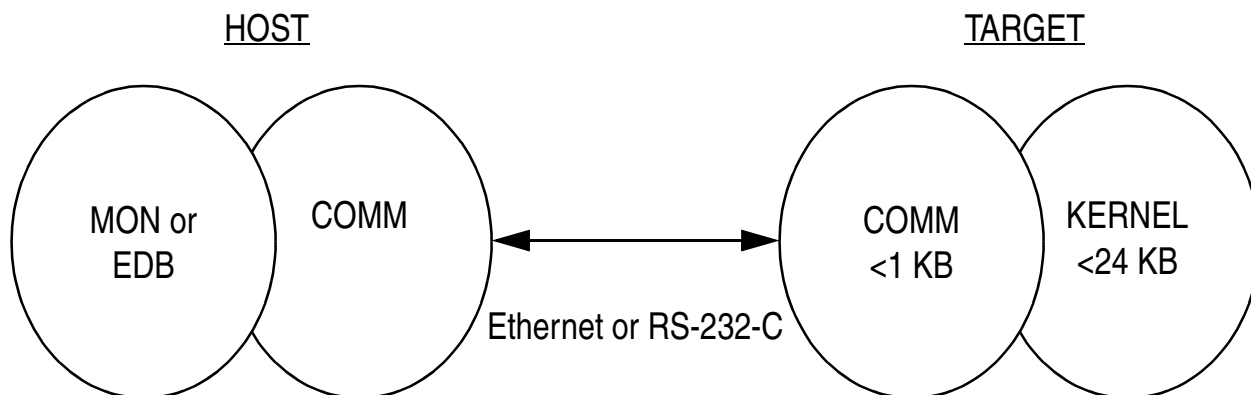
Both debuggers employ the facilities of a host computer to manage the user interface, symbol tables, file systems, etc. This leaves the emulator free to manage and track the target system.

These debuggers also work with the RSS target-resident debug kernel to provide very low-cost debug stations. Without learning a new debugging interface, developers can easily access networked emulators when their power is needed to track down the elusive bugs that can kill a development schedule.

Source-Level Debugger

EDB is an exceptional source-level debugger for C. You can follow execution in the source window, view formatted data in the value window, and track the nesting of routines in the Call Stack Summary window.

"Point and click" entry of common commands gives fast, flexible control over the behavior of your application. EDB also accepts a rich set of command-line directives.

EDB displays variables in their declared type. It displays C structures in the same format you might code them yet allows custom formatting.

The debugger is also compatible both with ISS, the instruction set simulator, and with EPI's in-circuit emulators.

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Model EDB-MIPS Source-Level Debugger

Salient Features

‣ Windowing GUI user's interface

‣ Command-line or mouse control

‣ Supports command files and command aliases

‣ Assembly-level subsystem

‣ Hyperlink to align source display to traced data or memory windows

‣ Quality technical support

‣ Supports MIPS ISA I, II, III, IV

CPUs Supported

VR43xx, VR5xxx

Host Platforms

Sun-4: SunOS, Solaris

PC: Windows 95/NT

HP 9000: HP-UX

Product Overview

EDB is an exceptional windowed source-level debugger for C and assembly language programs. You can follow execution in the source window, view formatted data in the value window, and track the nesting of routines in the Call Stack Summary window.

"Point and click" entry of common commands gives fast, flexible control over the behavior of your application. EDB also accepts a rich set of command-line directives.

The value watch window can EDB displays variables in their declared type. It displays C structures in the same format you might code them, yet allows custom formatting.

The debugger offers convenient windows to display the general registers and the coprocessor registers too.

The debugger provides a common user interface, whether debugging using the ISS instruction set simulator, the RSS target-resident debug kernel, or the models SYS4K or MAJIC emulators.
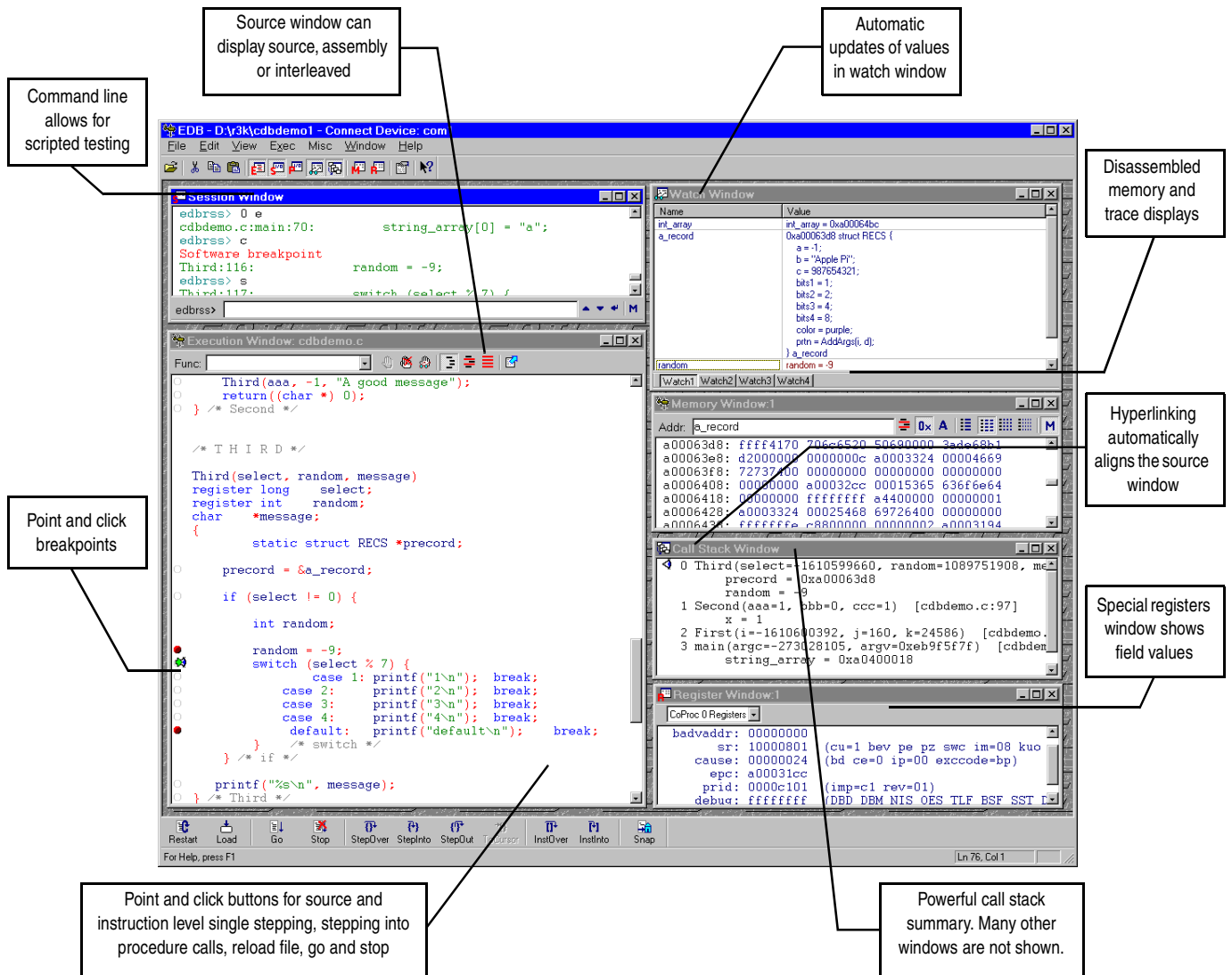
EPI

Source window can display source, assembly or interleaved

Automatic updates of values in watch window

Command line allows for scripted testing

Disassembled memory and trace displays

Point and click breakpoints

Hyperlinking automatically aligns the source window

Special registers window shows field values

Point and click buttons for source and instruction level single stepping, stepping into procedure calls, reload file, go and stop

Powerful call stack summary. Many other windows are not shown.

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Green Hills Ada 95 MIPS Compiler

Salient Features

▸ Industry's first fully validated Ada 95 compiler and software development environment for 32-bit embedded architectures

▸ Optimizing Ada compiler generates the fastest code in the industry

▸ Full Support for Ada language, including optional Chapter 13 features

▸ New task and synchronization features (Protected Types)

▸ Type extensions of Tagged Types and Child Library Units

▸ New hierarchical library organization

▸ Systems programming annex

▸ Real-time systems annex

▸ Numerics annex

▸ Ada, C, C++, embedded C++, and FORTRAN can be mixed into a single executable

▸ Supports the new MIPS16 ISA processor

▸ Produces extended debug information which allows the MULTI® debugger to be a true Ada debugger

▸ Big- and little-endian addressing

▸ Fully validated with VxWorks/Tornado and Solaris

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Supports most UNIX workstations, including Sun, HP, PC/Windows 95/98/NT, and more

Language Standard

Green Hills™ Ada is an optimizing Ada compiler with full support for the Ada language.

Optimizations

Green Hills optimization technology applies hundreds of optimizations to generate the best possible code, including:

• The capability to select an optimization that allows for speed or size

• Loop optimizations can be enabled on a function-by-function basis

• Fine user control of optimizations allows a program to be trimmed for best possible performance

• Small data area allows often-used variables to be gathered into a 64 KB memory block so that they can be accessed with a single instruction

• Functions can be automatically inlined across modules and even across languages

Embedded Features

Seventeen years of supporting the embedded market has yielded many features for embedded programming, including

• Multiple program and data sections

• Separate allocation of variable and constant data

• Startup routine to initialize variables

• Interrupt-level procedures

• Linker directive file

• Supports the new MIPS16 ISA processor

Green Hills
·S O F T W A R E , I N C.·

Debug Information

Extended debug format allows debuggers to handle Ada constructs (such as generics, scaled integer data types, attributes, and exception handling). Debug information is generated for optimized code.

Memory Models

- Big- or little-endian addressing
- Position-independent code performs branches, calls, and local variable accesses relative to the personal computer
- Position-independent data accesses globals relative to a base register

Object Formats

- COFF
- ELF/DWARF

Object format conversion utilities generate Motorola S-records, IEEE-695, and others.

Special Target Support

- VxWorks/Tornado

Libraries

The compiler is delivered with a full implementation of Ada libraries optimized for embedded use:

- Specially coded to be small and efficient
- Unused routines and data structures not linked into executable
- Hardware or software floating point
- Big- or little-endian addressing
- Source code available

Validation

Extensive testing ensures code you can rely on that has been validated against official DOD Ada validation tests and extensive Green Hills test suites.

Ada for Native Hosts

Fully compatible native compilers are available for most UNIX workstations and Windows 95/98/NT PCs. This allows portions of an application to be developed natively on the host, then included in an embedded program with a simple recompile. This is useful when target hardware is scarce.

On native hosts, Ada tasking is supported within a single process. The MULTI debugger has extensive support for Ada tasking, including:

- Task windows
- Ability for debugger to switch between tasks

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Green Hills C-MIPS Compiler

Salient Features

◗ Optimizing C compiler generates the fastest code in the industry

◗ Capability to mix C, C++, Embedded C++, FORTRAN, and Ada into a single executable

◗ Extended debug information

◗ Big- and little-endian addressing

◗ 64-bit integer support

◗ Compatibility with MULTI® 2000 Software Development Environment

◗ Four major dialects of the C language (K&R, Transition, ANSI, and Full ANSI) can be configured

◗ Supports the new MIPS16 ISA processor

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Supports most UNIX workstations, including Sun, HP, PC/Windows 95/98/NT, and more

Multiple Language Dialects

The C-MIPS compiler supports all major dialects of the C language, so you can compile almost any C code:

• K&R mode compiles the original C language.

• Transition mode extends the original language to include prototypes and new keywords.

• Permissive ANSI implements ANSI features, but does not enforce all the restrictions.

• Full ANSI conforms strictly to the ANSI standard.

Language Configuration Options

The C-MIPS compiler provides compile time options that support dozens of minor language variations, including:

• Default type of *char* may be signed or unsigned

• Enable/disable various classes of warnings

• Allow initialized externals, use GNU extensions, and use an alias keyword

Optimizations

Green Hills™ optimization technology applies hundreds of optimizations to generate the best possible code, including:

• Loop optimizations can be enabled on a function-by-function basis.

• Fine user control of optimizations allows programs to be trimmed for best possible performance.

• Small data area allows often-used variables to be gathered into a 64 KB memory block so that they can be accessed with a single instruction.

• Functions can be automatically inlined across modules and even across languages.

Embedded Features

Seventeen years of supporting the embedded market has yielded many features for embedded programming, including:

• Multiple program and data sections

• Separate allocation of variable and constant data

• Startup routine to initialize variables

• Interrupt-level procedures

• Linker directive file

• Supports the new MIPS16 ISA processor

Green Hills
·S O F T W A R E, I N C.·

```
mips Options for default.bld          _ □ ✕

     mips Options for default.bld    ?  ◆       ☐

Processor:  [ Default              ▼ ]
                Default
Floating Point Processor:  R1900
                           R3000
☐ Position Independent Co  R3640
                           R3700
☐ Position Independent Da  R3750
☐ PIC Compatible Code      R3900
                           R3900E
☐ MIPS Assembler Compa     RH32
☐ Little-Endian            CW400X
                           CW401X
☐ MIPS-16 Instruction Set  R4000
☐ 64 bit integers          R4100
                           R4200
☐ Far Function Calls       R4300
                           R4400
☐ Small Data Area          R4500
                           R4600
Small Data Area Thresh     R4650
                           R4700
                           R5000
```
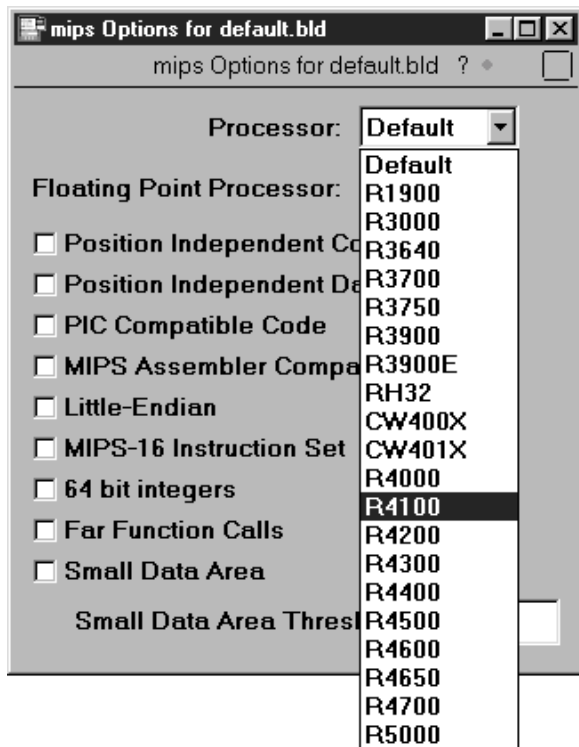
Debug Information

Extended debug format allows debuggers to recognize symbols defined with *#define* statements and *typedef keywords*. Debug information is generated for optimized code.

Memory Models

- Big- or little-endian addressing is available.
- Position-independent code performs branches, calls, and local variable accesses relative to the personal computer.
- Position-independent data accesses globals relative to a base register.

Object Formats

Object formats include COFF and ELF/DWARF. Object format conversion utilities generate Motorola S-records, IEEE-695, and others.

Kanji Support

- Allows Kanji characters in comments, character strings, and character constants
- Run-time libraries correctly process character data containing Kanji characters

Libraries

The compiler is delivered with a full implementation of the standard C library optimized for embedded use:

- Specially coded to be small and efficient
- Source code available
- Big- or little-endian addressing
- Unused routines and data structures not linked into executable
- Hardware or software floating point

Validation

Extensive testing ensures code you can rely on.

- Validated against Perennial, Plum Hall, MetaWare, and Green Hills test suites
- Entire UNIX operating system, (including the kernel and all utilities) successfully compiled

Native C for Hosts

Fully compatible native compilers are available for most UNIX workstations and Windows 95/98/NT PCs. This allows portions of an application to be developed natively on the host, then included in an embedded program with a simple recompile. This is useful when target hardware is scarce.

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Internet: http://www.adac.co.jp

Green Hills C++/EC++ MIPS Compiler

Salient Features

‣ Extended debug information that allows MULTI® 2000 debugger to be a true C++ debugger

‣ Scalable feature set; supports minimal C++ up to ANSI/ISO C++

‣ Full support for embedded C++ (EC++)

‣ Embedded C++ libraries

‣ Big- and little-endian addressing

‣ Optimizing C++ compiler generates the fastest code in the industry

‣ C++ version 3.0, including templates

‣ C, C++, embedded C++, FORTRAN, and Ada can be mixed into a single executable

‣ 64-bit integer support

‣ Supports the new MIPS16 ISA processor

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Supports most UNIX workstations, including Sun, HP, PC/Windows 95/98/NT, and more

The Language

Green Hills™ C++ conforms to the ANSI C++ standard, including support for templates, STL, namespaces, and exception handling. Language features are scalable, including embedded C++ for small code size and run-time efficiency.

Optimizations

Green Hills optimization technology applies hundreds of optimizations to generate the best possible code, including:

• The ability to select an optimization that allows for speed or size; loop optimizations can be enabled on a function-by-function basis

• Fine user control of optimizations allows a program to be trimmed for best possible performance

• Small data area allows often-used variables to be gathered into a 64 KB memory block so that they can be accessed with a single instruction

• Functions can be automatically inlined across modules and even across languages

Embedded Features

Seventeen years of supporting the embedded market has yielded many features for embedded programming, including:

• EC++
• EC++ libraries
• Multiple program and data sections
• Separate allocation of variable and constant data
• Startup routine to initialize variables
• Interrupt-level procedures
• Linker directive file
• Supports the new MIPS16 ISA processor

Debug Information

Extended debug information allows debuggers (such as the MULTI 2000 source-level debugger) to fully and seamlessly support the C++ language. MULTI 2000 evaluates C++ expressions and automatically mangles and demangles C++ names. Casts and coercions are performed implicitly, and ambiguities regarding overloaded operators are automatically resolved. Template debugging is fully supported. Debug information is generated for optimized code.
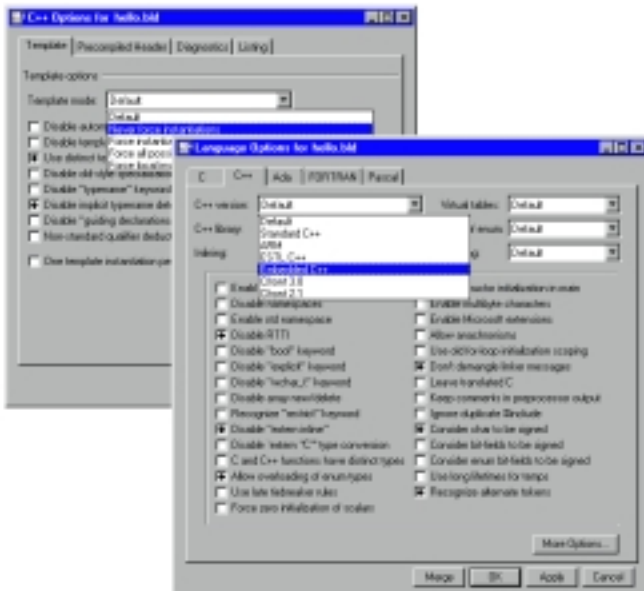
Memory Models

- Big- or little-endian addressing is available; position-independent code performs branches, calls, and local variable accesses relative to the personal computer.
- Position-independent data accesses globals relative to a base register.

Object Formats

Object formats include COFF and ELF/DWARF. Object format conversion utilities generate Motorola S-records, IEEE-695, and others.

Libraries

The compiler is delivered with a full implementation of the standard C and C++ library optimized for embedded use:

- Specially coded to be small and efficient; unused routines and data structures are not linked into executable
- Hardware or software floating point
- Big- or little-endian addressing
- Source code available

Validation

Extensive testing ensures code you can rely on.

- Validated against Perennial and Green Hills test suites
- Validated against bodies of C++ code, including NIH class library, Stanford InterViews, and GNU groff

Native C++ for Hosts

Fully compatible native compilers are available for most UNIX workstations and Windows 95/98/NT PCs. This allows portions of an application to be developed natively on the host, then included in an embedded program with a simple recompile. This is useful when target hardware is scarce.

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Green Hills FORTRAN MIPS Compiler

Salient Features

◗ Optimizing FORTRAN compiler generates the fastest code in the industry

◗ Support for the major dialects of the FORTRAN language (ANSI, F77, VMS, DOD, and extended)

◗ C, C++, Embedded C++, FORTRAN, and Ada can be mixed into a single executable

◗ Extended debug information that allows the MULTI® 2000 debugger to be a true FORTRAN debugger

◗ Big- and little-endian addressing

◗ 64-bit integer support

◗ Supports the new MIPS16 ISA processor

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Supports most UNIX workstations, including Sun, HP, PC/Windows 95/98/NT, and more

Multiple Language Dialects

The FORTRAN MIPS compiler provides support for the major dialects of the FORTRAN language and allows you to compile almost any FORTRAN code.

- ANSI mode implements the ANSI standard
- F77 mode mimics the UNIX F77 compiler
- DOD mode adds the DOD extensions
- VMS mode compiles the language as defined by DEC's VAX/VMS compiler
- Extended mode implements a nonconflicting union of these, plus many extensions

Language Configuration Options

The FORTRAN MIPS compiler provides compile-time options that support dozens of minor language variations, including:

- Setting default type for INTEGER to be INTEGER*2
- Allowing for case-sensitive variable names
- Executing at least one iteration of every DO loop
- Keeping local variables in registers or on stack (with the side effect that values are not saved from one call to the next)

Debug Information

An extended object format allows debuggers to handle COMMON and EQUIVALENCE variables, arrays with lower bounds other than 0, ENTRY statements, and column major arrays. Debug information is generated for optimized code.

Libraries

A full implementation of FORTRAN and standard C libraries is optimized for embedded use:

- F77 run-time libraries per ANSI standard
- VMS run-time libraries compatible with DEC's

Validation

Extensive testing ensures code you can rely on. The code is validated against U.S. Department of Commerce and Green Hills test suites.

Green Hills™ FORTRAN offers the same optimizations, embedded features, memory model support, object formats, and native compiler availability as the Green Hills C compiler (see entry for Green Hills C-MIPS).

Green Hills
·S O F T W A R E ,   I N C.·

Green Hills FORTRAN Language Extensions

Input/Output

- ENCODE/DECODE
- Full VAX syntax for OPEN and CLOSE statements
- IBM ('n) form of relative record specification
- ACCEPT statement and TYPE statement
- VMS-style indexed I/O extensions (VMS mode only)
- NAMELIST (VMS mode or -namelist)

Expression Extensions

- %VAL, %REF, and %LOC
- Concatenation of indeterminate-length strings
- Functions and ENTRY statements that return in definite-length strings
- Logical in Integer context (VMS mode)
- Integer in Logical context (VMS mode)

Line Formatting

- Continuation convention extension: tab character followed by any digit 1–9 and ! comments
- Up to 99 continuation lines and INCLUDE statement
- D in column 1 for debug statement (VMS mode)
- Free format lines (F77 mode) and as continuation marker (F77 mode)

Initialization Extensions

- Initialization in variable declaration
- Initialize CHARACTER variables with integer values (VMS mode)

Format Extensions

- 0 (octal) edit descriptors
- Z (hexadecimal) edit descriptors
- H edit descriptor on input
- Q edit descriptor
- $ edit descriptor
- Default field widths for edit descriptors '$' and '/o' carriage control

Built-In Subroutine and Function Extensions

- Degree trig functions
- System subroutines DATA, IDATE, RAN ERRSNS, EXIT, SECNDS, and TIME
- DOD functions IOR, IAND, INOT, IEOR, ISHFT, IBITS, MVBITS, BTEST, IBSET, and IBCLR (VMS mode, DOD)

Statement Extensions

- DO WHILE statements

- END DO statement
- Extended range DO loops
- Ampersand (&) for alternate return (VMS mode)
- OPTIONS statement (VMS mode)

Declaration Extensions

- INTEGER*1, *2, *4
- LOGICAL*1, *2, *4
- BYTE data type
- DOUBLE COMPLEX data type
- POINTER data type
- DATA statement anywhere in program unit
- IMPLICIT NONE statement
- VOLATILE statement
- "*n" size qualifier on function names and identifier declarations
- STRUCTURES and UNIONS
- Extended PARAMETER statement (VMS mode)
- Single subscript in EQUIVALENCE of multidimensional array (VMS mode)

Lexical Extensions

- $ and _ in identifiers
- Names to 31 characters
- Hollerith constants
- Radix 50 constants (VMS mode)
- Topless octal and hex constants (VMS mode)
- Strings enclosed in "as well as" (F77 mode)
- C-style backslash chars in strings (F77 mode)

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MULTI® 2000 Software Development Environment

Salient Features

- Source-level debugger
- Project Builder
- Performance Profiler
- Graphical browser
- Version control system
- Run-time error checking
- Text editor
- Event analyzer
- Communication between components provides enhanced functionality
- Support for both embedded and native development

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Supports most UNIX workstations, including Sun, HP, PC/Windows 95/98/NT, and more

Green Hills
·SOFTWARE, INC.·

Integrated Development Environment

The MULTI® 2000 Software Development Environment provides a framework of interactive tools to support program development by small or large workgroups. MULTI 2000 includes all the tools you need to support a major programming project.

Mixing Languages

MULTI 2000 supports program development in Ada, C, C++, embedded C++, FORTRAN, and assembly language. Source code from these languages can be mixed together in almost any combination to create a single executable. MULTI 2000 supports both embedded and native development, so programmers who do both types need only a single set of tools.

Source-Level Debugger

The MULTI 2000 debugger is a powerful windowing source-level debugger that enables program loading, execution, run control, and monitoring. MULTI 2000 provides an exhaustive set of debug features, designed to make it easy to find and fix bugs. Debug features include setting breakpoints, specifying conditional breakpoints, single stepping, examining variables, invoking data display windows, local variables display, and displaying stack trace and C++ objects.

Project Builder

The Project Builder provides an advanced means of controlling compilation that is easier to use than *make*, provides more project control, and works identically on all systems. Configure your program simply by listing your files; all dependencies are resolved automatically. The builder communicates with the compilers to allow automatic inlining across source modules and across languages.

Performance Profiler

The Performance Profiler provides detailed and summary profiling information to enable the developer to identify the code where execution consumes the greatest amount of time as well as how many times a given procedure or block of code was executed. This helps users select the best optimizations for a particular section of code.

Version Control

The integrated version control system automatically checks files in and out as you edit them. Named checkpoints can be
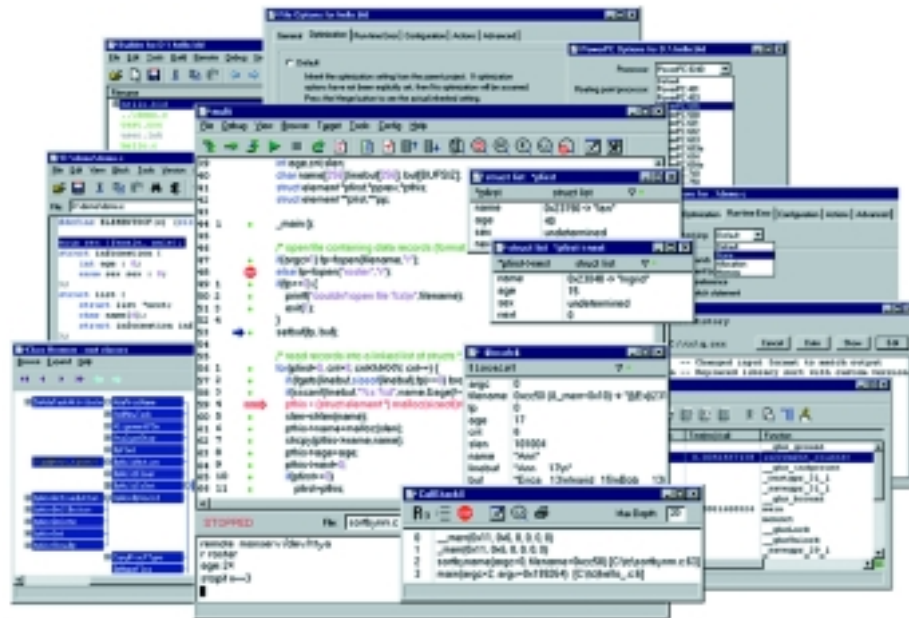
created at any time so that you can later retrieve the source code corresponding to an intermediate program version. Portions of your program can be split off into separate branches for development when major changes are required, then automatically merged back into the mainline program when the changes are finished.

Run-Time Error Checking

MULTI's run-time error checking capabilities can provide useful information on a wide variety of run-time errors. MULTI detects the errors when they first occur, rather than later, when they manifest themselves through secondary effects. MULTI can check for several errors, including memory leaks, assignment bounds, and unused variables.

Graphical Browser

The graphical class browser is an easy-to-use tool to help you visualize class hierarchies. Many portions of the graphical display are active. For example, clicking the name of a class opens a display window on that class and breaks out its members.

Text Editor

The powerful editor is designed specifically to run under a window manager and is fully configurable to meet your individual style.

Supports Native Development

The MULTI 2000 Software Development Environment supports native development on most UNIX hosts. This allows the same tools to be used for both embedded and native development.

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MULTI 2000 Source-Level Debugger

Salient Features

▶ ROM monitors available for many commercial CPU boards

▶ Capability to interface MULTI® 2000 to any hardware using ROM monitor source

▶ RTOS support for velOSity, INTEGRITY, ThreadX, Nucleus PLUS, Vxworks/Tornado, custom RTOSs, and more

▶ Same debugger for both native and embedded development

▶ Capability to debug programs written in Ada, C, C++, embedded C++, FORTRAN, or assembly language

▶ Multitask debugging (each process with its own debug window)

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Supports most UNIX workstations, including Sun, HP, PC/Windows 95/98/NT, and more

Target Support

MULTI 2000 can be used to debug most target systems. It can be used in conjunction with software simulators, ROM monitors, in-circuit emulators, and many commercial real-time operating systems. MULTI 2000 is also available for native development on most UNIX and Windows 95/98/NT systems. This allows programmers to use the same tools for both native and embedded development.

Full-Function Windowing Debugger

The MULTI 2000 debugger takes full advantage of the properties of a windowing environment to bring you more features and greater ease of use than any debugger you've ever seen. In addition, it has many advanced features, including special support for multiple processes, X-Window development, and embedded programming. Class and program browsing capabilities enable you to understand the structure of your program and of programs you inherit.

True C++ Debugging

MULTI 2000 is a true C++ debugger, with support for C++ seamlessly integrated at every level. It evaluates C++ expressions and automatically mangles and demangles C++ names. Casts and coercions are performed implicitly, and ambiguities regarding overloaded operators are automatically resolved. Template debugging is fully supported. MULTI 2000 also supports true debugging for Ada, C, Embedded C++, and FORTRAN.

Green Hills
·SOFTWARE, INC.·
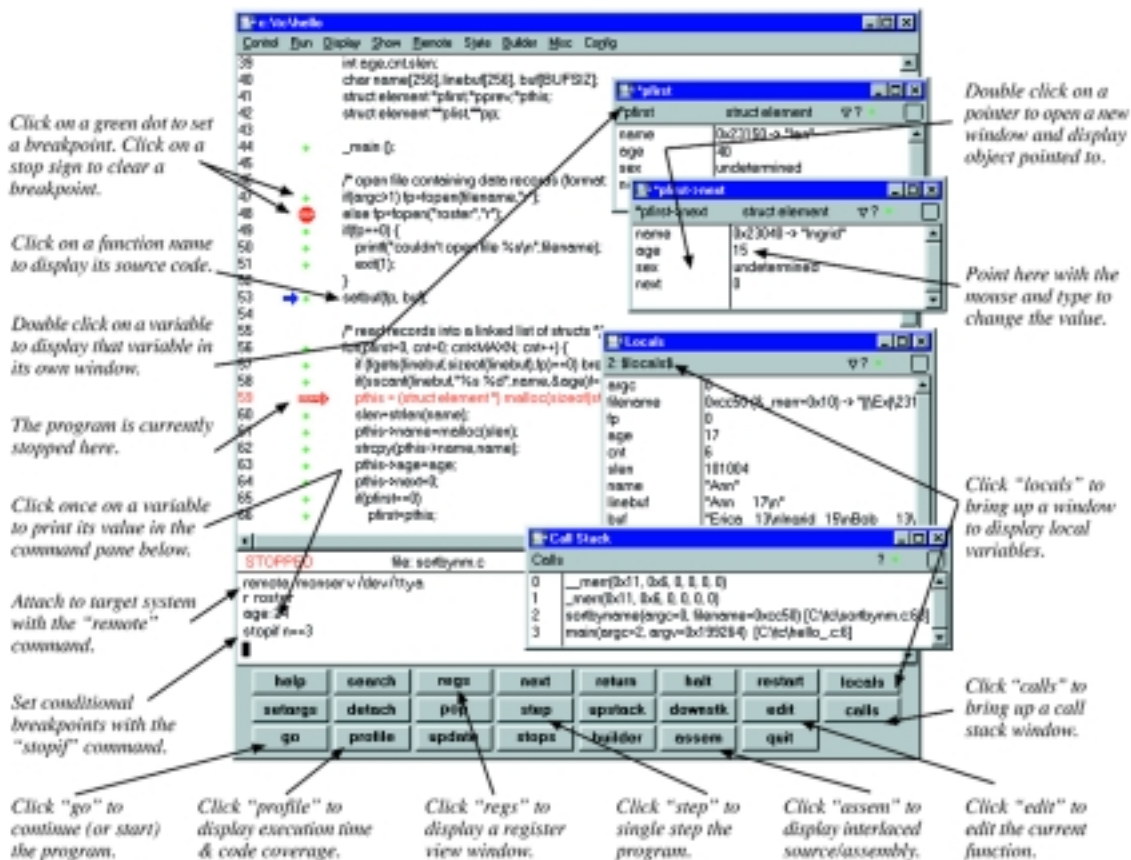
As shown here, the MULTI 2000 source-level debugger supports programming in Ada, C, C++, Embedded C++, FORTRAN, and assembly language. Its basic functions are intuitive and simple to use. Programmers can generally do useful work simply by starting MULTI 2000 and following their instincts. The captions on the accompanying diagram illustrate the basic functionality of the debugger.

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Windows CE Platform Builder

Salient Features

▶ Microsoft® Windows® CE is a compact, real-time OS based on the Win32® API

▶ Platform Builder offers an integrated development environment for Windows CE-based products

▶ The Platform Wizard matches platform needs with 8 different configurations

▶ Allows easy input of Board Support Packages (BSPs) and drivers

▶ Allows creation of a software development kit (SDK) for custom platforms

CPUs Supported

NEC VR41xx, VR43xx

Product Overview

Platform Builder is the next-generation set of tools and APIs that enables you to develop the software for your next embedded system project using Windows CE. Platform Builder includes all of the components of the Windows CE operating system in binary form, along with sample code for NDIS and USB device drivers that make development easier.

Platform Builder includes eight prebuilt configurations of the Windows CE operating system. These configurations range from only core kernel functionality to a complete system with a rich graphical user interface and preloaded applications. The Integrated Development Environment (IDE) makes your embedded system development easier.

Configuring the Windows CE operating system for your custom device in Platform Builder is very similar to building an application in the Microsoft Visual Studio® development environment. The Platform Builder IDE, like the Visual Studio IDE, enables you to configure, build, and debug your software all within this consistent environment. The Platform Builder Export SDK feature allows you to create an SDK for your custom device.

Application developers can import their Software Development Kit (SDK) into the Windows CE Toolkit for Visual C++® or the Windows CE Toolkit for Visual Basic® and develop the application-level software for a platform. The SDK consists of the APIs, header files, etc. that comprise the operating system environment for a custom device. The extensible "Catalog" allows you to easily incorporate third-party components into the Platform Builder IDE.

Platform Builder Catalog is a repository of Windows CE components. Using drag and drop you can add components from the catalog to a platform. You can extend the catalog by adding your own components, or components developed by third parties. Platform Builder enables you to target the processor families supported by Windows CE.

For the latest list of supported processors, or for more information on Windows CE and Platform Builder, visit:

http://www.microsoft.com/windowsce/embedded

Microsoft® Windows® CE

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Internet: http://www.microsoft.com/windowsce/embedded

Windows CE

Embedded Visual Tools

Visual Basic for Embedded Devices

To help you take advantage of new business opportunities, Microsoft has created a version of Visual Basic specifically for embedded devices. This toolkit, which integrates with the Microsoft Visual Basic development environment, is the most productive way to build applications for Windows CE-based devices. It supports familiar Visual Basic features, including visual design and IntelliSense® technology, making it easy to apply your knowledge of Visual Basic to Windows CE-based devices.

Familiar Environment Gets You Up and Running Fast

- Use your existing knowledge and training to quickly create Windows CE-based solutions within the same development environment you use for traditional Windows-based applications

- Use Visual Basic IntelliSense® technology to increase your productivity with on-the-fly programming assistance, including statement completion, parameter information, and syntax error checking

- Build applications for Windows CE efficiently by dragging Windows CE-specific components from the toolbox and dropping them onto the Visual Basic Form Designer

Comprehensive Access to Windows CE Platform Increases Productivity

- Save time by using COM/OLE, the world's most successful and powerful component model, to build reusable solutions for Windows CE-based devices

- Develop compelling, commercial-quality applications by using the DECLARE statement to gain direct access to custom Dynamic Link Libraries (DLLs) and Windows CE operating system functionality

- Build compelling mobile applications by accessing communication protocols such as TCP/IP via an infrared or serial port

- Save time and eliminate duplication of effort by reusing ActiveX® code modules

Salient Features

◗ Target a Windows® CE componentized OS

◗ Integrated into the Developer Studio visual development environment

◗ Cross-compilers optimized for each CPU family

◗ Debug, check memory, edit the registry, and manipulate the file system using the remote tools

◗ ROM Image Maker produces a binary image of your software for burning into ROM

CPUs Supported

NEC VR41xx, VR43xx

Microsoft®
Windows® CE

Visual C++ for Embedded Devices

With its power, familiarity, and flexibility, Microsoft has created a version of Visual C++ specifically for embedded devices. If you're a Win32 developer today, you can use the Windows CE Toolkit and your existing Visual C++ knowledge to access the entire Windows CE operating system. The toolkit supports features such as visual design and IntelliSense technology, making it the most efficient way to build Windows CE-based applications. Plus, it's readily extensible, so you can develop for all of today's Windows CE-based PC Companions, as well as tomorrow's devices.

Use Windows-based Development Tools To Create Full-featured Portable Applications

- You can use the Microsoft Foundation Classes (MFC) framework for Windows CE to create stand-alone executables or DLLs. With MFC for Windows CE, you can build anything from a simple dialog-box-based program to a sophisticated application that employs the full MFC document/view architecture.

- With the Active Template Library (ATL) for Windows CE, you can create small, fast Microsoft ActiveX® components and COM objects, and cut development time by using the ATL to create composite controls that host multiple Microsoft ActiveX or Windows-based controls.

- The Windows CE Toolkit enables you to build business applications that take advantage of the ActiveX Data Objects Control (ADOC) for Windows CE. ADOCE—a subset of ADO—includes an internal database provider, so Windows CE-based applications can access databases that are stored locally on a device.

- Free, pluggable SDKs let you build for all Windows CE-based devices: palm-size PCs, handheld PCs, handheld PC Pros, and auto PCs. Use pluggable SDKs to keep the toolkit up to date and be the first to develop for newly released devices.

For more information on our toolkits, please visit:

http://www.microsoft.com/windowsce/embedded

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Internet: http://www.microsoft.com/windowsce/embedded

PMON Tools for Debugging Software Applications

Salient Features

‣ Complete source code available

‣ No redistribution or royalty fees

‣ Robust debug monitor

‣ Source-level debugging using MIPS-targeted version of gdb

‣ Local, remote, and transparent connection modes to a host

‣ Able to download binary files over Ethernet via TFTP

‣ Memory display, disassembly, copy, fill, and search

‣ C Shell-style command history support

‣ Drivers for standard UARTs

CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms

PC and UNIX hosts

Powerful Tool for RISC-Based Systems

PMON provides a flexible environment for users to perform debugging. Users can incorporate any of the code from the PMON source package into their own products with no redistribution or royalty fees. PMON provides command history, command-line editing, and downloadable symbols. PMON can also function as the target system back end for a symbolic debugger running on a host machine; compatible debuggers include gdb or the MIPS/SGI version of dbx.

Use of PMON involves three basic steps:

• Users first develop code on their own workstations or PCs, and cross-compile the code on these host machines.

• Users then download their code to the target board using either an RS-232-C or Ethernet link.

• After the code is downloaded, users use PMON's facilities to debug their code.

Debugging Facilities

PMON debugging facilities permit the user to start and stop program execution at any point via hardware and software breakpoints; up to thirty-two software breakpoints can be used. Single-step execution is also supported by PMON. The user is able to read any register contents and set any register to a new value. For the main memory, the user can read data, disassemble code from memory, copy memory contents from one area to another, fill areas of memory with a particular byte or string, or search memory for a particular byte or string. The memory test function is also provided by PMON.

Download Support

PMON provides four download formats: LSI Logic's FastLoad Format, Motorola S-records, ELF, and ECOFF binary object files via Ethernet.

The programs and data can be downloaded from a host machine to a target board by using a serial RS-232-C link. Two ports on the target board may be used, one for issuing monitor commands or for dumping data and another for transferring files.

PMON supports high-speed downloading and remote file access over Ethernet via TFTP. Several environment variables must be set to control the access to Ethernet. Command 'ping' in PMON can be used to test the network setup.

NEC

PMON Monitor Commands

Thirty-four commands are included in PMON to support software/hardware debug. These commands can be grouped into four categories: Execution Control (breakpoint, continue, call, delete breakpoint, go, trace, and trace over); Display and Modify (network loader, stack back-trace, copy, display, dump, fill, disassemble, download, memory display/modify, register display/modify, and search); Environment (display/set date and time, history, list symbols, screen-at-a-time display, set environment variables, command shell, set terminal options, set symbolic name, and remove environment variables); and Miscellaneous (enter remote debug mode, flush data and/or instruction cache, help, memory test, network test, and transparent mode).
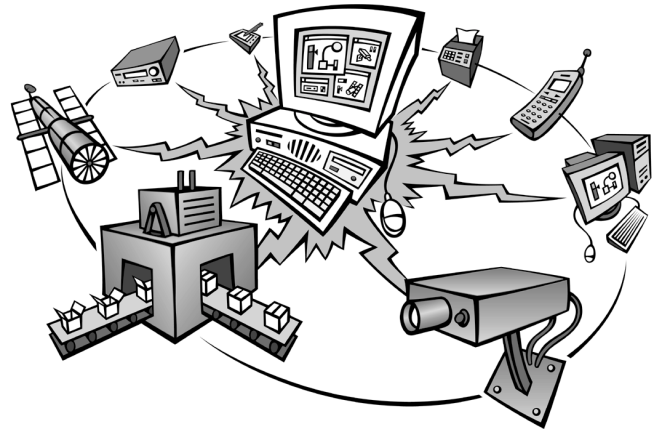
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NetPeer

Embedded Desktop Interface and Distributed Operating System

Salient Features

- Multiuser and C callable

- Simple, using standard Java-like methods—no need to learn Java or load it on the target

- Small, scalable, with only a 16 KB footprint on the target system

- Network independent using a BSD interface

- RTOS independent

- HYPERLINK free workstation application and source code examples at http://www.netpeer.com

CPUs Supported

NEC Vr43xx, Vr44xx

Product Overview

NetPeer allows you to create a dynamic target-to-desktop interface for your embedded project. With an ultra-small 16 KB footprint, NetPeer provides real-time, interactive multiuser GUIs, file access, multimedia, images, audio, and database access. Incorporate NetPeer on your embedded target to communicate with NetPeer on any workstation.

NetPeer's embedded target module is a C library requiring less than 16 KB of code space and 2 KB of RAM. This library is built to meet the needs of your processor and compiler. The free workstation component is an application that provides access to desktop services for any NetPeer embedded target. Both components can initiate communication to any NetPeer system.

NetPeer operates in almost any embedded application and workstation environment. On the target, it runs independently of your TCP/IP stack configuration and RTOS. The only workstation requirement is that it be capable of running the Java run-time environment. You can use almost any communication protocol, including TCP/IP, IrDA, RF, Ethernet, and PPP. With NetPeer, you can write a dynamic, functional interface in as little as 30 minutes. It's simple because the infrastructure already exists on the workstation module.

U S SOFTWARE
E M B E D D E D   E X C E L L E N C E
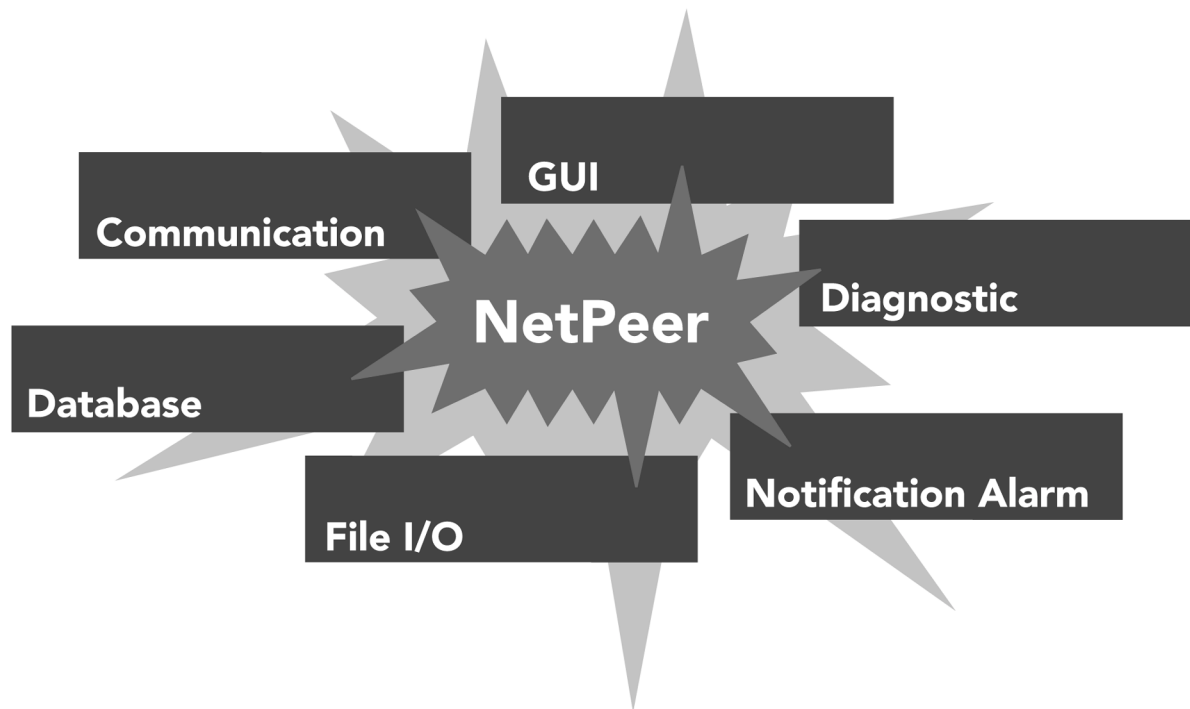
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USFiles DOS/Windows File System

Salient Features

◗ Processor independent

◗ RTOS independent

◗ Royalty free

◗ ROMable and reentrant

◗ Includes full source code in ANSI C

◗ User configurable

◗ Supports long file names (VFAT) and Kanji characters

◗ DOS-/Windows-compatible file system

◗ Supports ANSI C file I/O interface

◗ Supports binary and text files

◗ Accesses directories as files

◗ Includes dynamic .EXE loader

◗ Compatible with SuperTask! and TronTask!

◗ Includes product conformance test

◗ HYPERLINK CompactFlash add-on product available

◗ Support for HYPERLINK CD-ROM file system, available as an add-on product

CPUs Supported

NEC VR43xx, VR44xx

Product Overview

USFiles is a DOS-/Windows95-compatible file system designed to be target processor and RTOS independent. USFiles can operate in a stand-alone mode and because it is reentrant, it supports multitasking RTOSs such as our SuperTask! and ITRON-compliant TronTask! products. USFiles also supports standard ANSI C file I/O function calls. Source code is included and there are no royalties.

USFiles may be customized for operation with a floppy or hard disk by supplying a read sector and write sector function. If time-stamping of files is desired, a date/time function can also be supplied. *Complete source code is provided.*

USFiles may be used directly with an application or in conjunction with a multitasking system. Seamless support is provided for SuperTask! and TronTask!. Use with other multitasking executives requires minimal customization. USFiles is designed to allow multiple tasks to access files simultaneously.

USFiles is delivered with a driver that provides floppy and hard disk access through BIOS calls. RAM disk support is also provided. For 80x86 targets, additional drivers are provided that allow direct floppy and hard disk access in the absence of BIOS.

Drivers for supporting compact/ATA flash are available as stand-alone products or as add-ons to USFiles.

USFiles supports the same ANSI C user interface and functionality across all processors. You can take standard C code developed for one processor, recompile it, and move the code to another processor with minimal effort.

U S SOFTWARE
EMBEDDED EXCELLENCE

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Optimizing C, C++, and Java Compilers

Salient Features

◗ Highly optimizing compiler suites for C, C++, and Java™

◗ Fast, compact, high-quality code for NEC MIPS CPUs

◗ Application-specific (profile-driven) optimizations for increased performance

◗ Run-time analysis tools, including run-time error checker and profiler, for improved code quality, performance, memory usage

◗ FastJ™ compiles Java to native machine code for applications without a JVM

◗ Powerful SingleStep GUI debugger for advanced C, C++, Java, and ASM debugging

◗ Task-/kernel-aware debug

◗ Exceptional flexibility and reliability for embedded applications

◗ Proven with leading RTOS and kernel packages

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

## Host Platforms

Windows 95/98/NT, Solaris, HP-UX

Target Connections Supported

Simulators, ROM monitors, OCD/JTAG, HP logic analysis systems

Highly Optimizing Compilers

The Diab compiler suites are the expert's choice for demanding NEC MIPS-based designs. These compilers feature the industry's most advanced compiler optimization techniques and offer superior performance, flexibility, and reliability. In addition to providing robust, standards-compliant compilers for C, C++, and Java, Diab tools offer many features specific to embedded development. These features include: generating ROMable code and data; ability to mix assembler with C/C++ and Java code; ROMable reentrant code and libraries; options to pack or byte-swap structures to match existing data types; and complete control of code and data memory allocation and placement.

For developers who want to program in Java but cannot afford the performance and size costs of a JVM, Wind River offers the FastJ compiler suite. FastJ compiles Java source code directly to native machine code and offers code size and performance comparable to C++. FastJ also supports mixed-language programming so you can mix native C and ASM code with Java code. The SingleStep debugger features Java-specific capabilities that allow you to debug Java and mixed-language applications. FastJ interfaces to an RTOS using Pthreads calls (a subset of POSIX). Check with Wind River to see if your RTOS/kernel is supported.

WindRiver®
S Y S T E M S
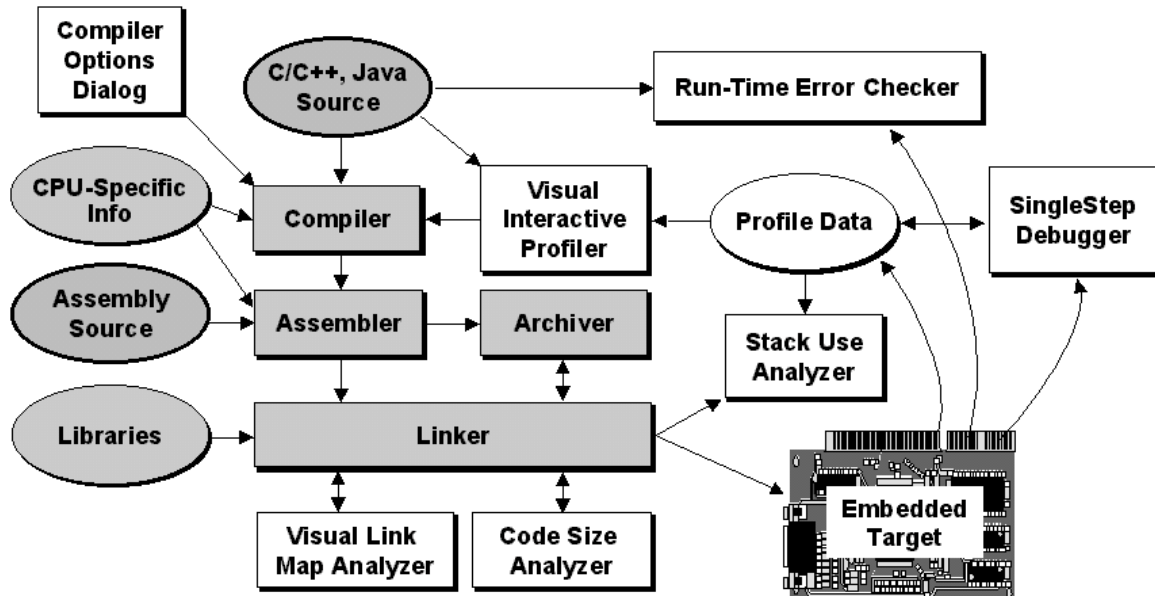
Run-Time Analysis (RTA) Tools

The award-winning RTA Suite provides an integrated set of run-time analysis tools to help you develop higher quality, higher performance code in less time. The RTA Suite includes a powerful Run-Time Error Checker, Visual Interactive Profiler, Stack Use Analyzer, Visual Link Map Analyzer, Code Size Analyzer, and other tools to help you improve program reliability, performance, and memory usage. In particular, the Run-Time Error Checker detects hard-to-find pointer errors and memory leaks, while the profiler identifies true program hot spots for optimization purposes. Diab compilers can also generate application-specific optimizations based on run-time profile data.

SingleStep Debug Solutions

The SingleStep debugger is a powerful debugging environment for embedded development. Graphical source-level and assembly-level debug features are combined with a wide array of tools to provide a rich environment for debugging and developing NEC MIPS-based designs. Target connections include simulators, ROM monitors (PMON), OCD/JTAG connections, and logic analysis solutions to provide a complete range of debugging capabilities.

SingleStep also features advanced RTOS-/kernel-aware debug capabilities. These features allow you to debug applications in the context of your RTOS or kernel.

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StethoScope

Real-Time Graphics Monitoring, Performance Analysis, and Data Collection Tool for Tornado™ and VxWorks®

Salient Features

▶ Monitor or modify program variables from the GUI, even while program is running

▶ Display live time histories and X vs. Y plots

▶ Collect and store data for further analysis

▶ Monitor variables in any running process with minimal intrusion

▶ Print plots, save data to file, or export data to analysis tools such as MATLAB

▶ Find noisy signals, glitches in signals

▶ Collect data at high frame rates

Product Overview

Part of Wind River's powerful suite of WindPower™ Tools, StethoScope is a real-time graphical monitoring, performance analysis, and data collection tool. It lets application developers dynamically examine and analyze real-time applications as they run on a target system. StethoScope's powerful multiwindow environment enables developers to choose any program variables interactively, and watch them change in real time.

Designed to run in Tornado and VxWorks host-target cross-development environments, StethoScope consists of two distinct modules: a Motif graphical user interface that runs on the host workstation, and a real-time signal manager that runs on the target system. The real-time code collects and buffers time histories of any variables in the application or the underlying kernel. Variables to be collected can be easily specified, even while the program is running. A low-priority process transfers data from the buffer to StethoScope. This design permits on-line viewing while imposing minimal intrusion on the application.

StethoScope's full-color graphical display allows the application developer to open multiple windows simultaneously and plot an independent set of signals in each. Signals can be selected with a click of a mouse and plotted in both time history and "X vs. Y" formats. Data of particular interest can be captured with StethoScope's powerful triggering modes, using any desired signal as the trigger. Data can be collected before the trigger event with pre-triggering, after the event with delayed triggering, or directly with user-code triggering. All collection and triggering parameters can be set and dynamically changed.

WindRiver®
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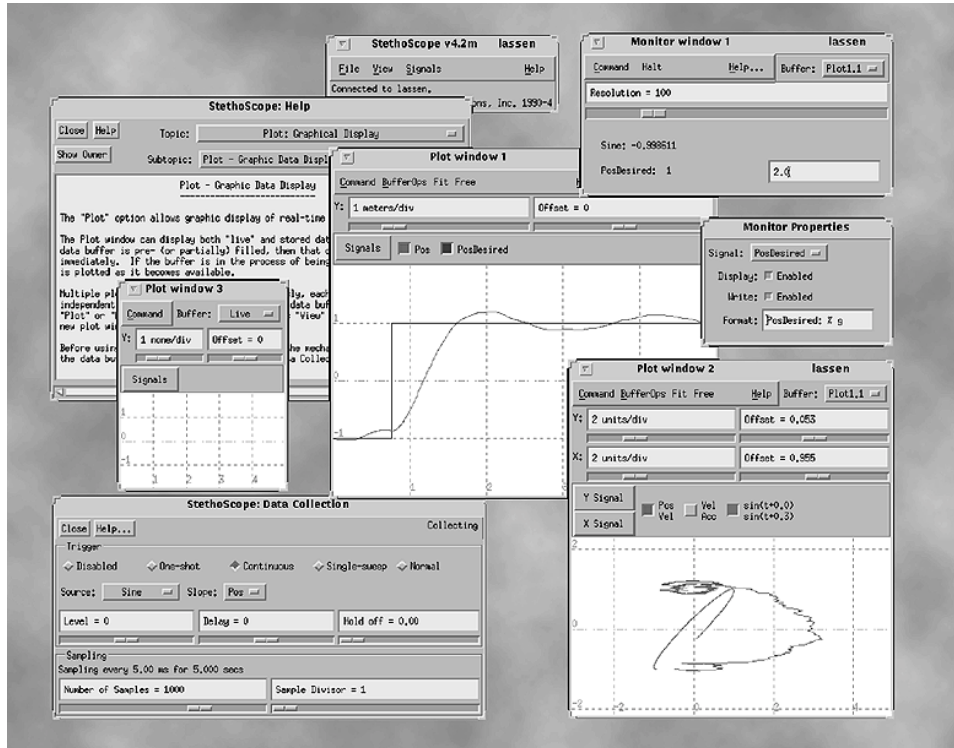
Developers can install StethoScope directly into the Tornado file tree structure and can connect to targets through the target server, thus allowing access to deeply embedded targets that do not have networking support. Also, the RTILib tool and utility package contains a new utility to provide target server access. It allows the target to access the symbol table and load objects, even when the target-resident symbol table option is not used.

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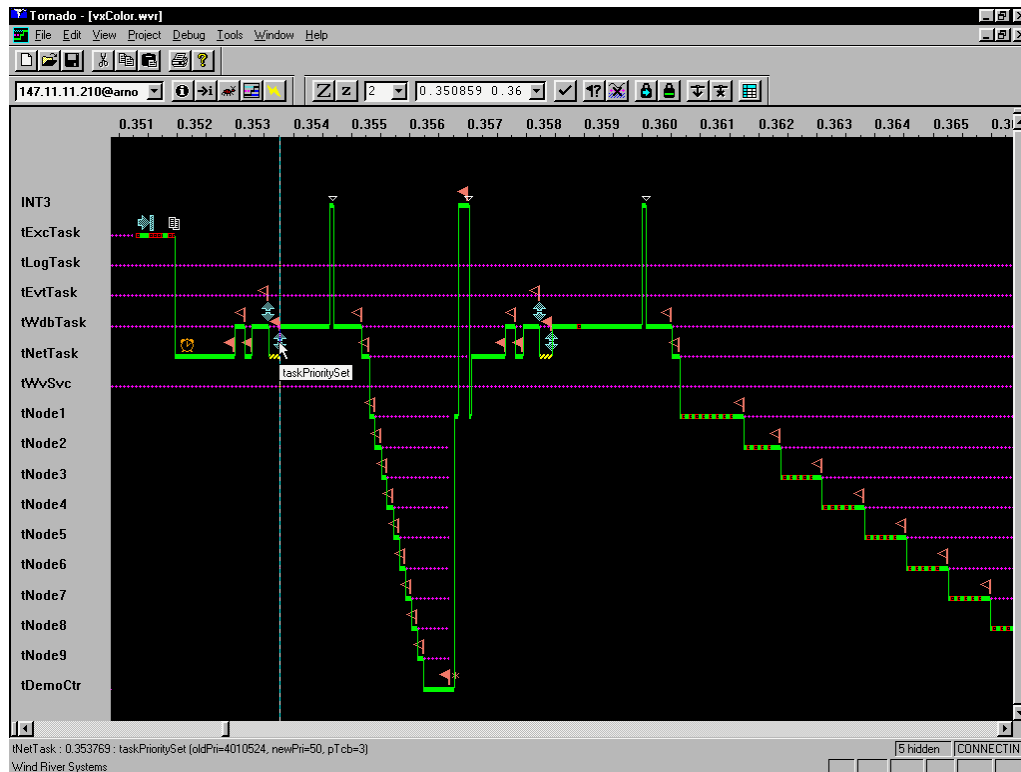# WindView™ System Visualizer for Embedded Software

Product Overview

WindView is a revolutionary diagnostic and analysis tool that provides detailed visibility into the dynamic operation of an embedded system. Using it, the user can quickly and easily visualize the complicated interaction among tasks, interrupt service routines, and system objects in an application. This information is presented and can be manipulated through a state-of-the-art graphical user interface (GUI).

WindView gives developers the unprecedented ability to examine the full history of the system, rather than just a snapshot in time. In addition, it allows the interaction of complex event data to be easily analyzed—locating problems in minutes that might otherwise have taken weeks or months to diagnose.

The background of the WindView display traces the execution thread as the operating system switches between tasks. As the event stream unfolds, icons representing other system events, such as blocking and unblocking on semaphores and message queues, interrupts, timer expirations, and so on, are overlaid on this trace. Detailed information on each event is available simply by clicking on the corresponding icon and dragging it into an event inspection window.

In WindView, the VxWorks® real-time operating system is instrumented to log events of interest. Because each event is marked with a precise high-resolution time stamp, the user can see exactly when the event happened as well as the elapsed time between events. These logging and time-stamping activities are highly optimized and operate with minimal intrusion on the system and application software. The instrumentation can be selectively enabled and disabled at run time, and the user can choose when to upload data to the host.

WindView is one of Wind River's WindPower™ Tools, which provide a quantum leap in developer productivity by addressing critical issues such as system visibility, information presentation and access, interactive and incremental development, scalability, and portability.

Salient Features

▶ Complex event triggering

▶ Reveals race conditions, deadlocks, and other problems relating to task interaction

▶ Instrumented kernel captures context switches, semaphore gives and takes, message queue sends and receives, interrupts, etc. with high-resolution time stamp

▶ Minimal intrusion on system and application performance

▶ User-defined event-logging capability using "event points"

▶ Postmortem mode for catastrophic failure analysis

▶ Large amounts of information easily handled through the sophisticated GUI

▶ C++ and Tcl APIs on event log

CPUs Supported

NEC VR43xx, VR4400, VR5000, VR5432

Host Platforms

Sun and HP workstations and Windows 95/NT

WindRiver®
S Y S T E M S

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Real-Time Operating Systems

Nucleus PLUS Real-Time Operating System

Salient Features

◗ No royalties

◗ Scalable: 4 KB–45 KB, depending on necessary functionality

◗ C source code provided

◗ 95% written in ANSI C

◗ Deterministic, low interrupt latencies

◗ Extensible: make new services by combining existing services

◗ Configurable: easily exclude services not used

◗ Dynamic creation of all Nucleus PLUS tasks

◗ Intertask communication: mailboxes, variable queues, pipes, task synchronization, counting semaphores, events, UNIX-like signals

◗ One-shot and multiple-shot timers

◗ Memory management: fixed partitions, variable length (malloc)

◗ Place any Nucleus PLUS component in any area of memory

◗ Advanced Interrupt Management Mechanism (AIMM)

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Product Overview

Real-time services that are available in the basic Nucleus PLUS product are more full-featured and capable than virtually any real-time kernel on the market today. Accelerated Technology performed an evaluation of the most prominent real-time kernels currently on the market. From this analysis, Nucleus PLUS was developed. Nucleus PLUS has been developed with a "micro-kernel" structure in mind. That is, the essential services of the real-time, embedded environment are provided in such a way that additional operating-system-oriented features can be easily added.

Nucleus PLUS is a real-time, preemptive, multitasking kernel designed for time-critical embedded applications. Approximately 95% of Nucleus PLUS is extremely portable and is currently available for use with most microprocessor families.

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Nucleus PC+ Prototyping Environment for Use with Windows 3.1/95

Salient Features

◗ Interface identical to Nucleus PLUS

◗ Test software using PC software tools (Borland C/C++ and Microsoft C/C++)

◗ Recompile with Intel i960-Dependent files for target system

◗ Use DOS services for I/O

◗ Executes as a native Windows 3.1 or Windows 95 application

◗ Flexible frame mechanism

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Product Overview

Nucleus PC+ is the version of Accelerated Technology's Nucleus PLUS kernel that can be used in an MS-DOS environment. This environment is ideal for embedded applications requiring the responsiveness of multitasking while taking advantage of low-cost PC hardware. Further, all of your C code can be developed in the friendly PC environment.

Development Tools

The real mode version of Nucleus PC+ has been prepared for use with the Borland and Microsoft C compilers and assemblers. Accelerated Technology provides libraries that can be linked with your application to build a Nucleus PLUS-based application that is an MS-DOS executable. A special version of Borland's Turbo debugger that has been enhanced with Nucleus PLUS awareness has been developed by Paradigm Systems. This product, Paradigm DEBUG, is ideal for debugging Nucleus PC+ applications that have been developed with either the Borland or Microsoft compilers.

For programs exceeding the 640 KB boundary or those requiring the advantage of a 4 GB address space, the protected mode version of Nucleus PC+ can be used. It's been prepared for use with the MetaWare High C and Watcom C compilers in combination with the PharLap DOS Extender and the PharLap, Turbo, or Microsoft assemblers.

Interrupt Management

Nucleus PC+ provides access to the PC's interrupt structure, allowing you to invoke a task thread from an interrupt. By doing this, executing threads can be preempted by an interrupt service routine. Nucleus PC+ also permits the processing of interrupts without kernel involvement. In this case, you perform the necessary register saving and restoring, or you can employ the INTERRUPT pragma.

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INCORPORATED

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Nucleus C++ Object-Oriented Real-Time Software

Product Overview

The power of C++ comes from its support for new ways of programming and thinking about programming problems. We at Accelerated Technology view this as being a significant breakthrough for the embedded industry. With C++, you can develop applications quickly by reusing components and efficiently designing applications using an object-oriented approach.

Nucleus C++ brings true object-oriented development to real-time systems. Objects can be statically or dynamically declared, while the creation and deletion of services become transparent to the user. Tasks, Task Communication, Task Synchronization, Timers, Memory Management, Interrupt Management, and I/O Drivers are all accessible as objects.

Service calls are handled as member functions specifically targeted to the object in question (e.g., task, queue, etc.). All Nucleus PLUS parameters use the data abstraction features of C++ automatically. Nucleus C++ Memory and Partition Pool objects allow an easy alternative to memory-sharing methods. Default parameters and typed objects, which simplify the application development cycle, make programming easier for C++ users.

Salient Features

◗ Object-oriented version of Nucleus PLUS

◗ Object-oriented approach to programming

◗ Objects can be statically or dynamically declared

◗ Service calls are handled as member functions

◗ Easy alternative to memory-sharing methods

◗ Full support for new and free operators

◗ Available for any C++ compiler

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

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Nucleus
REAL-TIME SOFTWARE
By Accelerated Technology, Inc.

Nucleus NET TCP/IP Protocol Stack for Use with Nucleus PLUS

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Product Overview

Nucleus NET is a set of networking protocols that provide interoperability between Nucleus PLUS-based systems and other TCP/IP- or UDP/IP-based systems.

A socket interface is provided to maintain a programming environment similar to that of the UNIX socket programming model.

Nucleus NET provides a well-defined driver interface for user-supplied drivers, and can support various MAC-layer drivers. There is less wasted memory space, due to a more efficient packet buffering scheme. Support is available for raw IP, IP forwarding, IP reassembly, IP fragmentation, and IP multicasting and IGMP and DHCP services. Network-centric applications such as routers, switches, and bridges are also supported. Nucleus NET is also the foundation for Accelerated Technology's latest Web-related products, including Nucleus WebServ.

As with all Accelerated Technology (ATI) products, Nucleus NET is delivered in source code form and no royalties are charged for the inclusion of binary copies in a single product line. Nucleus NET is also provided with six months of free technical support, which includes phone, fax, e-mail, and new releases. For more information, contact Accelerated Technology today.

Salient Features

◗ TCP/IP protocol stack

◗ Protocols supported: TCP, UDP, IP, BOOTP, IGMP, ICMP, ARP, RARP, DNS, DHCP

◗ Optional protocols: RIP/RIPII, PPP, POP3, and SMTP

◗ Socketlike user interface

◗ Full integration with Nucleus PLUS for optimal performance

◗ Blocking and nonblocking services supported

◗ Standard interface to physical layer devices

◗ Send/receive ping requests

◗ Compact and scalable

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Nucleus
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By Accelerated Technology, Inc.

Nucleus VNET Virtual Networking Support for Nucleus PLUS

Salient Features

◗ Supports virtual networking between multiple Nucleus PLUS-based TCP/IP, WinSock, and remote node applications

◗ Hosted on Windows NT or remote nodes on network

◗ Access to full Visual C++ features

◗ Depends on Nucleus MNT and Nucleus NET

◗ Can build and test multiple TCP/IP applications on same target

◗ Two levels of device driver support

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

PC

Product Overview

TCP/IP services are provided for Windows NT in the Nucleus MNT environment through a virtual networking facility. Nucleus VNET is a version of Nucleus NET that has been ported to the Windows NT environment.

Nucleus VNET allows Nucleus MNT processes to communicate with each other via a shared memory area. That means multiple versions of Nucleus MNT can be executed on an NT machine, each with its own IP address. Developers who use this technology have the ability to simulate a network on an NT machine. The same shared memory area can be used to communicate with Windows NT applications via a virtual NDIS driver and nodes on the physical network using Windows NT routing facilities.

Initialization

Nucleus VNET's virtual NDIS driver, which is responsible for allocating the global memory area, is started when the NT workstation is booted. The VNET driver is then started manually by the user. This driver must be started after the NDIS driver because it depends on the NDIS to allocate and initialize the common memory. After both drivers have been started, one or more Nucleus MNT/Nucleus VNET applications can be executed.

Communication

Nucleus VNET applications communicate with the VNET driver via NT's device I/O control call. Because Nucleus VNET requires Windows NT device drivers, it will execute only on a Windows NT workstation. Nucleus MNT will execute on either a Windows NT or Windows 95 workstation.

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Nucleus
REAL-TIME SOFTWARE
By Accelerated Technology, Inc.

AlgRTX
POSIX Threads Microkernel

or provide quite such good support. You also benefit from integration with our GNU-based toolkit and excellent reference boards.

CPUs Supported

All NEC VR Series processors

Product Overview

AlgRTX is a multithreading run-time system for any MIPS RISC target, available as an extension to Algorithmics' SDE-MIPS compiler toolkit.

The POSIX "Threads" standard (IEEE standard 1003.1c) represents a brave attempt to write a generic API for multitasking applications, and presents an opportunity for customers who don't want to buy into a complete operating system to achieve a useful measure of code portability.

AlgRTX is not a substitute for a full-blown real-time OS—if you need task/task protection, virtual memory, or a third-party software market, you should look elsewhere. But if you considered a do-it-yourself scheduler and other RTOS vendors want you to buy more than suits you, AlgRTX provides a good working multithreading implementation optimized to the MIPS architecture.

AlgRTX Features

- Example-based kit: We provide a number of working mini-applications with complete source code you can build out of the box. These provide a model for "makefiles" and software building, worked examples of the use of the threads and interrupt API, and a set of basic tests for a new board support package.
- Low-pain interrupts: Interrupts may be handled with a natural extension to POSIX "conditions," avoiding all assembly-level programming and insulating your application completely from the MIPS architecture.
- Toolkit integration: AlgRTX has grown up with SDE-MIPS, and builds on its unequalled GNU C compiler. Host/target communications can be via Ethernet or serial port; the debugger is threads-aware.
- SDE-MIPS libraries are either truly reentrant or protected by semaphore calls, so there is no trouble with multiple threads using the libraries
- Reference platform integration: Working AlgRTX implementations are available with Algorithmics' P-5064 and P-4032 reference platforms; between them, these allow you to prototype with a very wide range of MIPS CPUs, including: NEC VR43x0, VR54xx, and VR5000.

Salient Features

- POSIX for portability: this is not the only OS component you'll ever need, so adherence to a widely respected API protects your software investment. With AlgRTX you need write no assembler code at all, and your application will be highly architecture independent.

- Good quality scheduler: OS theory and practice have come quite a long way in the last few years, leaving many older systems trapped in a dilemma between compatibility and modernization. With no history to carry, AlgRTX can offer a well-mannered modern scheduler with features like priority inheritance.

- No per-target or per-project royalties: your one-time payment gets you source code and an unfettered right to redeploy it—no per-project licenses

- Supportable and maintainable: AlgRTX source code is clean and well-written, and you are welcome to support it yourself. But we want to make money on support and upgrade services, and to do that we'll provide the same standard of support as we do for SDE-MIPS.

- From a MIPS specialist: Algorithmics know MIPS like nobody else. Multiplatform OS specialists can't equal our in-depth knowledge,

algorithmics

- You're welcome to download information (including manuals) for these boards; you'll find them very fully equipped and very fast. Since the platforms and software are designed in the same room, we can offer the best possible support.

Drivers and BSPs

The AlgRTX kernel needs a timer and an interrupt controller. Most MIPS CPUs have a suitable interval timer, and have simple building blocks for interrupt functions; but most workable systems will need an external interrupt controller of some kind.

Apart from any interrupt connection, drivers are no more special to the kernel than any other software module—though if you're using POSIX threads you'll probably be looking for a POSIX-style generalized file system interface to drivers. SDE-MIPS kit drivers are suitable, and are typically available for at least serial ports and Ethernet on supported boards.

Creating a basic support package for a new board is equivalent to the process for SDE-MIPS, which is described in its excellent user manual.

Customization

AlgRTX can be extended to your requirements; we'll consider doing that at low cost where we expect to be able to reuse the code.

More about POSIX Threads

The IEEE's "Portable Application Standards Committee" (PASC) look after the 1003.1c "threads" standard. Several good books are available about programming to this interface (though we don't imply that their authors endorse our software!). You may like to look at:

- Kleiman, Shah & Smaalders: Programming With Threads (from Amazon) (published by Prentice-Hall), ISBN 0131723898. This book has been around for a while and has been our guiding light during implementation, but the next two are newer.
- David Butenhof: Programming With Posix Threads (from Amazon) (published Addison-Wesley)
- Lewis & Berg: Multithreaded Programming With Pthreads (from Amazon) (published by Prentice Hall), ISBN 0136807291

AlgRTX vs. other OSs

Here's our summary of how we stand up against some well-known alternatives:

- Windows CE is new, but has immense potential in creating an RTOS backed up by a huge mass of vertical-application software from Microsoft, and a thriving third-party software market. Windows CE is not very real-time, and has a pretty large footprint; but those are big virtues and Algorithmics are signed up as a Systems Integrator.
- Linux is in many ways the ideal OS for applications which are not real-time, but want to build software for a UNIX-like system and take advantage of the biggest pool of high-quality free software
- Tornado/VxWorks from Wind River has extensive tools, a simple run-time system and a fair amount of run-time software. Its big virtue is that the low-level and relatively small runtime does give you genuine portability across different CPU architectures. "Traditional RTOS" vendors do take away some portability headaches—but of course you have to pay them to do that

The closest things to AlgRTX are source-code-supplied RTOSs like Accelerated Technology's Nucleus. The difference here is down to customer preference, and perhaps our MIPS orientation.

More About Algorithmics

Algorithmics, probably the most experienced MIPS technology support group anywhere, was founded in 1988 by a group of MIPS veterans. Our customers include 1996's two biggest MIPS design wins, as well as a host of small companies. In addition to tools we offer evaluation boards, training, contract design and porting, design reviews, and so on.

We are interested in custom projects; call us if your requirements are special.

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ThreadX High-Performance Real-Time Operating System

Product Overview

Express Logic's ThreadX™ provides real-time embedded NEC developers with the most technically advanced multitasking solution on the market today. Its picokernel™ design results in very high performance and extremely small memory requirements—requiring less than 4 KB for minimal usage. ThreadX also provides embedded NEC applications with significant technical innovations, including extremely fast software timers and a mechanism to help reduce context switching called preemption-threshold™.

In addition, ThreadX is completely compatible with many development tools. Express Logic also partners with embedded software component companies to provide embedded solutions for TCP/IP, ATM, Frame Relay, etc.

Express Logic provides many high-quality and royalty-free software solutions for embedded software developers. For more information about Express Logic and its products, please call 888-THREADX or visit the Web site at http://www.expresslogic.com.

Salient Features

- High performance

- Small footprint

- Advanced features and services

- Ease of use

- Quality design and documentation

- Reasonable pricing

- Absolutely NO ROYALTIES!

- Full source code

- Development tool integration

- Partner-oriented customer support

CPUs Supported

NEC VR41xx, VR43xx, VR4400, VR5xxx

Host Platforms

Host independent
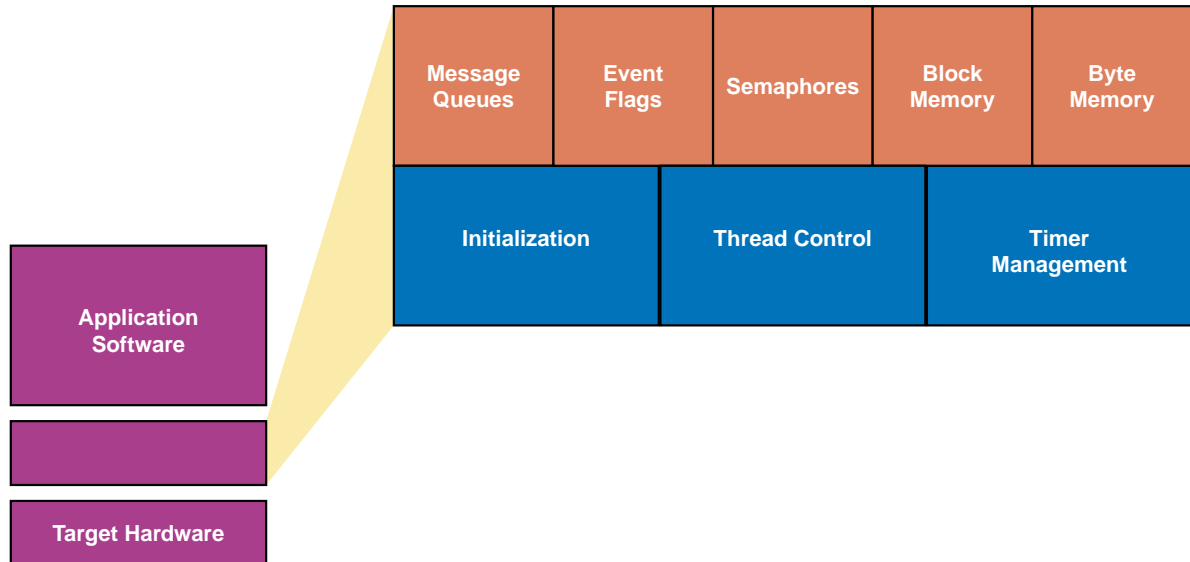

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ThreadX™ Real-Time Operating System

Salient Features

▶ Royalty-free licensing

▶ Fully integrated with Green Hills Software's optimizing compilers and MULTI® 2000 IDE

▶ Per-task and system-wide execution profiling

▶ Comprehensive run-time error checking, including per-task stack overflow

▶ Powerful multitasking and system debugging features

▶ Advanced features: Preemption Threshold™

▶ Small footprint

▶ Fast system services

▶ Source code provided

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Host independent

Product Overview

ThreadX provides real-time MIPS developers with the most technically advanced multitasking solution on the market today. Its picokernel™ design results in very high performance and extremely small memory requirements—requiring less than 3 KB for minimal usage.

ThreadX also provides embedded MIPS applications with significant technical innovations, including extremely fast software timers and a mechanism to help reduce context switching called Preemption Threshold™.

ThreadX is completely compatible with Green Hills Software's optimizing compilers and MULTI® 2000 Integrated Development Environment (IDE) and is available exclusively through Green Hills Software.

ThreadX/MULTI Solution

Green Hills Software's MULTI 2000 Integrated Development Environment (IDE) works seamlessly with the ThreadX embedded real-time kernel and provides detailed, kernel-aware information to developers. MULTI for ThreadX is fully aware of all seven ThreadX kernel components and includes live easy-to-understand summary lists and detailed individual views of all ThreadX component types: threads, message queues, semaphores, event flag groups, memory block pools, memory byte pools, and application timers.

MULTI 2000 for ThreadX is a powerful, finely tuned package designed to dramatically reduce development time for your next embedded project. MULTI 2000 for ThreadX includes: Green Hills™ world-class optimizing C, C++, and embedded C++ compilers; MULTI 2000 IDE, including source-level debugger, program builder, execution profiler, browser, editor, run-time error checker, and version control system; and the high-performance ThreadX real-time kernel.

Green Hills
·S O F T W A R E ,   I N C .·

APPLICATION SOFTWARE

Message queues
Event flags
Semaphores

Block memory
Byte memory

Timer management
Thread control
Initialization

TARGET HARDWARE

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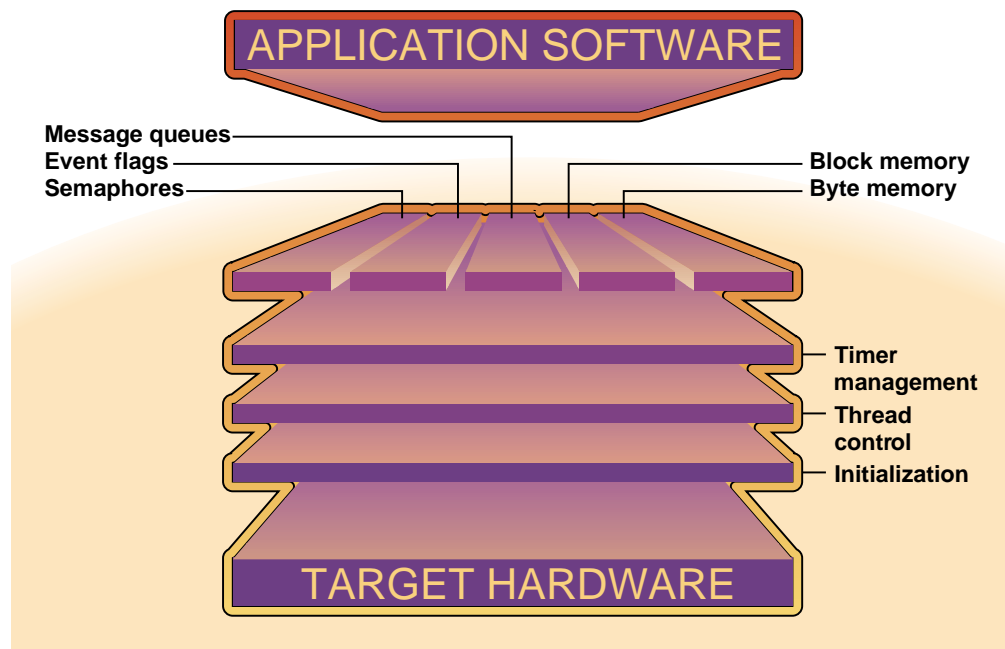
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The Jeode™ Platform

Accelerated Java™Solutions for Internet Appliances and Embedded Devices

J E O D E ™

Salient Features

▶ Full compatibility
- Fully compatible with Sun's PersonalJava™ and EmbeddedJava™ specifications
- A "Sun Authorized Virtual Machine"
- Full featured—includes Java run-time environment and embedded class libraries

▶ Better performance
- Adaptive dynamic compilation for high performance in a small memory footprint
- Averages 6 times the speed of interpreter-only VMs

▶ Highly configurable
- Scalable within system constraints
- RAM usage can be bounded
- Can be tuned for optimal balance between speed, size, and predictability

▶ Designed for constrained memory spaces
- ROM footprint from approximately 250 KB to 2.7 MB
- 2.7 MB is full-featured VM (English language)
- 5.0 MB for full international language support
- Can specify use of system memory to meet application requirements

▶ More predictable
- Precise, concurrent garbage collection, which can be preemptible
- Asynchronous compilation, which can be preemptible

▶ Extensive tools support
- Integrated with CodeWarrior IDE
- Includes JeodeConfigurator to monitor events, analyze memory usage, and tailor the Jeode EVM
- Supports JVMDI and JDWP standard debugging interfaces for third-party tools

CPUs Supported

NEC VR41xx, VR42xx, VR43xx (other CPUs also supported)

RTOSs Supported

Windows CE (other RTOS/CPU combinations are supported)

Product Overview

Implement accelerated, Java-compatible technology in your Windows CE/NEC VR4xxx Internet appliances or embedded devices.

The Jeode platform is Insignia's accelerated implementation of the EmbeddedJava and PersonalJava specifications that is tailored for Internet appliances and embedded devices. It is also the first independently developed implementation to pass Sun's EmbeddedJava technology and PersonalJava platform compatibility tests to earn the distinction of "Sun Authorized Virtual Machine." The Jeode platform provides developers with a full-featured, compatible, and optimized development and run-time environment for implementing Java technology-based applications on consumer and embedded devices.

INSIGNIA
SOLUTIONS ®

At the core of the Jeode platform is the Embedded Virtual Machine™ (EVM™), a Java run-time engine that delivers an optimal balance of performance and predictability in a small memory footprint. Using a proprietary technique called adaptive dynamic compilation, the Jeode EVM can execute Java applications on average six times faster than interpretive VMs can. The Jeode EVM also implements precise, concurrent garbage collection for more predictable behavior.

The Jeode EVM can be configured and tuned in several different ways to assist developers in building a specific implementation of the Jeode EVM that is optimized for a particular embedded device. Developers can specify the maximum system memory, maximum heap size, maximum stack size, and several parameters associated with dynamic compilation.

The Jeode EVM can be highly instrumented to provide helpful diagnostic and debugging insights into the Jeode EVM itself. Developers can observe the application's behavior as it executes, relative to parameters that they selected to configure and build the Jeode EVM. On viewing these results, developers can adjust certain parameters, and configure and test another version of the Jeode EVM.

Service and Support

Insignia Solutions provides the Jeode*Assist* Technical Support Program to users of the Jeode platform. This program includes direct access to Jeode support engineers via e-mail and access to the Jeode*Assist* Web site. This Web site contains current news, documentation, the latest updates, and a problem-reporting facility. This service is provided free of charge during the evaluation period, and is offered as part of the development licensing agreement. Insignia Solutions also provides consulting and porting services to augment a customer's engineering team and reduce the time to market for high-priority projects.

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JAVA™

Sun Authorized
Virtual Machine

C EXECUTIVE and PSX Real-Time Operating System Kernels

Salient Features

▶ Real-time, multitasking kernel optimized for C language embedded applications on the NEC VR Series microprocessors

▶ System calls for task scheduling, time control, task coordination, and C-style I/O

▶ Fast system call mechanism for C programs

▶ ROMable, reentrant portable C library included

▶ Fully prioritized, preemptive and event-driven scheduler

▶ Multiple methods of intertask communication (including events, semaphores, signals, and data queues)

▶ Built-in queuing for variable-length messages, with optional special character alert and/or time-out

▶ PSX adds 140 calls from POSIX, including threads

▶ For use with any development system (such as DOS, Windows, or UNIX)

▶ Optional DOS-compatible file system (CE-DOSFILE™)

▶ Optional TCP/IP communications

▶ Optional SNMP™

▶ Optional system-level debugger (CE-VIEW™)

CPUs Supported

NEC VR43xx, VR4400, VR5000

Future: VR10000

Part Numbers: C EXECUTIVE®/PSX-VR4200/VR43xx, VR4400, VR5000

Host Platforms

Any host such as DOS, Windows, or UNIX with VR Series cross-compiler, assembler, and linker

Product Overview

C EXECUTIVE for the NEC VR Series is a real-time, multitasking kernel specifically designed for embedded microprocessor applications using the C language.

C EXECUTIVE is in wide use in both military and FAA radar systems, PBX, laboratory data acquisition, cardiac monitors, military avionics, process control, laser printer controllers, X-Window terminals, factory automation, PDA, and wireless applications.

C EXECUTIVE has supported the MIPS architecture since 1989 and has been specifically packaged for the NEC VR4300, VR4400, and VR5000.

The VR Series version of C EXECUTIVE provides a field-proven, portable operating system adapted to the high performance MIPS architecture. C EXECUTIVE can be used on any VR Series board. Device drivers and configuration modules are included.
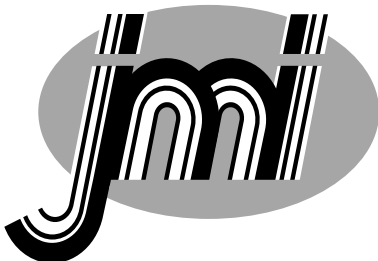
C EXECUTIVE is unique among real-time operating system kernels because of the software technology used in its implementation. These same software methods—including C language, optional UNIX host development, data flow design, and device-independent standard I/O with redirection—have now become popular for the development of real-time applications software. C EXECUTIVE brings these advantages of modern software engineering, long available with UNIX on minicomputers, down to a board-level kernel.

C EXECUTIVE was designed from its inception for C language multitasking embedded systems. A system call is simply a direct C function call. Sixty-two system calls—for example, open, close, read, write, exit, and select—provide a subset of UNIX calls. Other kernels make their systems callable from C programs by providing run-time "hooks" and interface libraries, thereby adding permanent additional execution overhead.

C EXECUTIVE has an optional DOS-compatible file system, CE-DOSFILE, which provides a standard medium for data interchange between any of NEC's RISC microcontrollers and standard PCs. CE-TCP™ is an optional TCP/IP networking package for those applications requiring communications facilities.

PSX extends the C EXECUTIVE system call library by adding 140 POSIX.1 system calls, providing a single-user, single-group, but multiprocess execution environment.

Training

A standard training course is available that not only teaches fundamentals of system calls, system configuration, and device driver design, but also reviews concepts of data flow design and the use of portable C to implement structured programming constructs. The last one to three days of the course include a design seminar that helps the customer produce a formal data flow design of the application, and map the design into C EXECUTIVE system calls and configuration tables. In fact, some customers have actually produced simple running prototypes of their applications by the end of the course.

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Windows CE Operating System

Salient Features

- Compact, highly efficient modular operating system

- Built-in support for communications, the Windows® CE shell, and device drivers

- Subset of Win32® API set and familiar development model and tools

- Allows OEMs to adapt Windows CE to their hardware

- Includes a set of small drivers for interrupt services, RTC, etc.

- Advanced features for connection to Windows and the Web

CPUs Supported

NEC VR41xx, VR43xx

Product Overview

Microsoft® Windows CE is a compact, highly efficient, modular operating system designed for a wide range of embedded systems, such as industrial controllers, kiosks, data terminals, set-top boxes, and handheld computers. Since Windows CE supports a large subset of the Win32 API, you can use your existing Windows programming skills or come up to speed quickly by taking advantage of the numerous books and training courses on Win32 and developing with Windows CE. Then use that knowledge to develop applications for a whole new category of connected devices.

The Microsoft Internet Explorer for Windows CE class browser control enables you to develop full-featured branded browsers for your Windows CE-based devices

You can use tables, cascading style sheets, JavaScript, DHTML, JPEG, and animated GIF and WAV files to create full-featured browsers for your device.

The updated desktop applications for Windows CE make your devices more appealing to your customers

You can easily integrate the Pocket versions of Word and Microsoft Internet Explorer, along with Inbox and Handheld PC Pro-style shells into your devices. With Pocket Word, you can create documents on your Windows CE-based device that are equivalent to their desktop counterparts. With Internet Explorer for Windows CE, you can surf the Web, save favorite sites, and view local HTML files. With Inbox you can create, send, receive, and reply to e-mails from your devices. And with the Handheld PC Pro-style shell, you can provide the familiar Windows 9X-style user interface, including a start button, TaskBar, desktop icons, and the Recycle Bin.

Windows CE supports a large range of communication options and application program interfaces

You can now create connected devices with the communications component in Windows CE. This component provides support for the following communications hardware and data protocols: Serial I/O support, Remote Access Service (RAS), Transmission Control Protocol/Internet Protocol (TCP/IP), Network Directory Interface Specification (NDIS) for Local Area Network (LAN), Telephony API (TAPI), Wireless Services for Windows CE.

Microsoft® Windows® CE

Cryptography tools in Windows CE enable you to digitally sign files and prevent unsigned applications from loading

With the Cryptography Service Provider developer kit, you can create your own cryptography service providers, and add extra protection to your data using custom cryptographic algorithms.

The Dial-Up Bootloader allows you to dynamically update your OS image over the Network

The Dial-Up Bootloader makes upgrading for bug fixes or new services very easy for remotely installed devices.

Windows CE is portable to a wide range of today's most popular processors

For the latest list of supported processors, or for the latest Windows CE product updates and technical information, visit:

http://www.microsoft.com/windowsce/embedded

Contact List

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QNX®
Real-Time OS

Salient Features

◗ Scalable microkernel architecture: Use one OS and one API for everything from handheld appliances to high-end SMP clusters

◗ Provides full memory protection for all drivers, applications, and OS components

◗ Recovers from software faults—even in drivers and other system services—without rebooting

◗ Supports hot-swapping for drivers and OS modules

◗ Most drivers are source-code identical across processor platforms

◗ Fits POSIX RTOS plus full-featured GUI into less than 1 MB of ROM

◗ Connects seamlessly to Windows desktops (control Windows from QNX, or QNX from Windows)

◗ Supports multiple file systems—embedded, POSIX, CIFS, CD ROM—simultaneously

◗ Full Internet technology suite (including embedded browser, e-mail client, and Web server)

CPUs Supported

VR41xx, VR43xx, VR5xxx

Host Platforms Supported

Windows NT, Windows 95/98, QNX 4

## Microkernel Architecture for Massive Scalability

QNX's microkernel architecture offers unprecedented scalability. Link your application code directly against the kernel to create a single multithreaded image for small embedded systems—as you would with a real-time executive. Or run the QNX Process Manager for all the advantages of a full process model and the ability to add thousands of applications—all running in MMU-protected memory.

Or take QNX to the extreme and run your applications over a distributed network of SMP clusters for the ultimate in large-scale configurations! Whatever your configuration—tiny, medium, massive, or distributed—recoding is never an issue since the QNX API remains consistent throughout.

Superior Memory Protection

Conventional operating systems use a single flat memory architecture in which hard-to-detect programming errors like corrupt C pointers can cause programs to overwrite each other (bad) or the kernel (worse). The inevitable result: system failure. A QNX-based system, however, can intelligently recover from software faults, even in drivers and other critical programs—without rebooting—because every OS component runs in its own MMU-protected address space.

QNX's full MMU support also simplifies testing because it identifies which module tried to perform an invalid memory access—at the exact instruction. What can often take weeks or months to identify in a conventional RTOS takes virtually no time with QNX.
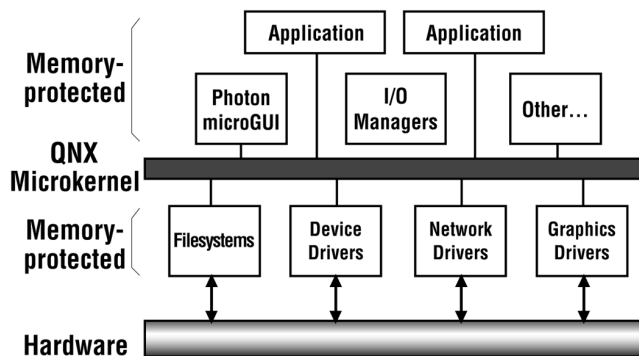
QNX provides memory protection for all applications, OS components, and drivers.

Portable POSIX APIs

QNX is the world's first microkernel with a POSIX personality. Unlike real-time executives and OS implementations that have proprietary APIs, QNX is engineered from the ground up for the latest POSIX 1003.1 standards and drafts, including real-time and thread options.

QNX's POSIX implementation means portability—not only of your application code, but also of your software developers. In fact, programmers familiar with UNIX won't need any training to feel right at home in this POSIX environment.

What's more, this built-in POSIX compatibility comes without the penalty of extra code. Even after the Process Manager is added to include services like process creation, pathname-space management, and memory protection, a QNX-based system is extremely small and efficient—crucial for ROMable systems.

Minimize Hardware Costs

Unlike some OSs that try to squeeze monolithic designs or bulky windowing systems into embedded environments, QNX was designed from the ground up to reduce the cost and component count of your products.

For example, QNX supports execute-in-place (XIP), which allows applications to run directly out of ROM or flash. And, since its system image is actually a simple read-only file system, it allows applications to start without a separate file system manager or command interpreter.

Integrated Development Environment

QNX development is supported under the award-winning CodeWarrior Integrated Development Environment (IDE) Command-line GNU-compatible tools are also available.

Dynamically Loadable Functionality

No other real-time OS scales so easily—just plug in the modules or drivers you need. Like other operating systems, QNX supports shared objects (also known as DLLs). But unlike other operating systems, QNX lets you add or remove entirely new OS functionality (via software modules) on the fly without rebooting your system.

Embeddable Photon microGUI®

Running in an extremely small memory footprint, Photon offers a highly functional windowing system that connects seamlessly to QNX's message-passing architecture.

Photon also gives you exceptional connectivity between windowing systems. With Photon's remote user interface (RUI) technology you can view—and control—the GUI of a QNX embedded system from a window on a Windows NT/95/98 or UNIX desktop. RUIs are baud rate aware and can run across a serial or network link. For embedded systems, this can give you a graphical interface into your consoleless black box.

With the optional Citrix ICA client for Photon, reverse connectivity is also available: Run a Windows NT/95/98 session from within a window on the Photon desktop.

Embeddable Web Server

With our tiny TCP/IP manager and embedded Web server, you can control your embedded device—be it a printer, photocopier, router, or PLC—from any Web browser. Retrieve statistics, configure system parameters, or troubleshoot problems without leaving your desktop PC.

Platform-Independent Device Drivers

From the beginning, drivers for QNX were designed to be source-code identical across CPUs and boards. In fact, the same binaries for a CPU can run on different boards—no more BSP nightmares.

To reduce the time required to write your own device drivers, QNX provides a resource manager framework and C functions that handle the default behaviors common to most devices; all you need to worry about are the low-level details specific to your device.

And because each QNX driver runs as a standard process (rather than as part of the kernel itself), you can test changes in driver code without going through the time-consuming task of rebuilding the kernel. Simply recompile and restart the driver.

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SuperTask!
Multitasking RTOS
Development Suite

Salient Features

◗ ANSI C source code included

◗ No royalties

◗ Over 70 powerful system calls

◗ Supports over 16 target processor families

◗ Task-aware plug-ins (DLLs) are available

◗ Benchmarks are available from our
  HYPERLINK "mailto:sales@ussw.com" sales
  department

◗ USNET, NetPeer, and USFiles are fully
  compatible to provide seamless solutions

CPUs Supported

NEC VR43xx, VR44xx

Host Platforms

DOS and UNIX

Product Overview

SuperTask! is a suite of development tools intended to aid in
the creation of multitasking embedded applications. At
SuperTask!'s core is MultiTask!, US Software's real-time
operating system kernel. MultiTask! provides over 70 system
calls to control various tasks inside an application. OPUS
Make! is a make utility program to build MultiTask!

Get complete source code with ANSI C stream I/O, including
sprintf, sscanf, and pipes. Stream I/O can be enhanced to
support MS-DOS files by using HYPERLINK
products/USFiles. With MultiTask! you perform serial I/O
operations on your target processor using the standard ANSI
interface. MultiTask! is available for over 16 target processor
families and is specifically designed to have a low interrupt
latency.

US Software also offers TronTask! TronTask! is a real-time
operating system implementing the ITRON real-time kernel
specification designed for consumer products and other small-
scale embedded systems where memory constraints and
performance are critical. TronTask! is both ITRON 2.01 and
3.02 compliant and supports multiple 16-and 32-bit
embedded processors.

U S SOFTWARE®
EMBEDDED EXCELLENCE

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Arriba!
Embedded Edition

Emulators: HP and Macraigor Systems

RTOSs: ThreadX, pSOSystems, Embedix, and other in-house RTOSs (via SDK)

Product Overview

Over the last several years, the growth in size and complexity of embedded applications has presented embedded developers with new challenges. Emerging RTOSs, System-On-Chip (SOC), multicore designs, mixed-language applications, and the diversity of new and existing processors make it increasingly difficult for traditional tool vendors to provide a consistent and comprehensive tool solution.

By recognizing that good software isn't simply about the features of today, but about the ability to adapt to the changing needs of tomorrow, Viosoft took great care to ensure that the design of Arriba! is future-proof. Unlike other development tools that are constructed from a single monolithic core, Arriba! is designed as a collection of well-defined, collaborating components that communicate over a CORBA framework. The flexibility of this architecture empowers Arriba! to easily and quickly extend support of future processors, RTOSs, and target platforms.

With each customized version of Arriba!, Viosoft works with IP, processor, compiler, and RTOS vendors to ensure maximum compatibility and the highest degree of quality.

Salient Features

❱ Complete integration with target hardware and instruction set simulator (ISS)

❱ Support for hardware-assisted debug probe (JTAG) and software-resident monitor (pROBE, pMON)

❱ Supports various flavors of GNU, Algorithmics, Diab Data and Apogee compilers

❱ RTOS awareness debugging and monitoring

❱ Full integration with GNU-make and CVS via Arriba! plug-ins

Compatibility

Host Platforms: Linux, Solaris, and Windows 95/98/NT. Ports to other UNIX platforms available upon request.

Host Processors: x86

Target Platforms: Intel, NEC, DENSAN, Toshiba, LSI Logic, and Algorithmics development boards. Also available with cycle accurate/approximate processor simulators (ISS and monitors).

Target Processors: MIPS, ARM, StrongARM, PowerPC, SmartJ/TinyJ (ST-22), and x86

IDE Features

• **Integrated Edit-Compile-Run** functionality constructed within a single, uniform windows-desktop environment… all at the convenience of a few mouse clicks

• **Flexible and Portable Project Management** with "smart recompile" and Makefile export

• **Optional Integration with CVS** supports visual check in/out and diff/merge capabilities from a unified desktop (through Arriba! plug-ins).

• **Syntax-Highlighted Edito**r with built-in parser, class/method viewer, and optional VI/EMACS emulation

• **Optional Code Profiler** quickly finds hot spots and memory leaks in code (through Arriba! plug-ins).

V I O S O F T

Debugger Features

- **Consistent User Interface:** Native and remote debugging
- **Remote Debugging**: Serial, Ethernet, or Hardware-assisted debug probes (JTAG/BDM) or Instruction Set Simulators (ISS).
- **Mixed-Language Debugging:** C/C++ and Java
- **RTOS Kernel Awareness:** Support for kernel-level debugging, including device drivers and interrupt handler code (via emulators)

Target Monitor (VMON)

- **Full Integration with RTOS:** Allows VMON to coexist and debug the Linux kernel, even when the Linux kernel exception handlers are in place.
- **Fast/Reliable Remote Debug:** Dedicated Ethernet connection to target. (Download time for typical kernel images of 1–2 MB is less than 20 second.)
- **ROM:** Designed to operate as a stand-alone debug/boot monitor or as a component that can be incorporated into a custom application ROM or flash memory.
- **Low Footprint:** VMON requires a very small amount of the processor's DRAM to operate, making it attractive to low-footprint applications.
- **Extensible:** VMON can be updated dynamically at runtime to incorporate Linux kernel awareness features. This ability increases visibility without the expense of a larger kernel footprint at deployment.

The Arriba! IDE build environment

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Internet: http://www.viosoft.com

Arriba! Linux Kernel Edition

Salient Features

▶ An integrated, graphical environment for configuring, integrating, and building the Linux kernel

▶ Device driver wizard with automatic code generator for Linux kernel

▶ Full source-level symbolic debugger

▶ Prebuilt kernel root file system ("user land")

Compatibility

Host Platforms: Linux, Solaris, and Windows 95/98/NT. Ports to other UNIX platforms available upon request.

Target Processors: MIPS, ARM, StrongARM, PowerPC, and x86

Target Platforms: Intel, NEC, DENSAN, Toshiba, LSI Logic and Algorithmics development boards. Also available with cycle accurate/approximate processor simulators (ISS and monitors).

Product Overview

Over the last several years, Linux has begun to emerge as the *alternative* OS of choice. Speed, reliability, footprint, and accessibility are some of Linux is desirable attributes that

appeal not only to desktop users, but also to embedded developers. Yet, developing applications for Linux is a challenging affair for those who don't speak *VI, Emacs*, and *Makefile*. Clearly, Linux development tools still lag behind those of the other OSs.

Viosoft believes that better tools are super-critical to the future success of the Linux movement. Higher quality performance and quicker development cycles from better tools are an incentive for programmers to migrate toward Linux platforms.

Enter Arriba!, a powerful IDE specifically customized to meet the needs of in-depth Linux application development.

By recognizing that good software isn't simply about the features of today, but about the ability to adapt to the changing needs of tomorrow, Viosoft took great care to ensure that the design of Arriba! is future-proof. Unlike other development tools that are constructed from a single monolithic core, Arriba! is designed as a collection of well-defined, collaborating components that communicate over a CORBA framework. The flexibility of this architecture empowers Arriba! to easily and quickly extend support of future processors and target platforms.

Viosoft's target agent monitor, VMON, is a prime example of the flexibility of Arriba! Although it is Linux kernel aware, it doesn't hardcode such knowledge within its program space, making it fully compatible with future kernel releases.

Along with the Kernel Developer Edition, Viosoft works with IP and processor vendors to provide ports of Linux for several popular embedded processors, including MIPS, ARM/StrongARM, PPC, and X86. In doing so, we reach a level of integration between the OS and the tools that result in the highest degree of visibility into the kernel.

IDE Features

• **Integrated Edit-Compile-Run** functionality constructed within a single, uniform windows-desktop environment… all at the convenience of a few mouse clicks

• **Flexible and Portable Project Managemen**t with "smart recompile" and Makefile export

• **Optional Integration with CVS** supports visual check in/out and diff/merge capabilities from a unified desktop (through Arriba! plug-ins).

• **Syntax-Highlighted Editor** with built-in parser, class/method viewer, and optional VI/EMACS emulation

• **Optional Code Profiler** quickly finds hot spots and memory leaks in code (through Arriba! plug-ins).
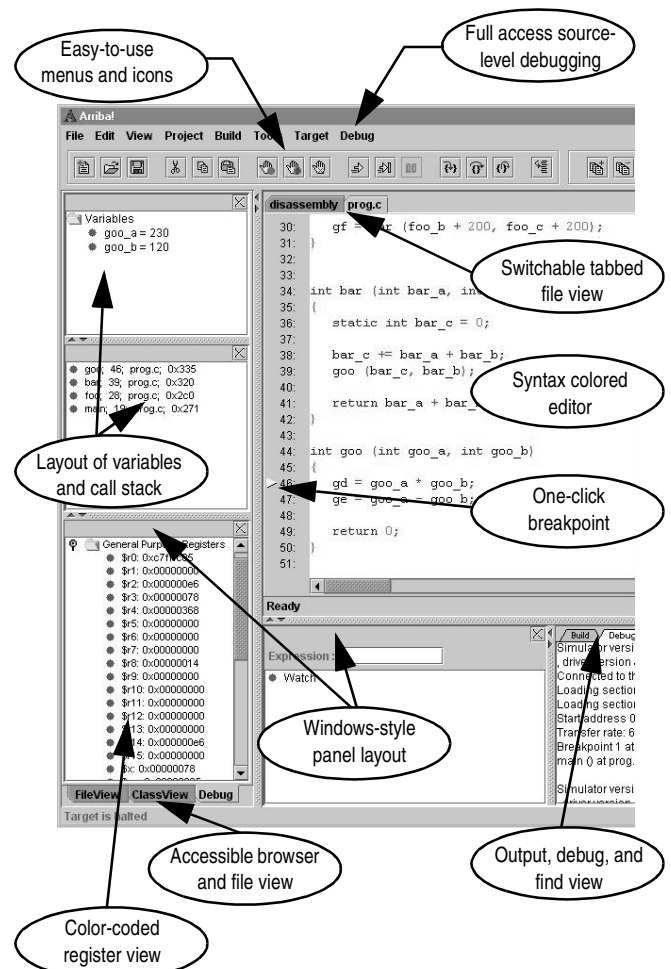
- **Mixed-Language Debugger:** C/C++ and Java (through Arriba! plug-ins)
- **CORBA-based Framework:** Makes it easy for other third parties to integrate and leverage capabilities of Arriba!

Debugger Features

- **Consistent User Interface:** Native and remote debugging
- **Remote Debugging:** Serial, Ethernet, or hardware-assisted debug probes (JTAG/BDM) or Instruction Set Simulators (ISS).
- **Mixed-Language Debugging**: C/C++ and Java
- **Linux Kernel Awareness:** Support for kernel-level debugging, including device drivers and bottom-half kernel code.

Target Monitor (VMON)

- **Full Integration with Linux:** Allows VMON to coexist and debug the Linux kernel, even when the Linux kernel exception handlers are in place.
- **Fast/Reliable Remote Debug**: Dedicated Ethernet connection to target. (Download time for typical kernel images of 1—2 MB is less than 20 seconds.)
- **ROM:** Designed to operate as a stand-alone debug/boot monitor or as a component that can be incorporated into a custom application ROM or flash memory.
- **Low Footprint**: VMON requires a very small amount of the processor's DRAM to operate, making it attractive to low-footprint applications.
- **Extensible**: VMON can be updated dynamically at runtime to incorporate Linux kernel awareness features. This ability increases visibility without the expense of a larger kernel footprint at deployment.

The Arriba! IDE build environment

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Arriba! Linux Native Edition

Salient Features

▶ A full IDE with integrated edit/compile/debug support from a single, unified desktop

▶ Modern graphical user interface (100% pure Java)

▶ Full source-level symbolic debugger

▶ Full integration with GNU tools

Compatibility

Host Platforms: Caldera OpenLinux 2.3 (or above), Debian 2.1 (or above), RedHat 6.x, SUSE 6.x, and TurboLinux 4.0

Host Processors: x86 and PowerPC (SPARC planned for Q2 2000)

Product Overview

Over the last several years, Linux has begun to emerge as the *alternative* OS of choice. Speed, reliability, footprint, and accessibility are some of Linux's desirable attributes that appeal not only to desktop users, but also to embedded developers. Yet, developing applications for Linux is a challenging affair for those who don't speak *VI, Emacs,* and *Makefile*. Clearly, Linux development tools still lag behind those of the other OSs.

Viosoft believes that better tools are super-critical to the future success of the Linux movement. Higher quality performance and quicker development cycles from better tools are an incentive for programmers to migrate toward Linux platforms.

Enter Arriba!, a powerful IDE specifically customized to meet the needs of Linux engineering development.
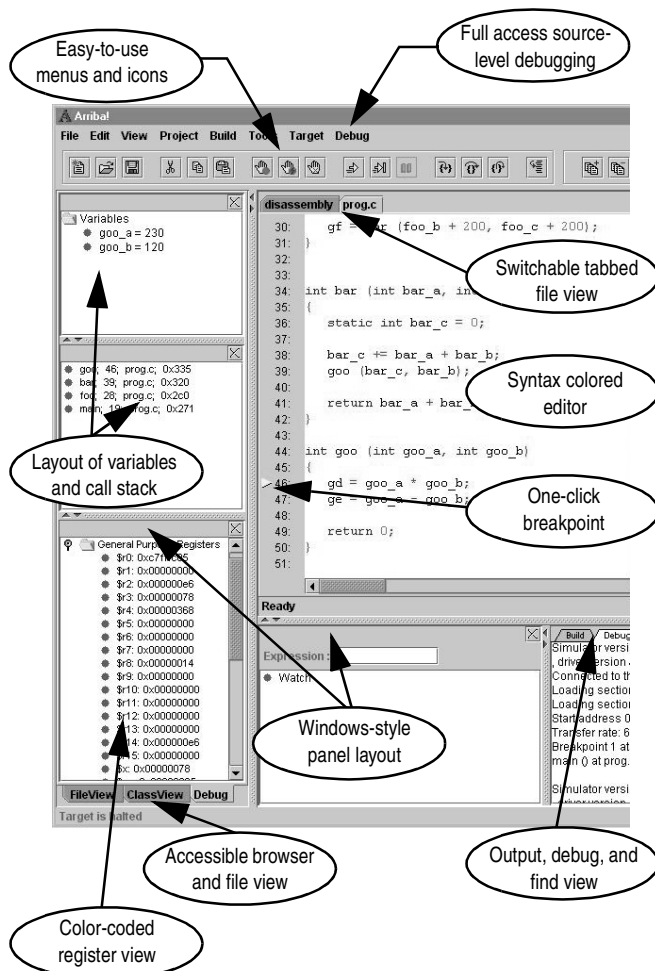
By recognizing that good software isn't simply about the features of today, but about the ability to adapt to the changing needs of tomorrow, Viosoft took great care to ensure that the design of Arriba! is future-proof. Unlike other development tools that are constructed from a single monolithic core, Arriba! is designed as a collection of well-defined, collaborating components that communicate over a CORBA framework. The flexibility of this architecture empowers Arriba! to easily and quickly extend support of new features or versions of Linux.

Because of the open-source nature of Linux, Viosoft continually commits to testing and ensuring that Arriba! runs on many different Linux distributions. This is just one more reason why Arriba! is truly a sensible and affordable choice for Linux development.

IDE Features

• **Integrated Edit-Compile-Run** functionality constructed within a single, uniform windows-desktop environment… all at the convenience of a few mouse clicks

• **Modern User Interface:** High-performance user interface in 100% pure Java

• **Flexible and Portable Project Management** with "smart recompile" and Makefile export

• **Optional Integration with CVS** supports visual check in/out and diff/merge capabilities from a unified desktop (through Arriba! plug-ins).

• **Syntax-Highlighted Editor** with built-in parser, class/method viewer, and optional VI/EMACS emulation

• **Optional Code Profiler** quickly finds hot spots and memory leaks in code (through Arriba! plug-ins).

• **Mixed-Language Debugger:** C/C++ and Java (through Arriba! plug-ins)

• **CORBA-based Framework:** Makes it easy for other third parties to integrate and leverage capabilities of Arriba!

VIO SOFT

The Arriba! IDE build environment

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pRISM+ for pSOSystem/MIPS

Embedded Development for MIPS Processors

Salient Features

- pRISM+ cross-development environment speeds all phases of embedded application development and debugging

- Bundled with pSOSystem RTOS

- Most complete offering of communications protocols and network management tools in the embedded industry

- Includes BSP source code for NEC evaluation boards (DDB-VRC4373, DDB-VRC4375, DDB-VRC5074, DDB-VRC5476)

- Bundled with full documentation, sample applications, and utilities to speed time to market

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Sun and HP workstations and Windows 95/98/NT

Product Overview

pRISM+ for pSOSystem/MIPS is a complete development environment for embedded applications using the MIPS family of microprocessors. pRISM+ features sophisticated OS aware debugging and includes advanced browsing and code management tools. It provides project management for all sizes of product development teams, from individuals to complete departments. The open, extensible environment is based on the CORBA standard. pRISM+ is supported by a wide variety of third-party partners.

The pSOSystem/MIPS family of embedded products can be scaled to produce simple stand-alone devices all the way up to complex, fault-tolerant multiprocessing systems. The pSOSystem's object-oriented design delivers maximum flexibility, efficiency, and reliability.

pSOS+ and pSOS+m Kernels

The pSOSystem/MIPS target software family is based on the robust pSOS+ real-time kernel technology—it's fully preemptible, reentrant, multitasking, and deterministic. Its sophisticated priority-based scheduler supports preemptive, round-robin, and time-based scheduling.

Its modern, object-oriented design provides maximum flexibility and reliability. pSOS+ objects include tasks, semaphores, events, timers, and fixed- and variable-length queues, along with memory regions and partitions.

Interrupt handling is done through Interrupt Service Routines (ISRs) placed outside the kernel. To provide the fastest possible interrupt response time, interrupts can be passed directly to ISRs. System calls made from an ISR return to the ISR, eliminating time-consuming kernel scheduling mechanisms.

The pSOS+m kernel is a multiprocessor extension of the pSOS+ kernel. It shares the pSOS+ API, allowing you to easily migrate your uniprocessor application to a multiprocessor environment. pSOS+m's object-oriented design provides processor-independent operation, allowing different families of processors to be mixed in the same application.

Complementing the object-oriented kernels is pROBE+, a sophisticated kernel-aware target debugger and monitor. Optionally, both a reentrant ANSI C library and a C++ class library are available.

High-Performance File Systems

The pSOSystem file system manager, pHILE+, provides support for four separate file system formats: an integrated systems file system format optimized for real-time operation; an MS-DOS file system covering both floppies and hard disks; the ISO 9660 CD-ROM file system; and the client services side of the NFS file system.

Networking Support

The pSOSystem networking suite offers the industry's richest set of target-based networking capabilities.

- TCP/IP Internet protocol bundle—Zero-copy pNA+, NFS, Telnet, FTP and BootP (both client and server), TFTP server product
- STREAMS networking framework—OpEN product
- STREAMS-based protocols—X.25, OSPF, RIP2, TCP/IP
- SNMP Version 1 and Version 2, CMIP
- PPP and compressed SLIP
- Remote Procedure Calls (RPC) with XDR support

Integrated Development Environment

pRISM+ is an Integrated Development Environment (IDE) running on either UNIX workstations or PC-compatible systems. The pRISM+ cross-development environment enables both individual programmers and project teams to focus on efficient development of applications. Included in this environment are:

- pRISM+ software development environment, including C and C++ compilers, editor, version control system, graphical class browser and program builder
- Searchlight source-level debugger
- Application profiling and tuning tools
- Object and code browsers
- ESp visual debugging and task-level profiler

Board Support Packages (BSPs)

pRISM+ for pSOSystem includes, at no charge, tested Board Support Package source code. ISI provides BSP source code to facilitate the support of custom boards, as well as to support developers who wish to use standard boards.

Currently, BSP code is supplied for these NEC evaluation boards:

- DDB-VRC4373
- DDB-VRC4375
- DDB-VRC5074
- DDB-VRC5476

Integrated Systems views its customer relationships as long-term partnerships. Much of its 15 years of success and the over 5,000 pSOS+ embedded design wins can be attributed to this customer commitment. In addition to nonstop research and development to keep pRISM+ for pSOSystem software at the technological forefront, Integrated Systems' customers enjoy comprehensive training, maintenance, on-line and telephone support, and field applications engineering.

Additionally, Integrated Systems provides the latest in third-party hardware and software support. Contact Integrated Systems for information on all MIPS processor supported tools and products.

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Tornado™ Development Platform

Featuring the Industry-Leading VxWorks® RTOS

Salient Features

▶ A superior development and deployment platform for the embedded developer

▶ Makes all tools available regardless of target resources or connection strategy

▶ Runs on UNIX workstations, or PCs using Microsoft Windows 95 or Windows NT

▶ Offers published APIs for easy customization and third-party tool integration

▶ Provides central "control panel" and productivity-enhancing GUI

▶ Supports industry standards, including ANSI-C, POSIX, and TCL

▶ Fully integrated with proven, high-performance VxWorks operating system

▶ Scalable across all real-time implementations

CPUs Supported

NEC VR43xx, VR4400, VR5000, VR5432

Host Platforms

UNIX workstations, Windows 95/NT

Product Overview

Available for both UNIX- and Microsoft Windows-based hosts, the revolutionary Tornado development platform consists of the Tornado tools suite, the VxWorks RTOS, and a full range of communications options connecting host and target. All Tornado tools can be utilized at any stage of application development, with any level of target system resources. All are fully integrated and have sophisticated GUIs, and all are available regardless of target connection strategy (Ethernet, serial, ICE, ROM monitor, or custom). The Tornado APIs are published, from the GUI interfaces down to the debug agent interface, to facilitate customization and third-party integration. In addition, developers can take advantage of a variety of productivity-enhancing WindPower™ tools, including the VxSim™ simulator, the WindView™ system visualizer, and the StethoScope data monitor.

VxWorks provides fast multitasking, preemptive scheduling (with optional round-robin scheduling for same-priority tasks) and fast interrupt responses. To these microkernel features, VxWorks adds intertask communications and synchronization facilities, efficient memory management, multiprocessing support, a fast I/O system, IDE and SCSI support, and MS-DOS- and RT-11-compatible file systems.

Tornado networking includes 4.4 BSD UNIX TCP/IP, sockets, NFS, RPC, ftp, rlogin, telnet, and optional support for the X Window system. A wide range of integrated third-party networking products are available through Wind River's WindLink™ Partner program, including ATM, OSI, SS7, Frame Relay, CORBA, ISDN, X.25, CMIP/GDMO, V.2, Iv6, XTP, Internet Protocols, and distributed network management.

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Evaluation Boards

P-4032 Prototyping Board for VR4300 Applications

Salient Features

◗ High performance through simplicity

◗ Supports VR4300 and VR4100 CPUs

◗ CPU interface runs at up to 133 MHz

◗ PCI expansion slots

◗ PC-world devices for low-cost, rich I/O

◗ Modular reusable design, easy license terms

◗ Extensive software support

◗ "Debug board" makes cycles visible, hides high-speed signals

CPUs Supported

NEC VR43xx, VR4100: any 32-bit bus "SysAD" MIPS CPU from NEC

Host Platforms

Compatible with any PC or UNIX host

Product Overview

Algorithmics' P-4032 is a key part of a package of hardware, software tools, and support which can help you through evaluation, porting, and redesign using the VR4300 or VR4100 with the minimum of hassle.

About P-4032

P-4032 is designed to help you get your software running, and to form a reusable example of an efficient VR4300 system design. And it's surrounded by software (some freely reusable, all available for reasonably priced licensing).

• NEC VR4300 or VR4100 CPU: 64-bit power in a low-cost, low-power package with a 32-bit bus

• High performance through simplicity: P-4032 models the kind of design useful in embedded systems. It uses high clock rates and simple, low-latency data paths, but avoids features which add cost and complexity.

• PCI expansion: standard 32-bit, 33-MHz PCI bus, with 3.3-volts-compatible slots available

• PC-world devices for low-cost, rich I/O: includes a big choice of cheap I/O to solve your interfacing problems

• Hardware featured for development support: Centronics interface for fast download from PC; flash PROM for easy reprogramming; onboard Ethernet for download/debug from UNIX hosts; customizable interrupt controller

• Modular reusable design: the P-4032's logic design is open. Schematics and logic listings are available to customers; you can license the complete design; or you can obtain permission to reuse chunks of logic for a modest one-off payment.

• PMON monitor and SDE-MIPS integration: the PMON debug monitor is fitted to every board. You can build programs for P-4032 with Algorithmics' SDE-MIPS package, right out of the box.

• OS support: Windows CE OAL and VxWorks BSP available from Algorithmics—in-house developed and supported.

• OpenBSD and Linux available; ported by volunteers encouraged by Algorithmics. Sources and binaries are free; support is available.

P-4032 Hardware Features

• CPU: NEC VR4300 at up to 67 MHz interface speed. Various configurations are jumper selectable, including the "little-endian" mode. However, software will have to adapt appropriately.

• Main memory: from 2–64 MB 32-bit-wide DRAM using two slots for industry-standard 32-bit SIMMs. Burst EDO memory gives the best performance, but standard EDO or fast page mode modules work too. You can even fit a DRAM-pinout flash module. This is just about as efficient

◈)algorithmics

a 32-bit MIPS memory as can be implemented, with access latency of 100 ns at the CPU pins and burst bandwidth of 266 MB/s.

- PROM: 512 KB (8-bit) flash PROM, and a socket for a 512 KB (8-bit) EPROM or emulator. The CPU can boot from either ROM, and run cached from it.
- Ethernet interface: "thickwire" interface using a DEC 21041 PCI bus controller. Supports fast download and host access, essential for a good development environment.
- SCSI interface: using a 53C810 PCI bus controller for high performance and flexibility
- Other I/O: dual high-speed serial ports, bidirectional Centronics (can implement either a "host" or "printer" port), diskette interface, EEPROM for "environment" store, real-time clock, PC-compatible keyboard, general-purpose parallel I/O, customizable interrupt controller
- Diagnostic display: either 4-character LED display, or a larger LCD display, for diagnostic and debug messages
- PCI bus sockets: two standard edge connector sockets and one optional slot for customer's development daughterboards (all PCI signals, plus some useful extras)
- Optional debug header/card: fits onto the board, demultiplexing and presenting address and data for your logic analyzer. Includes reprogrammable trigger PAL.

Software Support

Algorithmics' SDE-MIPS is a software development toolkit available for a wide range of hosts. The GNU C compiler at the heart of SDE-MIPS supports modern language standards and its optimizer is state of the art. SDE-MIPS supports source-level debug of software running on the P-4032.

Target Software and OS

Customers can choose run-time software for P-4032 from:

- Windows CE OAL and drivers are available from Algorithmics.
- Wind River Systems' VxWorks real-time OS runs on most of these CPUs, and Algorithmics can supply a BSP (priced according to support levels).
- Other RTOSs such as pSOS from ISI should run; enquire for details.
- AlgRTX, Algorithmics' lightweight POSIX-threads RTOS, is available as source code on a one-time license for applications needing a customized but standards-compliant kernel.

- Both Linux and the OpenBSD derivative of BSD4.4 run on P-4032. They each offer a high-end multitasking environment for the board; appropriate for customers whose need is easy porting more than real-time scheduling.
- PMON is a bootstrap/monitor program originally developed by LSI Logic, Inc., but placed by that company in the public domain. Algorithmics have enhanced PMON to run on R4xxx processors, and to incorporate an Ethernet loader.

Price and Availability

P-4032 is available directly from Algorithmics in England, and has been in full production since April 1996. Prices (with 16 MB DRAM) start around $3200/£2100 in small volumes.

Technology Licensing

The P-4032 and its software are available for license. A comprehensive manufacturing license for the whole board is available for a one-time payment of $35,000, with no royalties payable thereafter. Similar affordable, no-nonsense deals are available for use of chunks of logic.

P-4032 History

Algorithmics are the leading supplier of R4x00 evaluation platforms; our P-4000i product is in use with about 100 customers all over the world. P-4032 was developed over the winter of 1995/96 in response to increasing customer interest in the low-cost VR4300 variant of the MIPS CPU.

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P-5064 Prototyping Board for VR5000 Applications

Salient Features

◗ High performance through simplicity

◗ Fast SDRAM memory system: CPU/DRAM system runs up to 100 MHz

◗ PCI and ISA expansion slots

◗ PC-world devices for low-cost, rich I/O

◗ Modular reusable design available for license

◗ Excellent software support

CPUs Supported

NEC VR5000

Host Platforms

Compatible with UNIX and PC hosts

Product Overview

Some of the biggest names in embedded applications rely on Algorithmics' packages of hardware, software tools, and support. We can help you through evaluation, porting, and redesign with the minimum of hassle.

About P-5064

If your application requires all the CPU power you can reasonably get, you will find the best deal from 64-bit MIPS CPUs - and you're going to need a high-end I/O system and first-class tools to support it.

P-5064 will help you get your software running soon and fast, and is a reusable example of an efficient MIPS system design.

And it's surrounded by software (some freely reusable, all available for reasonably priced licensing).

- CPU: NEC VR5000. Get power up to and beyond 200 MHz PC processors but without their price, heat, and power consumption.

- High performance through simplicity: P-5064 models the kind of design useful in embedded systems. It uses high clock rates and simple, low-latency data paths, but avoids features which add cost and complexity.

- SDRAM memory system: synchronous DRAM modules provide 1-word/clock bursts of 64-bit data, with parity protection. The DRAM module sets the bus interface clock rate, between 75–100 MHz.

- PCI + ISA expansion: standard 32-bit 33-MHz PCI bus, old-fashioned ISA slot

- PC-world devices for low cost, rich I/O: a vast choice of I/O to solve your interfacing problems

- Hardware featured for development support: Centronics interface for fast download from PC; flash PROM for easy reprogramming; onboard Ethernet for download/debug from UNIX hosts; customizable interrupt controller

- Modular reusable design: P-5064's logic design is open. Schematics and logic listings are available to customers; you can license the complete design; or you can obtain permission to reuse chunks of logic for a modest one-off payment.

- PMON monitor and SDE-MIPS integration: the PMON debug monitor is fitted to every board. You can build programs for P-5064 with Algorithmics' SDE-MIPS package, right out of the box.

- OS support: VxWorks and pSOS, and a demonstrable port of OpenBSD.

P-5064 Hardware Features

- CPU: VR5000 or other 64-bit MIPS CPU at 75–100 MHz interface speed. These CPUs have big on-chip caches, but the board can also be configured with an external secondary cache as a build-time option.

- Various configurations are available, including the "little-endian" mode.

- Main memory: from 16–256 MB 72-bit-wide synchronous DRAM in DIMM modules. VR5000 CPUs need fast, low-latency memory, and this is just about the best that can be done at low cost; access latency is 100 ns at the CPU pins and the burst bandwidth hits 800 MB/s.

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- PROM: 1 MB x 8-bit flash PROM, and a socket for a 512 KB x 8-bit EPROM or ROMulator. The CPU can boot from either ROM, and run cached from it.
- PCI bus sockets: three standard edge connector sockets
- ISA bus socket: for those low-cost peripherals
- PC card (PCMCIA) dual socket: when you've got to prototype something which will be small...
- 10/100 Mb/s Ethernet: transceiver or twisted-pair connection using a DEC 21143 PCI bus controller. Supports fast download and host access, essential for a good development environment.
- SCSI interface: using a 53C810 PCI bus controller for high performance and flexibility
- IDE interface: two channels, PCI bus DMA
- Other I/O: dual high-speed serial ports, bidirectional Centronics (can implement either a "host" or "printer" port), diskette interface, EEPROM for "environment" store, real-time clock, USB sockets, PC-compatible keyboard + PS/2 mouse, general-purpose parallel I/O
- Customizable interrupt controller: can be reconfigured to group devices onto different CPU interrupt pins, to provide efficient support for a variety of different operating systems.
- Diagnostic display: choice of a 4-character LED display, or a larger LCD display, for diagnostic and debug messages.
- Debug header/card: available as an option, demultiplexes and presents address and data for your logic analyzer. Includes reprogrammable trigger PAL.

Software Support

Algorithmics' SDE-MIPS is a software development toolkit hosted on Windows95, Windows/NT, Sun SPARC, HP-UX, SGI (MIPS-ABI), BSD/OS, and Linux. The GNU C compiler at the heart of SDE-MIPS supports modern language standards and its optimizer is state of the art. The toolkit has full support for VR5000's MIPS IV instruction set. SDE-MIPS supports source-level debug of software running on the P-5064 and includes comprehensive libraries and lots of sample sources.

Target Software and OS

Customers can choose run-time software for P-5064 from:

- Windows CE OAL and drivers are available from Algorithmics.

- BSPs for Wind River Systems' VxWorks RTOS and ISI's pSOS will be available at launch or soon after, priced according to support levels.
- AlgRTX, Algorithmics' lightweight POSIX-threads RTOS, is available for applications needing a customized but standards-compliant kernel. Enquire for details.
- We will have the OpenBSD derivative of UNIX 4.4BSD running on P-5064. This offers a highly POSIX-compliant multitasking environment for the board; appropriate for customers whose requirements are ease of implementation and porting, rather than real-time scheduling.
- We expect to have Linux available soon.
- PMON is a bootstrap/monitor program originally developed by LSI Logic, Inc., but placed by LSI in the public domain. Algorithmics use PMON on all our MIPS products.

Price and Availability

P-5064 is available directly from Algorithmics in England.

Technology Access

The P-5064 and its software are open to customers. Schematics and logic programs are available to any customer on request. We encourage customers to reuse logic from the design and can offer transfer and support packages.

P-5064 and Algorithmics

Algorithmics are the leading supplier of 64-bit MIPS prototyping platforms; our P-4000i product is in use with about 100 customers all over the world, but our P-4032 (for CPUs with 32-bit bus interfaces) has overtaken it in volume after only 12 months. P-5064 was developed in 1996/97 in response to increasing customer interest in the vast potential of the VR5000 CPU.

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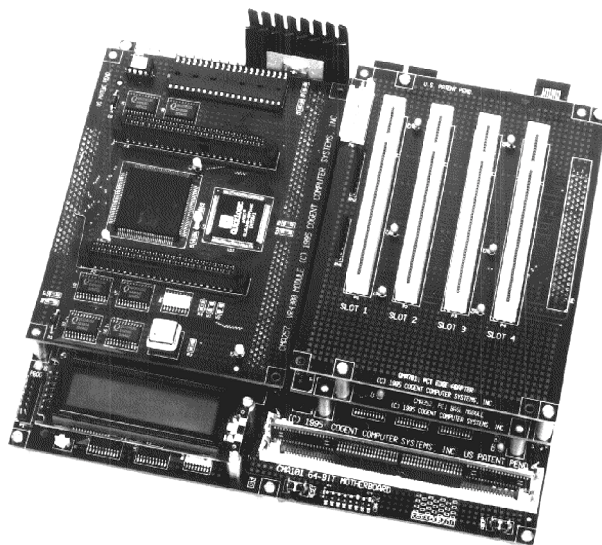
Cogent Modular Architecture (CMA) Support for the VR4300 and VR5000 Processors

Salient Features

- Universal development platform

- Interchangeable 32/64-bit CPU slot

- Three 32/64-bit I/O expansion slots

- 32-bit VR4300 CPU module

- 64-bit VR5000 CPU module

- Up to 32 MB 32/64-bit DRAM

- Parallel port—bidirectional Centronics

- Serial ports—dual RS-232

- 2-line x 16-character LCD display

- 512 KB user EPROM

- Real-time clock with 2 KB NVRAM

- PCI development options

- Flash, IndustryPack, and SRAM

- Compact 8.7" by 7.9" system board with PC-AT power supply connector

CPUs Supported

NEC VR4300 and VR5000

Host Platforms

Windows 3.1, Windows 95, Windows NT, Sun Solaris, SunOS, HP-UX, and DEC ULTRIX

Introduction

Cogent Modular Architecture (CMA) offers an exceptional microprocessor development tool for embedded system design. Featuring a universal motherboard that supports interchangeable CPU and I/O modules, the CMA can be customized to meet the developer's project needs. The platform's broad microprocessor support and PCI capability make it one of the most flexible tools currently available for hardware and software development.

CMA Motherboard

The CMA motherboard is a 32/64-bit platform designed to support a single CMA-compatible CPU module and up to three CMA I/O expansion modules. Standard features include dual channel RS-232 serial ports; bidirectional centronics-compatible parallel port; 2-line by 16-character LCD display for status/debug; real-time clock/calendar with 2 KB of battery-backed NVRAM; and two 32-bit standard SIMM sockets for up to 32 MB of DRAM. The motherboard requires
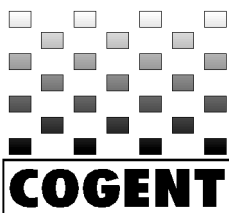
a standard PC AT-style power supply and a connector is provided.

CMA CPU Modules

The motherboard is customized with the development engineer's preferred microprocessor plugged into the dedicated, 32/64-bit CMA CPU module slot. Cogent's CPU module line currently supports over 25 RISC processors.

VR4300 CPU Module (CMA 257)

The CMA257 was designed to allow the user to add the power of the VR4300 to a standard CMA system. This 32-bit CPU module supports the VR4300 at up to 133 MHz. VR4300 features include 16 KB I-cache/8 KB D-cache; 64-entry TLB MMU; floating-point coprocessor; and on-chip 32-bit timer. In addition, a 4-deep external write buffer offloads the CPU during write operations. The CMA257 provides for code testing and debugging through a pair of high-density connectors that allow all CPU signals to be probed. There is also a 16-bit EPROM for boot code.

VR5000 CPU Module (CMA260)

The CMA 260 allows the user to add the power of the VR5000 to a standard CMA system. This 64-bit CPU module supports the VR5000 at up to 200 MHz. VR5000 features include 32 KB I-cache/32 KB D-cache; 48-entry TLB MMU; floating-point coprocessor; and on-chip 32-bit timer. In addition, a 4-deep external write buffer offloads the CPU during write operations. The CMA260 provides for code testing and debugging through a pair of high-density connectors that allow all CPU signals to be probed. There is also a 16-bit EPROM for boot code.

CMA I/O Modules

The CMA motherboard allows add-on functionality with its three I/O module slots. Cogent has designed a series of CMA I/O modules that work with any of the supported processors. CMA I/O modules include PCI, flash, SRAM, and IndustryPack. Custom I/O is also available.

CMA PCI Modules

PCI base modules and card adapters allow developers to integrate PCI functions into the system using off-the-shelf third-party or custom PCI cards. PCI bridge chip choices include V3 Semiconductor's V962PBC (CMA352) or PLX Technology's PCI9080 (CMA353). Card adapters support PCI Edge Cards, PMC Cards, and Compact PCI.

The CMABUS expansion module (CMA369) acts as a front end to interface various remote cards to the CMA system. Interfacing the CMABUS to a PCI Edge Paddle Card allows developers to use the CMA for prototyping intelligent RISC-based PCI cards.

Third-Party Tools

Cogent is committed to offering support for the latest in third-party tools. Current third-party tool support includes Green Hills, ISI pSOS, Wind River, and GNU. Call, e-mail, or check the Web for up-to-date information on tool support.

Ordering Information

CMA102:	Three-Slot Motherboard
CMA257:	VR4300 CPU Module @ 100 MHz
CMA260:	VR5000 CPU Module @ 200 MHz
CMA352:	PCI Base Module, V3 V962PBC
CMA353:	PCI Base Module, PLX PCI9080
CMA701:	PCI Edge Card Adapter Module
CMA701H:	PCI Edge Card Adapter w/ HP Connector
CMA369:	32-bit CMABUS Expansion Module
CMA601:	PCI Edge Paddle Card, V3 V962PBC
CMA602:	PCI Edge Paddle Card, PLX PCI9080
CMA801:	Generic Test Adapter (Order by sets of 2)
CMA802:	CPU to HP Logic Analyzer Adapter

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DVE-R4000/20 64-Bit VMEbus RISC Processor Board

The VR4400 is a single-chip RISC microprocessor integrating a CPU, an FPU, 16 KB instruction cache, and 16 KB data cache. It operates with a 50 MHz clock (an internal clock is 100 MHz) and a 33 MHz interface clock. Two types of gate arrays (two data path controllers and one address path controller) that have been developed for this board are installed. They control the CPU system interface, main memory, timing, local bus address decode, and other functions.

The standard main memory for this board is 32 MB RAM expandable up to 128 MB. The CPU can perform 1- to 8-byte single read/write cycles or 16- or 32-byte block read/write cycles with respect to this memory, while devices on the local bus can perform 1- to 4-byte read/write cycles. The following components are also installed on this board: two 40-pin ROM sockets (1 MB), a SCSI-II interface (NCR53C710), an Ethernet interface (i82596CA), a two-channel RS-232-C interface (μPD72001), a real-time clock with battery-backed RAM (DS1643), and a VMEbus interface gate array (including two channels of 24-byte timers and other components). This board operates on the VMEbus as a master board and also has functions as a VMEbus system controller.

The DVE-R4000/20 supports Wind River Systems' VxWorks and JMI's C-Executive for real-time operating systems, and also supports Green Hills' C-Compiler and MULTI as a symbolic debugging development environment. This outstanding processing speed and floating-point performance makes the DVE-R4000/20 an ideal solution for scientific and industrial applications.

Salient Features

◗ High-performance CPU

◗ 32 MB DRAM

◗ Two 40-pin ROM sockets

◗ Intelligent I/O functionality

◗ Dual full-duplex RS-232-C serial port

◗ Real-time clock plus battery-backed RAM

◗ VMEbus interface gate array

◗ Standard VMEbus interface

◗ Double-height VMEbus board

CPUs Supported

NEC VR4000

Product Overview

The DVE-R4000/20 is a VMEbus (IEEE-1014)-compatible CPU board. Its CPU core is a high-performance 64-bit RISC microprocessor, the VR4400PC (μPD30410), manufactured by NEC.

Features

CPU

NEC VR4000 PC operating clock: 50 MHz (internal clock: 100 MHz); interface clock: 33 MHz; instruction cache: 16 KB; data cache: 16 KB

Main Memory (DRAM)

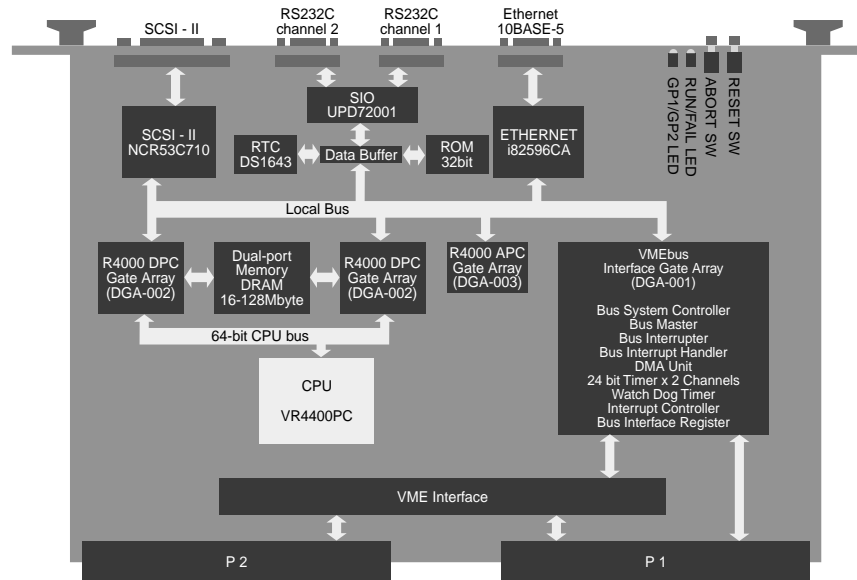144 bits (128 data bits with byte parity); 16 to 128 MB; 16/32/64/128 MB; four 1/2/4/8 Mword x 36-bit SIMMs

ROM

Two 40-pin IC sockets (1 MB at maximum); 2 x 27C1024: 256 KB, 2 x 27C2048: 512 KB, 2 x 27C4096: 1 MB

Ethernet Interface

i82596CA and 15-pin AUI connector

DENSAN

Serial Interface (J2 and J3)

Two full-duplex RS-232-C interfaces; µPD72001; 9-pin DSUB male connector.

SCSI-II Interface (J4)

NCR53C710; 5 MB max. (SCSI spec.) using asynchronous transfer; 10 MB max. (SCSI spec.) using synchronous transfer; 50-pin mini ribbon connector.

Real-Time Clock Plus Battery-Backed RAM

DS1643

VMEbus Interface Gate Array

VMEbus system controller; VMEbus master; VMEbus interrupter; VMEbus interrupt handler; DMA unit (between onboard RAM and VMEbus); 24-bit timer x 2 channels; watchdog timer; interrupt controller; VMEbus interface register.

VMEbus Interface

A32/D32 master/slave; A16/D32 slave (interface register); RMW function support; system controller (system clock driver, arbiter, IACK daisy chain driver, bus timer); IH (1 to 7), D08 (O) interrupt handler; ROAK, D08 (O) interrupt.

Operating Conditions

Operating temperature: 0–55°C; relative humidity: 90% max (noncondensing); cooling requirements: over 1m/s air flow for forced-air cooling.

Power Consumption

3.3 volts: 4.2 A typical; +12 volts: only when an Ethernet interface is used.

Mechanical Specifications

Double-height, single-slot VME board; height: 233.35 mm; depth: 160 mm; width: 40 mm (double slot).

Contact List

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DVE-R4100/20 64-Bit VMEbus RISC Processor Board

The VR4100 is a single-chip RISC microprocessor with 32-bit external address/data bus width integrating a CPU, 2 KB instruction cache, and 1 KB data cache. It operates with a 33 MHz internal clock and external clock.

The standard main memory for this board is 16 MB of DRAM. The CPU can perform 1- to 4-byte single read/write cycles or 8, 16-byte block read/write cycles with respect to this memory.

The following components are also installed on this board: two 40-pin EPROM sockets (1 MB at maximum) and 4 MB of flash EEPROM, a SCSI-II interface (NCR53C710), an Ethernet interface (i82596CA), a two-channel RS-232-C interface (μPD72001), a real-time clock with battery-backed RAM (DS1643), and a VMEbus interface gate array (including two channels of 24-byte timers and other components).

The DVE-R4100/20 operates on the VMEbus as a master board and also has functions as a VMEbus system controller.

The DVE-R4100/20 supports Wind Rivers Systems' VxWorks and JMI's C-Executive for real-time operating systems, and also supports Green Hills' C-Compiler and MULTI as a symbolic debugging development environment.

Salient Features

- High-performance CPU

- 16 MB DRAM

- Two 40-pin ROM sockets

- Intelligent I/O functionality

- Dual full-duplex RS-232-C serial port

- Real-time clock plus battery-backed RAM

- VMEbus interface gate array

- Standard VMEbus interface

CPUs Supported

NEC VR4100

Product Overview

The DVE-R4100/20 is a VMEbus (IEEE-1014)-compatible CPU board. Its CPU core is a high-performance 64-bit RISC microprocessor, the VR4100PC (μPD30100), manufactured by NEC.

Features

CPU

NEC VR4100PC. Internal/external clock: 33 MHz); instruction cache: 2 KB; data cache: 1 KB

Main Memory (DRAM)

16 MB (4 MB x 4 bits x 8) with byte parity

ROM

Two 40-pin IC sockets (1 MB at maximum); 2 x 27C1024: 256 KB; 2 x 27C2048: 512 KB; 2 x 27C4096: 1 MB

Ethernet Interface

i82596CA and 15-pin AUI connector

Serial Interface (J2 and J3)
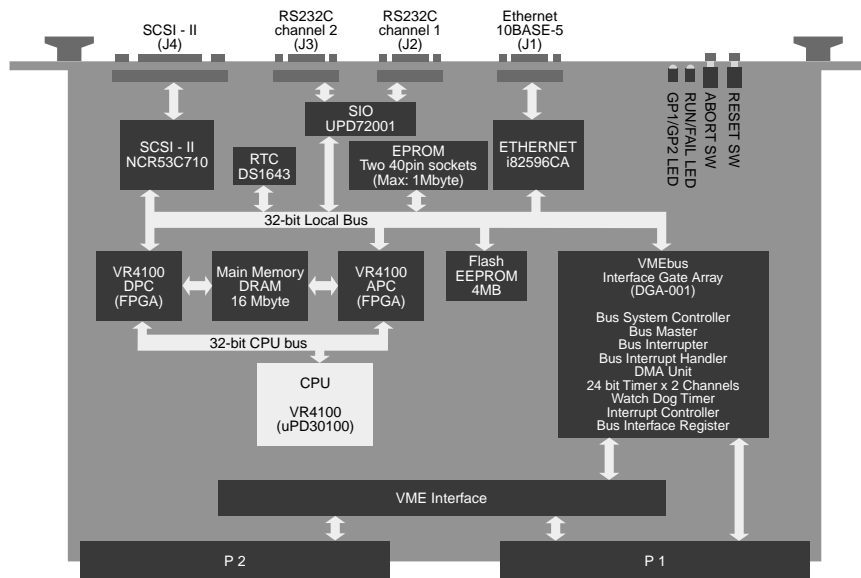
Two full-duplex RS-232-C interfaces; μPD72001; 9-pin DSUB male connector

SCSI-II Interface (J4)

NCR53C710; 5 MB max (SCSI spec) using asynchronous transfer; 10 MB max (SCSI spec) using synchronous transfer; 50-pin mini ribbon connector.

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Real-Time Clock Plus Battery-Backed RAM

DS1643

VMEbus Interface Gate Array

VMEbus system controller; VMEbus master; VMEbus interrupter; VMEbus interrupt handler; DMA unit (between onboard RAM and VMEbus); 24-bit timer x 2 channels; watchdog timer; interrupt controller; VMEbus interface register.

VMEbus Interface

A32/D32 master/slave; A16/D32 slave (interface register); RMW function support; system controller (system clock driver, arbiter, IACK daisy chain driver, bus timer); IH (1 to 7), D08 (O) interrupt handler; ROAK, D08 (O) interrupt.

Operating Conditions

Operating temperature: 0–55°C; relative humidity: 90% max. (noncondensing); cooling requirements: over 1m/s air flow for forced-air cooling.

Power Consumption

3.3 volts: 4.2 A typical; +12 volts: only when an Ethernet interface is used.

Mechanical Specifications

Double-height, single-slot VME board; height: 233.35 mm, depth: 160 mm, width: 40 mm (double slot).

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DVE-R4300/20 64-Bit VMEbus RISC Processor Board

The VR4300 is a 64-bit single-chip RISC microprocessor with a 32-bit external address/data bus integrating a CPU, an FPU, 16 KB instruction cache, and 8 KB data cache. It operates with a 100 MHz internal clock and a 33 MHz external clock.

On the DVE-R4300/20, 16 MB of RAM is installed as main memory which can perform single read/write cycles from 1 to 4 bytes and block read/write cycles with 8, 16, or 32 bytes.

The following components are also installed on this board: two 40-pin ROM sockets (1 MB at maximum), 4 MB of flash memory, and a jumper setting which allows either ROM or flash memory to run. It also has a SCSI-II interface (NCR53C710), an Ethernet interface (i82596CA), two channels of RS-232-C interface (µPD72001), a real-time clock with battery-backed RAM (DS1643), and a VMEbus interface gate array (including two channels of 24-bit timers and other components).

This board operates on the VMEbus as a master board, and also functions as a VMEbus system controller.

Salient Features

‣ High-performance CPU

‣ 32 MB DRAM

‣ Two 40-pin ROM sockets

‣ Intelligent I/O functionality

‣ Dual full-duplex RS-232-C serial port

‣ Real-time clock plus battery-backed RAM

‣ VMEbus interface gate array

‣ Standard VMEbus interface

‣ Double-height VMEbus board

CPUs Supported

NEC VR4300

Product Overview

The DVE-R4300/20 is a VMEbus (IEEE-1014)-compatible CPU board. Its CPU core is a high-performance 64-bit RISC microprocessor, the VR4300 (µPD30200), manufactured by NEC.

Features

CPU

NEC VR4300 (µPD30200) operating clock: 100 MHz (internal clock: 100 MHz); interface clock: 33 MHz; instruction cache: 16 KB, data cache: 8 KB

Main Memory

16 MB (32 bits) with parity

ROM

Two 40-pin IC sockets (1 MB at maximum); 2 x 27C1024: 256 KB, 2 x 27C2048: 512 KB, 2 x 27C4096: 1 MB

Flash Memory

4 MB

Ethernet Interface

i82596CA and 15-pin AUI connector

Serial Interface (J2 and J3)

Two full-duplex RS-232-C interfaces; µPD72001; 9-pin DSUB male connector

SCSI-II Interface (J4)

NCR53C710; 5 MB max. (SCSI spec.) using asynchronous transfer; 10 MB max. (SCSI spec.) using synchronous transfer; 50-pin mini ribbon connector.

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Real-Time Clock Plus Battery-Backed RAM

DS1643

VMEbus Interface Gate Array

VMEbus system controller; VMEbus master; VMEbus interrupter; VMEbus interrupt handler; DMA unit (between onboard RAM and VMEbus); 24-bit timer x 2 channels; watchdog timer; interrupt controller; VMEbus interface register.

VMEbus Interface

A32/D32 master/slave; A16/D32 slave (interface register); RMW function support; system controller (system clock driver, arbiter, IACK daisy chain driver, bus timer); IH (1 to 7), D08 (O) interrupt handler; ROAK, D08 (O) interrupt.

Operating Conditions

Operating temperature: 0–60°C; relative humidity: 90% max. (noncondensing); cooling requirements: over 1m/sec air flow for forced-air cooling.

Power Consumption

+5 volts: 4.2 A typical; +12 volts: only when an Ethernet interface is used.

Mechanical Specifications

Double-height single-slot VME board; height: 233.35 mm, depth: 160 mm, width: 40 mm (double slot).

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DVE-R5000/20 64-Bit VMEbus RISC Processor Board

The VR5000 is a single-chip RISC microprocessor integrating a CPU, an FPU, 32 KB of instruction cache, and 32 KB of data cache. It operates with an internal clock of 200 MHz and an external clock of 33 MHz. The VR5000 has a built-in secondary cache controller and an optional secondary cache of 512 KB.

The standard main memory for this board is 32 MB DRAM. The CPU can perform 1- to 8-byte single read/write cycles and 32-byte block read/write cycles with respect to this memory.

The following components are also installed on this board: two 40-pin ROM sockets (maximum of 1 MB of EPROM and 4 MB of flash EEPROM), a SCSI-II interface (NCR53C710), an Ethernet interface (i82596CA), a two-channel RS-232-C interface (μPD72001), a real-time clock with battery-backed RAM (DS1643), and a VMEbus interface gate array (including two channels of 24-byte timers and other components). This board operates on the VMEbus as a master board, and also has functions as a VMEbus system controller.

The DVE-R5000/20 supports Wind River Systems' VxWorks and JMI's C-Executive for real-time operating systems, and also supports Green Hills' C-Compiler and MULTI as a symbolic debugging development environment.

This outstanding processing speed and floating-point performance makes the DVE-R5000/20 an ideal solution for scientific and industrial applications.

Salient Features

- High-performance CPU

- 32 MB DRAM

- Two 40-pin ROM sockets

- Intelligent I/O functionality

- Dual full-duplex RS-232-C serial port

- Real-time clock plus battery-backed RAM

- VMEbus interface gate array

- Standard VMEbus interface

- Double-height VMEbus board

CPUs Supported

NEC VR5000

Product Overview

The DVE-R5000/20 is a VMEbus (IEEE-1014)-compatible CPU board. Its CPU core is a high-performance 64-bit RISC microprocessor, the VR5000 (μPD30500), manufactured by NEC.

Features

CPU

NEC VR5000 (μPD30500); internal clock: 200 MHz; external clock: 33 MHz; instruction cache: 32 KB; data cache: 32 KB

Main Memory

32 MB (parity option)

ROM

Two 40-pin IC sockets (1 MB at maximum); 2 x 27C1024: 256 KB; 2 x 27C2048: 512 KB; 2 x 27C4096: 1 MB

Flash Memory

4 MB
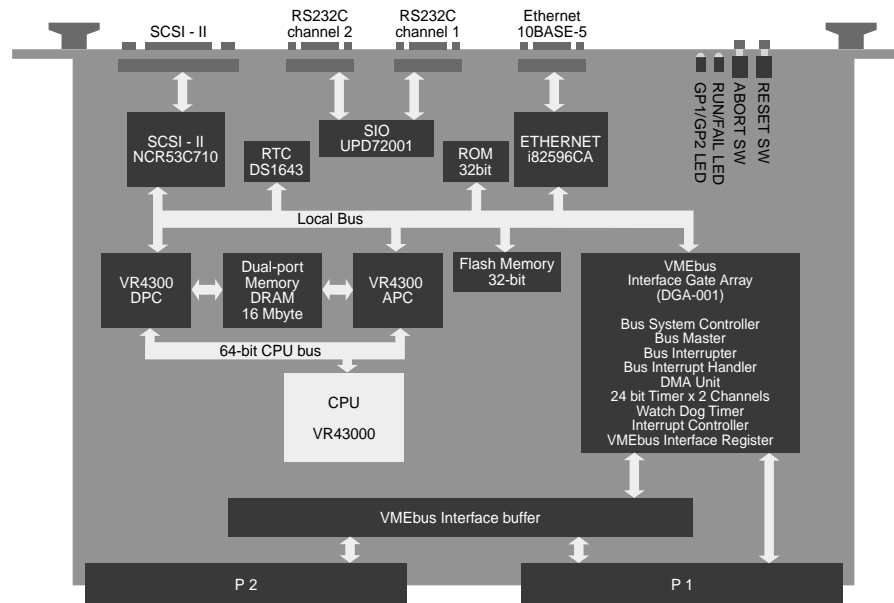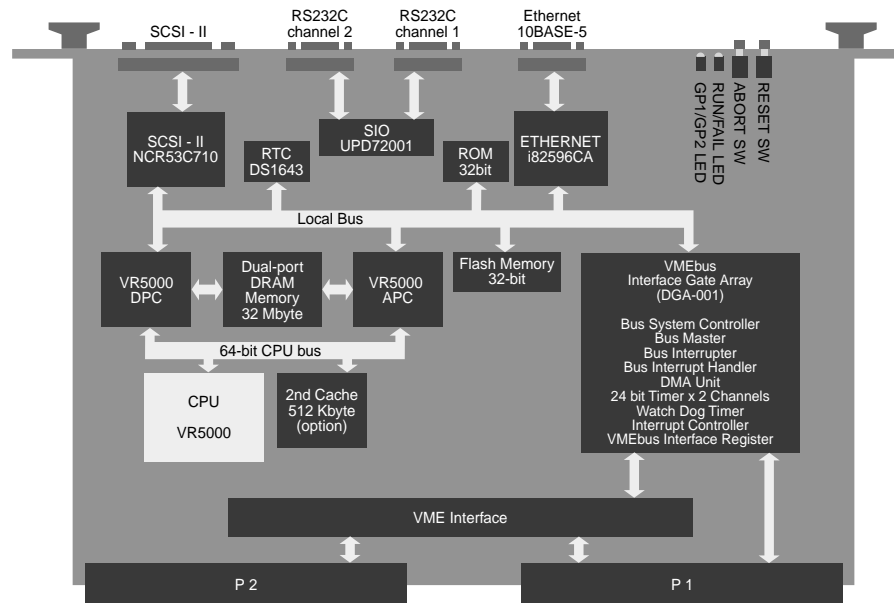
Ethernet Interface

i82596CA and 15-pin AUI connector (10BASE-5)

DENSAN

SCSI - II   RS232C channel 2   RS232C channel 1   Ethernet 10BASE-5

GP1/GP2 LED   RUN/FAIL LED   ABORT SW   RESET SW

SCSI - II NCR53C710   RTC DS1643   SIO UPD72001   ROM 32bit   ETHERNET i82596CA

Local Bus

VR5000 DPC   Dual-port DRAM Memory 32 Mbyte   VR5000 APC   Flash Memory 32-bit

VMEbus Interface Gate Array (DGA-001)

Bus System Controller
Bus Master
Bus Interrupter
Bus Interrupt Handler
DMA Unit
24 bit Timer x 2 Channels
Watch Dog Timer
Interrupt Controller
VMEbus Interface Register

64-bit CPU bus

CPU VR5000   2nd Cache 512 Kbyte (option)

VME Interface

P 2   P 1

Serial Interface (J2 and J3)

µPD72001; two full-duplex RS-232-C interfaces (DCE), 9-SCSI-II Interface (J4)

NCR53C710; 5 MB max. (SCSI spec.) using asynchronous transfer; 10 MB max. (SCSI spec.) using synchronous transfer; 50-pin mini ribbon connector.

Real-Time Clock Plus Battery-Backed RAM

DS1643; 8 KB of SRAM

VMEbus Interface Gate Array

VMEbus system controller; VMEbus master; VMEbus interrupter; VMEbus interrupt handler; DMA unit (between onboard RAM and VMEbus); 24-bit timer x 2 channels; watchdog timer; interrupt controller; VMEbus interface register.

VMEbus Interface

A32/D32 master/slave; A16/D32 slave (interface register); RMW function support; system controller (system clock driver, arbiter, IACK daisy chain driver, bus timer); IH (1 to 7), D08 (O) interrupt handler; ROAK, D08 (O) interrupt.

Operating Conditions

Operating temperature: 0–60°C; relative humidity: 90% max. (noncondensing); cooling requirements: over 1m/sec air flow for forced-air cooling.

Power Consumption

+5 volts: 4.2 A typical; +12 volts: only when an Ethernet interface is used.

Mechanical Specifications

Double-height single-slot VME board; height: 233.35 mm, depth: 160 mm, width: 20 mm (double slot).

Contact List

USA

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DDB-VR4121 Evaluation Board

Salient Features

◗ Optimized for Windows® CE development

◗ Features NEC's highly integrated VR4121™ processor

◗ Includes NEC's VRC4171A™ I/O and color/ monochrome LCD controller

◗ Comes with Windows CE operating system in flash ROM (other OSs are available)

◗ Color LCD and touch-panel interfaces

◗ PS/2 interface for keyboard and mouse

◗ 64 MB DRAM onboard (128 MB maximum)

◗ 32 MB flash memory onboard (64 MB maximum)

◗ Debug board provides three PCI slots, logic analyzer interface connectors

◗ May be used stand-alone or in Compact PCI chassis (not supplied)

◗ Includes design kit CD ROM

CPUs Supported

NEC VR4121

Host Platforms

PC running Windows NT 4.0 and Windows CE Platform Builder, Version 2.12

Product Overview

The DDB-VR4121 is an evaluation board for NEC's VR4121 processor and VRC4171A I/O and LCD Controller companion chip. The board provides a working example of a high-performance/low-cost engine for many Windows CE-based handheld products.

This hardware is designed to evaluate NEC's processor and companion chip capabilities and to serve as a reference design for customers. It is also used as the development platform to develop and test peripheral hardware, device drivers, and software applications. The evaluation board comes preloaded with the Windows CE operating system in flash ROM.

Specifications

• CPU: VR4121

• Companion chip: VRC4171A

• DRAM: 64 MB DIMM in standard socket (128 MB maximum with two DIMM modules

• ROM: 32 MB flash ROM using two Miniature flash memory cards (64 MB maximum)

• PS/2 interface for keyboard and mouse: 83-key scanning keyboard supplied with kit

• LCD panel interface: 640 x 480 for 16-bit color, 800 x 600 for 8-bit color, TFT, DSTN, STN panels

• CRT interface

• Touch-panel interface: Analog 4-line resistive type

• Audio: Microphone input and analog output directly to/from the VR4121

• Connectivity: IrDA (max. 4 Mbps), RS-232-C (max. 115.2 Kbps)

• Ethernet interface: DEC 21143 PCI 10/100 Mbps Ethernet LAN controller

• IDE interface: Standard 40-pin IDE interface supports up to two IDE devices

• Modem interface: Modem interface for daughtercard with analog front end and DAA circuitry

• LED: Two-digit, seven-segment display

• Peripheral daughtercard connectors: All CPU interface signals and PCI signals available on connectors

NEC

System Block Diagram
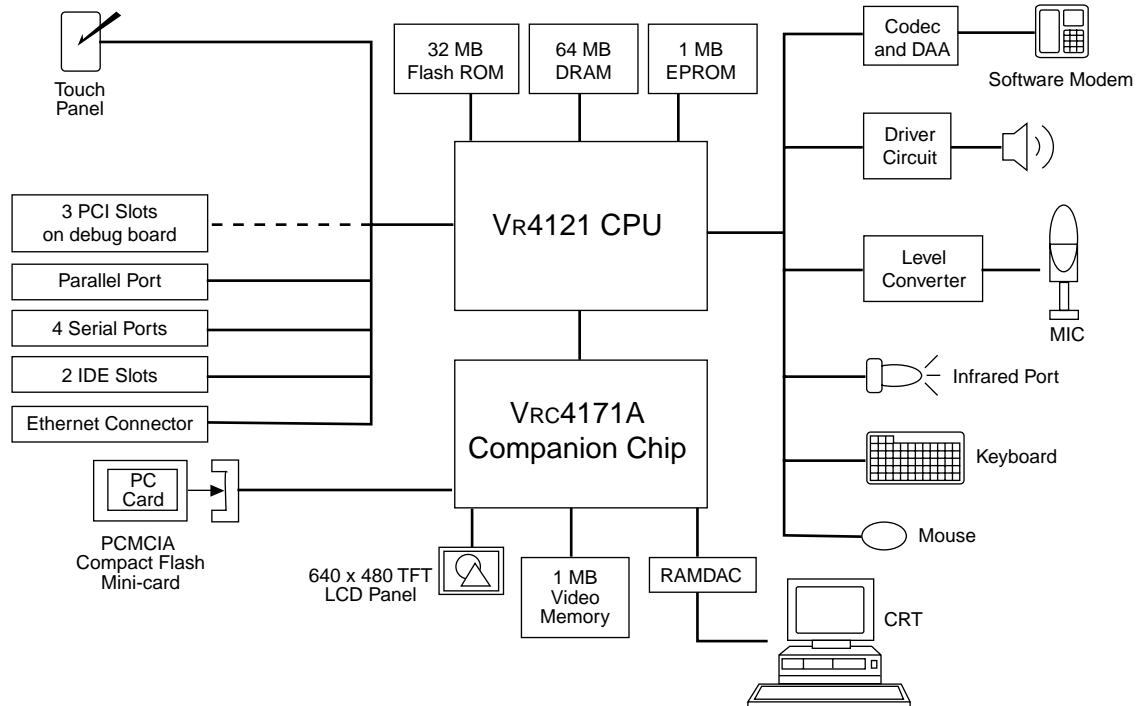
- May be used in stand-alone mode or installed in Compact PCI chassis (not supplied)
- Debug port: TL16PIR552A, one parallel device implemented in FPGA, one serial port
- Power source: +3.3 V, +5 V, +12 V, -12 V from PC ATX power supply

Ordering Information

Part Number	Description
DDB-VR4121S-1	Evaluation kit with color LCD, touchscreen, stand
DDB-VR4121SE-1	Evaluation kit without LCD, touchscreen, stand

Contact List

USA

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DDB-VRC4375 Evaluation Board

Salient Features

◗ High-performance NEC VR4300™ CPU and VRC4375™ support chip

◗ Fast SDRAM memory system

◗ Two PCI 2.1-compliant expansion slots

◗ On board standard IEEE 802.3 100/10-Base Ethernet interface

◗ Real-time clock with 32 KB NVRAM

◗ Two multiprotocol serial interface ports

◗ PMON PROM monitor with extensive diagnostics

◗ VxWorks/Tornado real-time operating system BSP available

CPUs Supported

NEC VR4300, VR4305, VR4310

Host Platforms

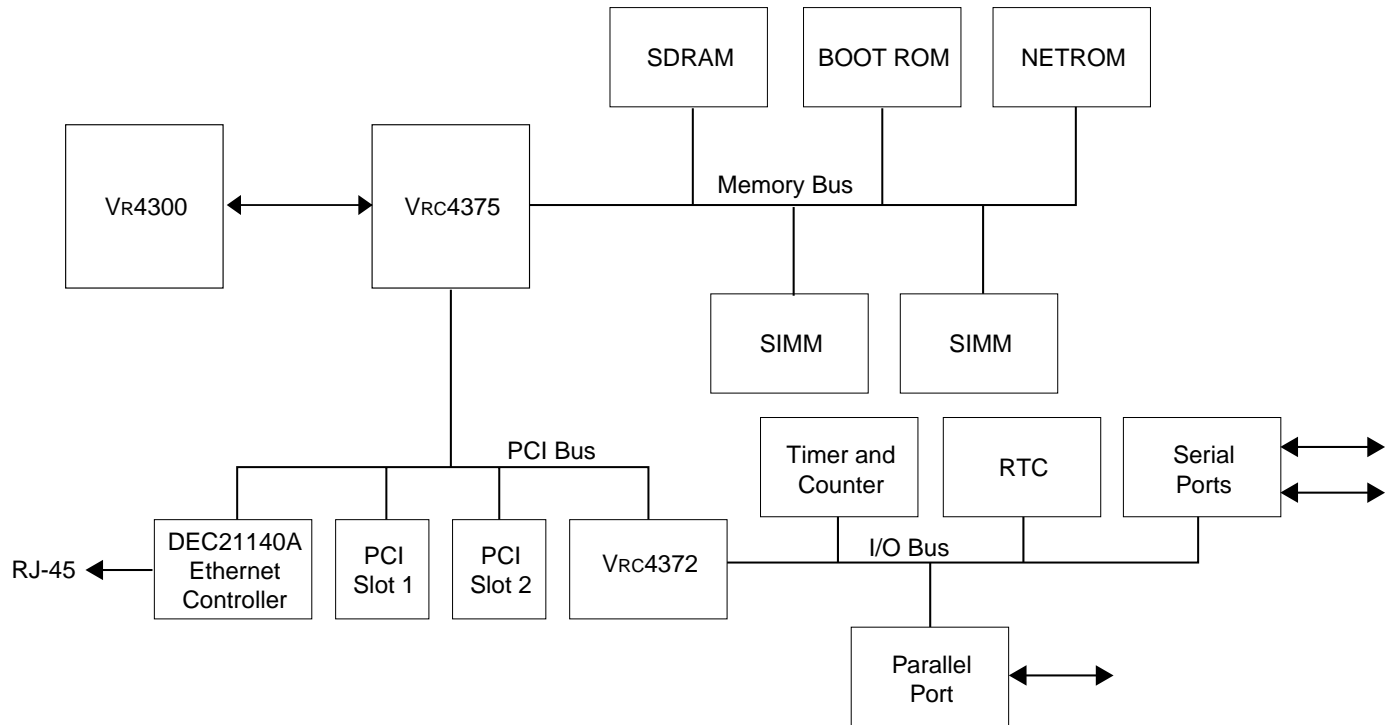PC and UNIX hosts

Product Overview

The DDB-VRC4375 evaluation board is designed as a test bed for all the features of the VRC4375 interface controller, the VRC4372 PCI based I/O controller, as well as the VR4300 microprocessor. It offers the processing power and interfacing capability of a PCI-based evaluation computer.

Hardware Features

• CPU: NEC 64-bit VR4300 133 MHz 2-way superscalar processor, 16 KB on-chip instruction cache and 8 KB on-chip data cache, 32-bit data path, MIPS III instruction set architecture

• Support chips: NEC highly integrated interface controllers VRC4375 and VRC4372
   — The VRC4375 features a glueless interface to the VR4300/VR4305/VR4310 processor family, a memory controller that supports base and SIMM memory, a PCI 2.1-compliant PCI bus controller, a DMA controller able to transfer data blocks from/to any physical address, timers, and a UART.
   — The VRC4372 PCI-based I/O controller features 4 DMA channels, an ISA-like bus, timer, general-purpose I/O, and interrupt controller.

• System bus: 32-bit at 133 MHz

• Memory system: 64 MB base SDRAM memory expandable via two SIMM sockets using memory modules

• PCI expansion: Two PCI edge connector sockets on board, standard 32-bit PCI bus running at 33 MHz

• Ethernet: A DEC 21140 100/10-Base PCI-based Ethernet controller is used to accomplish fast and efficient flow of information between a LAN interface and the PCI bus.

• I/O: Two serial ports implementing the EIA 232 electrical interface for software development and debugging, a bi-directional Centronics-compatible parallel port, connections for PS/2 keyboard and mouse, an RJ-45 connector for Ethernet, a real-time clock, 32 KB nonvolatile memory

• Counter/Timer: Three counter/timers with interrupt capability and a watchdog timer

• Diagnostic display: One 7-segment display for diagnostic and debug messages

• NETROM interface

• Supports PMON PROM monitor, which provides a flexible environment for users to perform debugging. Users can incorporate any of the code from PMON source package into their own products with no redistribution or royalty fees.

NEC

DDB-V$_{RC}$4375 Evaluation Board Block Diagram

- Capable of running VxWorks/Tornado real-time operating system
- Capable of running pSOSystem/pRISM
- Extensive diagnostic programs for self-test
- Operates in both little-endian and big-endian modes

Contact List

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DDB-VRC5074 Evaluation Board
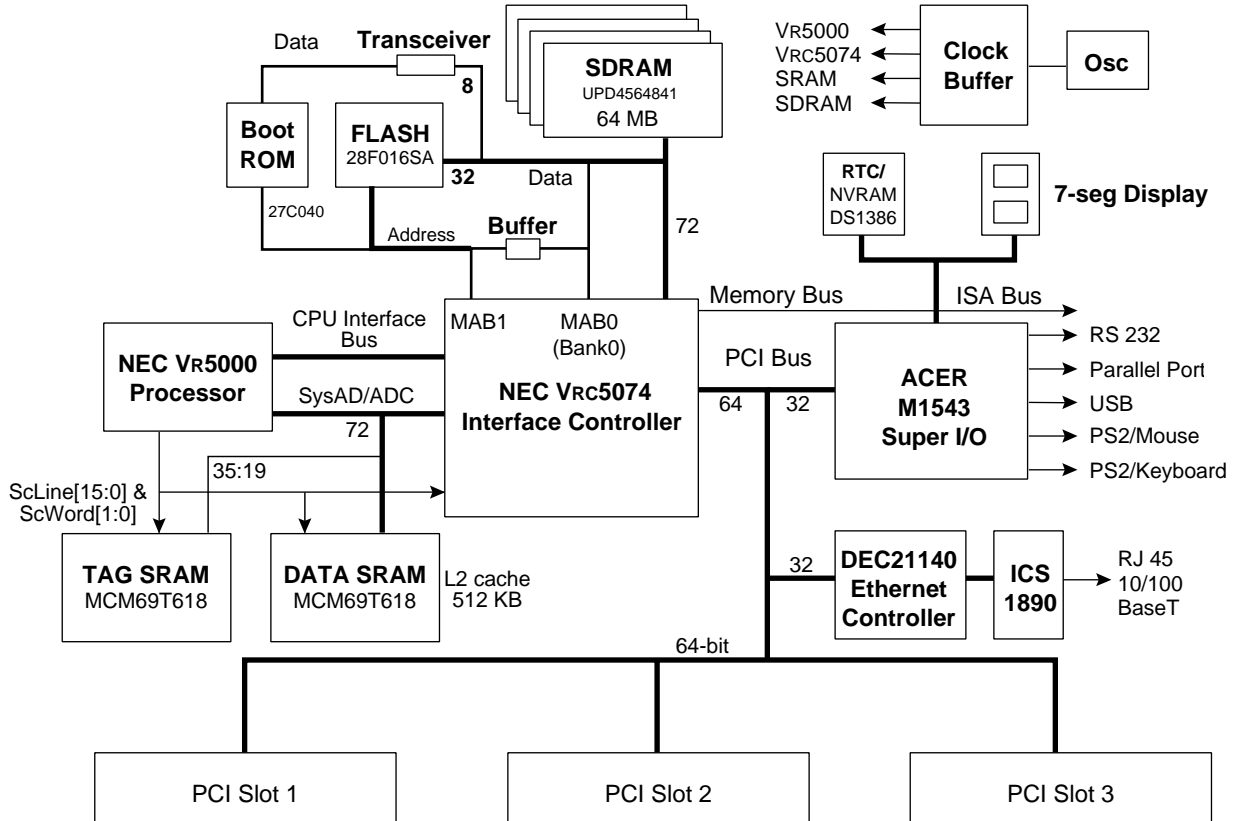
Product Overview

The DDB-VRC5074™ evaluation board is designed as a test bed for all the features of the VRC5074 interface controller, as well as the VR5000 microprocessor. It offers the processing power and interfacing capability of a PCI-based evaluation computer.

Hardware Features

- CPU: NEC 64-bit VR5000 at 200 MHz two-way superscalar processor, 32 KB on-chip instruction cache and 32 KB on-chip data cache, 64-bit data path, MIPS IV instruction set architecture

- Support chip: NEC's highly integrated VRC5074 interface controller features a glueless interface to the VR5000 processor. A memory controller supports two SDRAM banks and one flash memory bank, a PCI 2.1-compliant PCI bus controller, a DMA controller able to transfer data blocks from/to any physical address, an I/O controller with seven programmable device selects, a UART, and timers.

- I/O chip: Acer M1543 super I/O

- Secondary cache: 256 KB/512 KB

- System bus: 64-bit at 100 MHz

- Memory system: 64 MB onboard SDRAM main memory implemented in one memory bank

- PCI expansion: Three PCI edge connector sockets onboard, standard 64-bit PCI bus running at 33 MHz

- Ethernet: A DEC 21140A 100/10-Base PCI-based Ethernet controller is used to accomplish fast and efficient flow of information between a LAN interface and the PCI bus.

- I/O: Two serial ports implementing the EIA 232 electrical interface for software development and debugging, a bidirectional Centronics-compatible parallel port, connections for a PS/2 keyboard and mouse, a USB port and an RJ-45 connector for Ethernet, a real-time clock, 32 KB nonvolatile memory, a watchdog timer, a bus read timeout timer, and counters and timers with interrupt capability

- Diagnostic display: One 7-segment display for diagnostic and debug messages

Salient Features

- High-performance NEC CPU and ASIC support chips

- 512 KB onboard secondary cache

- Fast SDRAM memory system

- Three PCI 2.1-compliant expansion slots

- Onboard standard IEEE-802.3 100/10-Base Ethernet interface

- Real-time clock with 32 KB NVRAM

- Two multiprotocol serial interface ports

- PMON PROM monitor with extensive diagnostics

- VxWorks/Tornado real-time operating system available

CPUs Supported

NEC VR5000

Host Platforms

PC and UNIX hosts

NEC

DDB-VRC5074 Evaluation Board Diagram

Software Support

- Supports PMON PROM monitor, which provides a flexible environment for users to perform debugging; users can incorporate any of the code from the PMON source package into their own products with no redistribution or royalty fees
- Capable of running pSOSystem/pRISM
- Capable of running VxWorks/Tornado real-time operating system
- Extensive diagnostic programs for self-test
- Operates in bi-endian mode

Contact List

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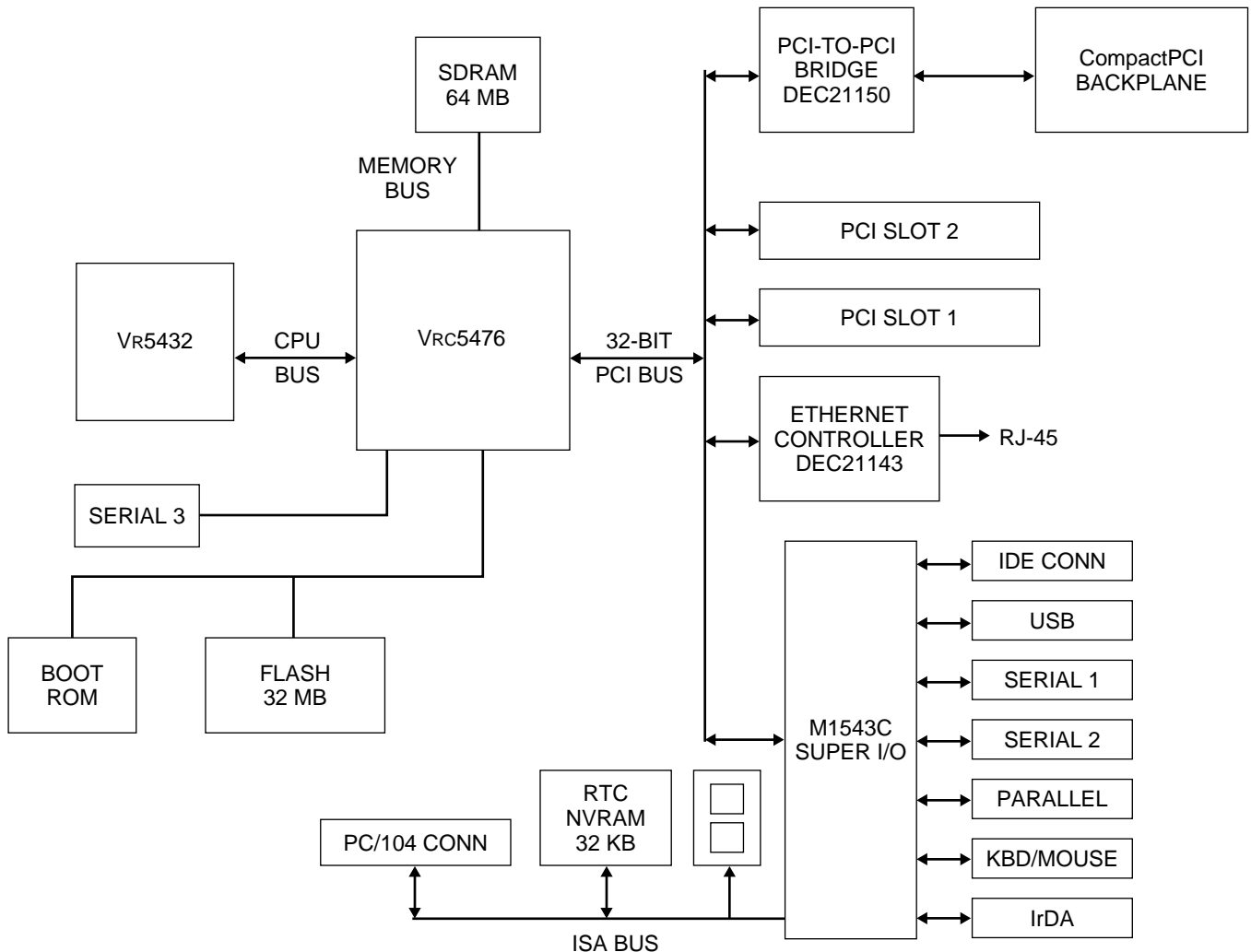
DDB-VRC5476 Evaluation Board

Product Overview

The DDB-VRC5476 evaluation board is designed as a test bed for all the features of theVR5432 processor as well as the features of the VRC5476 interface controller. It offers the processing power and interfacing capability of a PCI-based evaluation computer in a CompactPCI form factor.

Hardware Features

- CPU: NEC 64-bit VR5432 at 133 MHz two-way superscalar processor, 32 KB on-chip instruction cache and 32 KB on-chip data cache, 32-bit data path, MIPS IV instruction set architecture

- Support chip: NEC's highly integrated VRC5476 interface controller features a glueless interface to the VR5432 processor. A memory controller supports SDRAM and flash memory, a PCI 2.1-compliant bus controller, a four-channel DMA controller able to transfer data blocks from/to any physical address, an I/O controller with five programmable device chip selects, a UART, and timers.

- I/O chip: Acer M1543C Super I/O

- System bus: 32-bit at 133 MHz

- Memory system: 64 MB onboard SDRAM and 32 MB flash memory

- PCI expansion: Two PCI edge connector sockets onboard, standard 32-bit PCI bus running at 33 MHz

- Ethernet: A DEC21143 100/10-Base PCI-based Ethernet controller is used to accomplish fast and efficient flow of information between a LAN interface and the PCI bus.

- I/O: Three serial ports implementing the EIA 232 electrical interface for software development and debugging, a bidirectional Centronics-compatible parallel port, connections for PS/2 keyboard and mouse, an IDE interface, an IrDA-compliant infrared connector, an RJ-45 connector for Ethernet, a real-time clock, and 32 KB of nonvolatile memory

- Counter/Timer: Three counter/timers with interrupt capability and a watchdog timer

- Diagnostic display: One 7-segment display for diagnostic and debug messages

- CompactPCI system slot board with arbitration support for 7 PCI masters

- JTAG with N-Wire and N-Trace debug support

Salient Features

◗ High-performance NEC CPU and ASIC support chips

◗ Fast SDRAM memory system

◗ Two PCI 2.1-compliant expansion slots

◗ Onboard standard IEEE-802.3 100/10-Base Ethernet interface

◗ Real-time clock with 32 KB NVRAM

◗ Three multiprotocol serial interface ports

◗ CompactPCI® form factor and interface

◗ PMON PROM monitor with extensive diagnostics

◗ VxWorks/Tornado real-time operating system available

CPUs Supported

NEC VR5432

Host Platforms

PC and UNIX hosts

NEC

DDB-VRC5476 Evaluation Board Diagram

DDB-VRC5476 Evaluation Board Diagram

Block diagram showing: SDRAM 64 MB connected via MEMORY BUS to VRC5476. VR5432 connected to VRC5476 via CPU BUS. VRC5476 connected via 32-BIT PCI BUS to PCI-TO-PCI BRIDGE DEC21150 (which connects to CompactPCI BACKPLANE), PCI SLOT 2, PCI SLOT 1, ETHERNET CONTROLLER DEC21143 (to RJ-45), and M1543C SUPER I/O. SERIAL 3, BOOT ROM, FLASH 32 MB also connected to VRC5476. ISA BUS connects PC/104 CONN, RTC NVRAM 32 KB, and M1543C SUPER I/O. M1543C SUPER I/O connects to IDE CONN, USB, SERIAL 1, SERIAL 2, PARALLEL, KBD/MOUSE, IrDA.

Software Support

- Supports PMON PROM monitor, which provides a flexible environment for users to perform debugging; users can incorporate any of the code from the PMON source package into their own products with no redistribution or royalty fees
- Capable of running pSOSystem/pRISM
- Capable of running VxWorks/Tornado real-time operating system
- Extensive diagnostic programs for self-test
- Operates in both little-endian and big-endian modes

Contact List

USA

VR Series RISC Products Group
NEC Electronics Inc.
2880 Scott Boulevard
Santa Clara, CA 95054
Tel: (800) 366-9782 or (408) 588-6000
E-mail: vrsupport@el.nec.com

Japan

NEC Corporation
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Kawasaki, Kanagawa 211, Japan
Tel: +88-44-435-1485

QuickPrint® Evaluation Board for VR5432

Salient Features

The controller is based on the NEC VR5432 processor and the Peerless banding coprocessor. The controller operates at a bus clock rate of 66.666 MHz. The main features of the controller are shown below.

◗ NEC VR5432 processor operating at 66.666 MHz bus rate and 167 MHz CPU rate

◗ Peerless banding coprocessor/graphics accelerator providing the following functions:
- ROM control
- I/O control
- SDRAM control
- Printer video interface
- Printer communications interface
- Sense of time support
- Interrupt control
- IEEE-1284 parallel port

◗ Controller memory
- 8 MB of onboard page mode interleaved flash ROM
- Two 72-pin ROM SIMM connectors supporting 4/8/16 MB ROM/flash/OTP
- 4096-bit serial EEPROM
- Two 168-pin SDRAM DIMM connectors supporting array sizes of 4 to 256 MB of SDRAM each

◗ Controller I/O ports
- IEEE-1284-compliant bidirectional parallel port
- One 16-bit PSIO card interface (for NIC options)
- Onboard IDE hard disk interface
- Video connector to support different types of Printers

◗ Print engine interfaces
- SP-A410/SP-411—Monochrome, 600 x 600 dpi, 35 ppm
- Generic 100-pin video interface connector

◗ Debug facilities
- Diagnostic LEDs and test points
- JTAG connector
- Debug connectors, used for the QP1910 signals
- Peerless monitor debug connector
- Reset switch

CPUs Supported

NEC VR5432

Product Overview

The QP1910 is a high-performance 32-bit graphic banding coprocessor. It provides the NEC VR5432 processor with a powerful graphics accelerator and compression coprocessor that dramatically increases system performance and reduces printer controller system cost. The coprocessor provides all the necessary system control for the processor, and a direct interface to the laser print engine with the following features:

- Direct connection to four ROM banks
- Direct connection to three SDRAM DIMMs
- Direct connection to eight I/O banks
- IEEE-1284-compatible parallel port interface
- Serial port interface
- Direct printer video and communication interface

The QP1910 integrates all elements required for a page printer system, including a DRAM controller, ROM controller, I/O controller, IEEE-1284 parallel port interface with DMA, serial port with FIFO, and print engine communication. In addition, the QP1910 uniquely combines these features with two powerful logic units tailored for page printer systems: the Graphics Execution Unit (GEU) and the Print Engine Video Controller (PVC).

PEERLESS
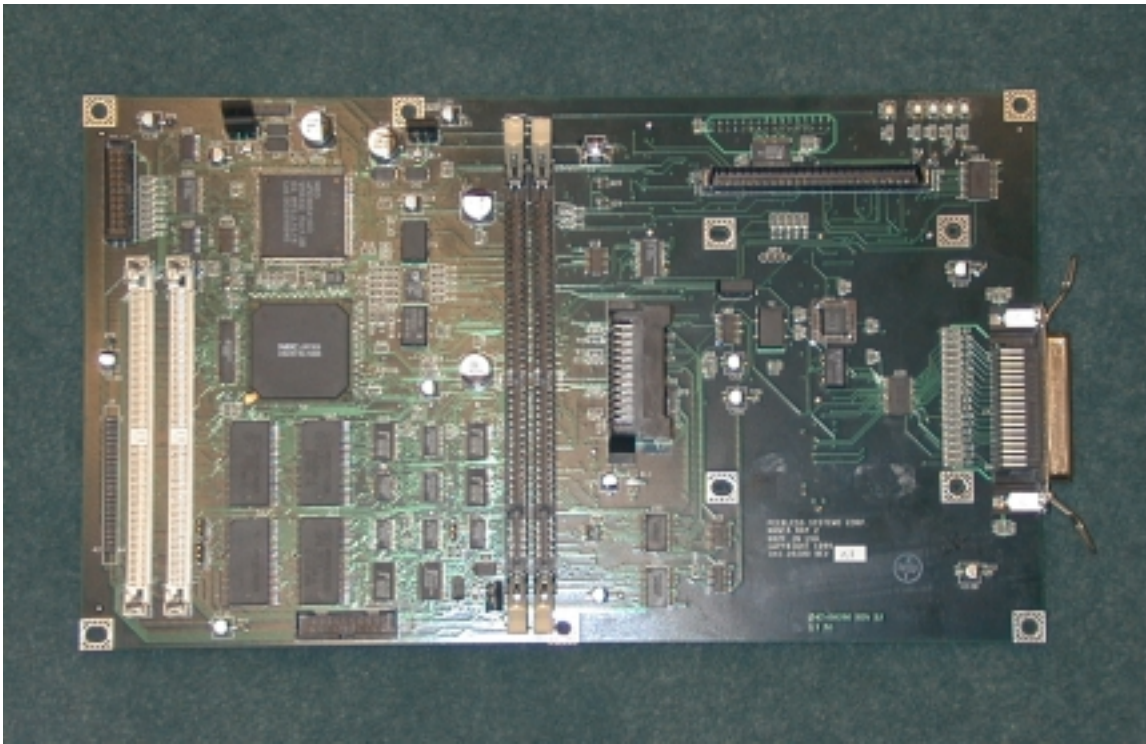
Contact List

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*Memory Reduction Technology (MRT) and QuickPrint are
registered trademarks of Peerless Systems Corporation.*

Preprocessors/Logic Analyzers/ Logic Scope

Agilent Technologies 16700A Series Logic Analysis System

Salient Features

⬧ Intuitive, easy-to-use multiwindow interface

⬧ Multiple time-correlated views of data for analog signal to source code execution

⬧ Integral emulation modules coupled with debuggers and real-time analysis help bring hardware and software together

⬧ Inverse assembler for MIPS processors helps debug code execution in real time

⬧ Available state, timing, oscilloscope, pattern generation, and emulation modules for correlating measurements to discover cause/effect relationships

⬧ Support for over 200 microprocessors, microcontrollers, and embedded core processors

CPUs Supported

NEC VR Series MIPS processors

Host Platforms Supported

Windows 95/NT

Product Overview

The Agilent Technologies 16700A series logic analysis systems offer the power of combined logic analysis and emulation in a simple, cost-effective package. With a large color display, on-screen setup assistant, and intuitive user interface, your design team can finally work together to find and solve the toughest problems. In addition, an emulator module and scope or pattern generator may be added. For a fully modular solution with up to 10 measurement modules supporting over 1000 channels and 4 emulation modules, you can use the 16700A logic analysis system with the 16701A expansion module.

Key Features

The Agilent Technologies 16700A series logic analysis systems share an intuitive, easy-to-use multiwindow interface and common capabilities. A large display with multiple sizeable windows allows you to see at a glance more of your target system's operation. Color lets you highlight critical information so you can find it quickly. Web-enabled logic analysis makes it easy to work remotely. Multiple time-correlated views of data let you examine target operation from different perspectives, to confirm both signal integrity and software execution flow with one tool. This is invaluable in solving cross-domain problems. On-chip emulation for many popular microprocessors together with links to debuggers help you bring hardware and software together into a working system more quickly than with conventional digital debug tools.
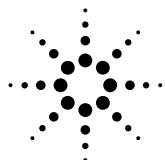
Agilent Technologies
Innovating the HP Way

Solutions for Digital System Debug

Configure a System with the Modules You Need

Most Agilent Technologies 16500 measurement modules are also compatible with the 16700 mainframes. All mainframes support the following acquisition modules.

Oscilloscope

Agilent Technologies offers a 500 MHz/2 gigasample per second (GSa/s) module and a 250 MHz/1 GSa/s module. Both have two channels and a 32 KB memory depth. You can use the logic analyzer to trigger the scope at the precise moment necessary to identify a possible ground bounce, metastability, or cross-talk problem.

State/Timing

Agilent Technologies offers a wide variety of state/ timing modules to help you match your tools to your specific measurement needs.

High-Speed Timing

To help you verify even the most demanding timing requirements, you can get up to 4 GSa/s and 128 KB with built-in setup and hold time violation triggering.

Pattern Generation

Agilent Technologies' 200-M vectors/sec, 40-channel module with 256 KB of memory for stimulus can substitute for missing system components or provide a stimulus-response test environment.

Postprocessing Tool Sets Help You Integrate Hardware and Software

When you want to really understand what your target is doing and why, you need to be able to view software execution results in the context of specific hardware events. Agilent Technologies' optional tool sets are available to assist in the processing of captured analysis data.

Source Correlation Tool Set

You can correlate a logic analyzer trace with the source code that produced it and set up the logic analyzer trigger by simply pointing and clicking on a source line. This tool helps you debug your code when you cannot or choose not to halt the microprocessor.

System Performance Analysis Tool Set

You can profile and analyze system performance to uncover bottlenecks in the software or hardware elements within your target.

Serial Analysis Tool Set

This tool lets you acquire and analyze serial data streams to debug problems in peripheral communications.

On-Chip Emulation Tools Make Fixing Bugs Easier

For specific microprocessor families that feature on-chip emulation, you can add a processor emulation module to connect the onboard debugging resources of the micro-processor to the logic analyzer and to a high-level debugger.

Integrated Debugger Support

Agilent Technologies offers you unprecedented visibility into software execution for systems running software written in C and C++. You can achieve the functionality of a full-featured emulator by using a third-party debugger which drives the installed HP emulation module. This gives you active and complete microprocessor run control.

Speed Problem Solving With Off-the-Shelf Solutions for Many Common Microprocessors

Analysis probes are available for over 200 microprocessors and microcontrollers. Bus probes allow probing of popular bus architectures such as PCI, USB, VXI, SCSI, and many others.

Contact List

USA

Agilent Technologies
Test and Measurement Call Center
P.O. Box 4026
Englewood, CO 80155-4026
Tel: (800) 452-4844
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Canada

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5150 Spectrum Way
Mississauga, Ontario
L4W 5G1
Tel: (877) 894-4414

Technical data is subject to change.

PI-VR4000 Logic Analysis Probe

Product Overview

The PI-VR4000/4400 logic analysis probe provides a complete interface between any VR4000/4400 target system and the HP16500, HP1660, HP1670, HP16600, or HP16700 family of logic analyzers. The PI-VR4000/4400 configuration software on a flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessor. It also loads the inverse assembler (disassembler) for obtaining displays of the processor data in assembly language mnemonics. The PI-VR4000/4400 logic analysis probe is a nonintrusive development tool and provides a powerful environment for debugging both hardware and software real-time applications.

Description

The PI-VR4000/4400 logic analysis probe is a specialized module that provides a convenient interface between the HP16500, HP1660, HP1670, HP16600, and HP16700 family of logic analyzers and a VR4000/4400 target system.

The PI-VR4000/4400 logic analysis probe is installed directly on the target board and the VR4000/4400 processor is installed into the PGA socket on the preprocessor. The logic analyzer pods, with HP 01650-63203 termination adapters, plug directly onto the mating Mictor connectors on the PI-VR4000/4400 logic analysis probe and provide tracing and monitoring of the processor signals. The signals are grouped in a logical order so that the HP logic analyzer configured with the disassembler software can display bus activity in mnemonic form. In addition to the mnemonic disassembly, the logic analyzer displays all the bus activity with the relevant status information. The preprocessor supports the 179-pin PGA chip package.

Hewlett-Packard logic analyzers are part of an integrated family of design and development tools. Many different models are available and include networking capability, oscilloscope add-ons, the ability to display high-level source code, and many other features. Please see your local Hewlett-Packard sales representative for additional information.

Salient Features

◗ Compatible with VR4000/4400 processors

◗ Complete mnemonic disassembly

◗ Display of cycle status information, including identification of instruction fetch and operand read/write codes

◗ Quick and easy connection of logic analyzer pods to a VR4000/4400 target system

◗ Low-capacitance probing

◗ Setup and data storage on built-in logic analyzer disk drive

◗ Trace data hard copy available via RS-232 serial port

◗ Multilayer, low-noise PCB construction with ground and power planes

CPUs Supported

NEC VR4000, VR4400

CORELIS

Specifications

Logic Analyzer Required

Hewlett-Packard HP16500, HP1660, HP1670, HP16600, or HP16700 family of analyzers

Maximum Acquisition Speed

50 MHz

Signal Line Loading

20 pF @ 100 KOhms

Number of Pods Required

The PI-VR4000/4400 requires eight sixteen-channel probes for complete state disassembly.

Package Supported

Supports the 179-pin PGA package

Included

- PI-VR4000/4400 logic analysis probe
- Disassembler and configuration software diskette
- Operating manual

Contact List

USA

Corelis, Inc.
12607 Hiddencreek Way, Suite H
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PI-VR4100 Logic Analysis Probe

Product Overview

The PI-VR4100 logic analysis probe provides a complete interface between any VR4100 target system and the HP16500, HP1660, HP1670, HP16600, or HP16700 family of logic analyzers. The PI-VR4100 configuration software on a flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessor. It also loads the inverse assembler (disassembler) for obtaining displays of the processor data in assembly language mnemonics. The PI-VR4100 logic analysis probe is a nonintrusive development tool and provides a powerful environment for debugging both hardware and software real-time applications.

Description

The PI-VR4100 logic analysis probe is a specialized module that provides a convenient interface between the HP16500, HP1660, HP1670, HP16600, and HP16700 family of logic analyzers and a VR4100 target system.

The PI-VR4100 logic analysis probe is installed directly on the target board and the VR4100 processor is installed into the PGA socket on the preprocessor. The logic analyzer pods, with HP 01650-63203 termination adapters, plug directly onto the mating Mictor connectors on the PI-VR4100 logic analysis probe and provide tracing and monitoring of the processor signals. The signals are grouped in a logical order so that the HP logic analyzer configured with the disassembler software can display bus activity in mnemonic form. In addition to the mnemonic disassembly, the logic analyzer displays all the bus activity with the relevant status information. The preprocessor supports the 100-pin TQFP chip package.

Hewlett-Packard logic analyzers are part of an integrated family of design and development tools. Many different models are available and include networking capability, oscilloscope add-ons, the ability to display high-level source code, and many other features. Please see your local Hewlett-Packard sales representative for additional information.

Salient Features

- Compatible with NEC VR4100 RISC embedded processor chips

- Complete VR4100 mnemonic disassembly

- Display of cycle status information, including identification of memory, I/O, and burst addresses

- Quick and easy connection of logic analyzer pods to a VR4100 target system

- Low-capacitance probing

- Setup and data storage on built-in logic analyzer disk drive

- Trace data hard copy available via RS-232 serial port

- Multilayer, low-noise PCB construction with ground and power planes

CPUs Supported

NEC VR4100

CORELIS

Specifications

Logic Analyzer Required

Hewlett-Packard HP16500, HP1660, HP1670, HP16600, or HP16700 family of analyzers

Maximum Acquisition Speed

The maximum acquisition speed is limited only by the speed of the logic analyzer.

Signal Line Loading

20 pF @ 100 KOhms

Number of Pods Required

The PI-VR4100 requires four sixteen-channel probes for complete state disassembly.

Package Supported

Supports the 100-pin TQFP package

Included

- PI-VR4100 logic analysis probe
- Disassembler and configuration software diskette
- Operating manual

Contact List

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PI-VR43xx
Logic Analysis Probe

Salient Features

◗ Compatible with NEC VR43xx RISC embedded processor chips

◗ Complete VR43xx mnemonic disassembly

◗ Display of cycle status information including identification of memory, I/O, and burst addresses

◗ Quick and easy connection of logic analyzer pods to a VR43xx target system

◗ Low-capacitance probing

◗ Setup and data storage on built-in logic analyzer disk drive

◗ Trace data hard copy available via RS-232 serial port

◗ Multilayer, low-noise PCB construction with ground and power planes

CPUs Supported

NEC VR43xx

Product Overview

The PI-VR43xx logic analysis probe provides a complete interface between any VR43xx target system and the HP16500, HP1660, HP1670, HP16600, or HP16700 family of logic analyzers. The PI-VR43xx configuration software on a flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessor. It also loads the inverse assembler (disassembler) for obtaining displays of the processor data in assembly language mnemonics. The PI-VR43xx logic analysis probe is a nonintrusive development tool and provides a powerful environment for debugging both hardware and software real-time applications.

Description

The PI-VR43xx logic analysis probe is a specialized module that provides a convenient interface between the HP16500, HP1660, HP1670, HP16600, and HP16700 family of logic analyzers and a VR43xx target system.

The PI-VR43xx logic analysis probe is installed directly on the target board and the VR43xx processor is installed into the PGA socket on the preprocessor. The logic analyzer pods, with HP 01650-63203 termination adapters, plug directly onto the mating Mictor connectors on the PI-VR43xx logic analysis probe and provide tracing and monitoring of the processor signals. The signals are grouped in a logical order so that the HP logic analyzer configured with the disassembler software can display bus activity in mnemonic form. In addition to the mnemonic disassembly, the logic analyzer displays all the bus activity with the relevant status information. The preprocessor supports the 120-pin PQFP chip package.

Hewlett-Packard logic analyzers are part of an integrated family of design and development tools. Many different models are available and include networking capability, oscilloscope add-ons, the ability to display high-level source code, and many other features. Please see your local Hewlett-Packard sales representative for additional information.

CORELIS

Specifications

Logic Analyzer Required

Hewlett-Packard HP16500, HP1660, HP1670, HP16600, or HP16700 family of analyzers

Maximum Acquisition Speed

The maximum acquisition speed is limited only by the speed of the logic analyzer.

Signal Line Loading

20 pF @ 100 KOhms

Number of Pods Required

The PI-VR43xx requires four sixteen-channel probes for complete state disassembly.

Package Supported

Supports the 120-pin PQFP package

Included

- PI-VR43xx logic analysis probe
- Disassembler and configuration software diskette
- Operating manual

Contact List

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Fax: +81-3-3724-2198
E-mail: h-kawano@rentec.orix.co.jp

PI-VR5000
Logic Analysis Probe

Salient Features

◗ Complete VR5000 mnemonic disassembly

◗ Setup and data storage on built-in logic analyzer disk drive

◗ Trace data hard copy available via RS-232 serial port

◗ Multilayer, low-noise PCB construction with ground and power planes

◗ Provides complete visibility for all address, data, status, and control lines

◗ Compatible with HP16505 prototype analyzer

◗ Adds real-time trace to VR5000 software debug for complete development solution

◗ Channel configuration assignment compatible with user target board

CPUs Supported

NEC VR5000

Product Overview

The PI-VR5000 logic analysis probe provides a complete interface between any VR5000 target system and the HP16500, HP1660, HP1670, HP16600, or HP16700 family of logic analyzers. The PI-VR5000 configuration software on a flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessor. It also loads the inverse assembler (disassembler) for obtaining displays of the processor data in assembly language mnemonics. The PI-VR5000 logic analysis probe is a nonintrusive development tool and provides a powerful environment for debugging both hardware and software real-time applications.

Description

The PI-VR5000 logic analysis probe is a specialized module that provides a convenient interface between the HP16500, HP1660, HP1670, HP16600, and HP16700 family of logic analyzers and a VR5000 target system.

The PI-VR5000 logic analysis probe is installed directly on the target board and the VR5000 processor is installed into the PGA socket on the preprocessor. The logic analyzer pods provide tracing and monitoring of the processor signals. The signals are grouped in a logical order so that the HP logic analyzer configured with the disassembler software can display bus activity in mnemonic form. In addition to the mnemonic disassembly, the logic analyzer displays all the bus activity with the relevant status information. The preprocessor supports the 223-pin PGA chip package.

Hewlett-Packard logic analyzers are part of an integrated family of design and development tools. Many different models are available and include networking capability, oscilloscope add-ons, the ability to display high-level source code, and many other features. Please see your local Hewlett-Packard sales representative for additional information.

CORELIS

Example of a Disassembled Trace

```
( 100/500MHz LA A )  ( Listing 1 )  ( Invasm )  ( Cancel )  ( Run )

 Markers          Acquisition Time
  Off         09 Jun 1997 15:49:56

 Label>   ADDR         MIPS BE 5000 Disassembly A4.2        STAT
 Base>    Hex     A[7:0]      Mnemonic                     Symbol

   0    1FC1F600  00  BEQ        v00,r00,1FC1F668    8 BYTE READ
                  04  SD         ra,0030(sp)
   1    1FC1F600          Wait...                     8 BYTE READ
   2    1FC1F600          Wait...                     8 BYTE READ
   3    1FC1F600          Wait...                     8 BYTE READ
   4    1FC1F600          Wait...                     8 BYTE READ
   5    1FC1F600          Wait...                     8 BYTE READ
   6    FFBF0030        opcode read                   DATA TRANSFE
   7    1FC1F668  68  LUI        at,A000             8 BYTE READ
                  6C  SW         s00,1A48(at)
   8    AC301A48        opcode read                   DATA TRANSFE
   9    0000E050  50  Data Write FFFFFFFF BFC1F698    8 BYTE WRITE
  10    BFC1F698        data write                    DATA TRANSFE
  11    00001A48  48  Data Write 00000007 --------    4 BYTE WRITE
  12    00000000        data write                    DATA TRANSFE
  13    00001A48  48  Data Write 00000007 --------    4 BYTE WRITE
```

Specifications

Logic Analyzer Required

Hewlett-Packard HP16500, HP1660, HP1670, HP16600, or HP16700 family of analyzers

Maximum Acquisition Speed

The maximum acquisition speed is limited only by the speed of the logic analyzer.

Signal Line Loading

20 pF @ 100 KOhms

Number of Pods Required

The PI-VR5000 requires six sixteen-channel probes for complete state disassembly.

Package Supported

Supports the 223-pin PGA package

Included

- PI-VR5000 logic analysis probe
- Disassembler and configuration software diskette
- Operating manual

Contact List

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PI-VR5432
Logic Analysis Probe

Salient Features

◗ Compatible with NEC VR5432 processor chips

◗ Supports the 208-pin PQFP package

◗ Complete MIPS mnemonic disassembly

◗ Compatible with the HP B4620B software analysis package

◗ Display of a complete bus cycle per line for maximum trace visibility

◗ Quick and easy connection of logic analyzer pods to the target system

◗ Low-capacitance probing

◗ Setup and data storage on built-in logic analyzer disk drive

◗ Trace data hard copy available

◗ Multilayer, low-noise PCB construction with ground and power planes

CPUs Supported

NEC VR5432

Product Overview

The PI-VR5432 logic analysis probe provides a complete interface between any VR5432 target system and the HP16500, HP1660, HP1670, HP16600, or HP16700 family of logic analyzers. The PI-VR5432 configuration software on a flexible disk sets up the format specification menu of the logic analyzer for compatibility with the microprocessor. It also loads the inverse assembler (disassembler) for obtaining displays of the processor data in assembly language mnemonics. The PI-VR5432 logic analysis probe is a nonintrusive development tool and provides a powerful environment for debugging both hardware and software real-time applications.

Description

The PI-VR5432 logic analysis probe is a specialized module that provides a convenient interface between the HP16500, HP1660, HP1670, HP16600, and HP16700 family of logic analyzers and a VR5432 target system.

The PI-VR5432 logic analysis probe is installed directly on the target board via a PQFP clip that attaches to the top of the processor. The logic analyzer pods, with HP E5436A termination adapters, plug directly onto the mating Mictor connectors on the PI-VR5432 logic analysis probe and provide tracing and monitoring of the processor signals. The signals are grouped in a logical order so that the HP logic analyzer configured with the disassembler software can display bus activity in mnemonic form. In addition to the mnemonic disassembly, the logic analyzer displays all the bus activity with the relevant status information. The preprocessor supports the 208-pin PQFP chip package.

Hewlett-Packard logic analyzers are part of an integrated family of design and development tools. Many different models are available and include networking capability, oscilloscope add-ons, the ability to display high-level source code, and many other features. Please see your local Hewlett-Packard sales representative for additional information.

CORELIS

Specifications

Logic Analyzer Required

Hewlett-Packard HP16500, HP1660, HP1670, HP16600, or HP16700 family of analyzers

Maximum Acquisition Speed

100 MHz

Signal Line Loading

20 pF @ 100 KOhms

Number of Pods Required

The PI-VR5432 requires six sixteen-channel probes for complete state disassembly.

Package Supported

Supports the 208-pin PQFP package

Included

- PI-VR5432 logic analysis probe
- Disassembler and configuration software diskette
- Operating manual

Contact List

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NEC VR Series Processors– Tektronix Logic Analyzer Probing Support

Salient Features

◗ Support for probing VR4100, VR4300, VR4310, VR5000, and VR5432 processors

◗ VR4100, VR43xx, and VR5432 support includes SMT adapter, probe adapter, and disassembler

◗ VR5000 support includes disassembler

◗ Acquire signal timing behavior to 0.5 ns resolution on all channels

◗ Acquire synchronous bus behavior to 200 MHz

◗ Perform state and timing acquisition simultaneously through a single set of probes

◗ Trigger acquisitions on signal and bus situations of interest

◗ View acquisitions as timing, state, and/or disassembly displays

◗ Symbolic display of address labels

◗ Multilayer SMT adapter and probe adapter PCBs with power and ground planes

◗ Capacitive loading as low as 2 pF

CPUs Supported

VR4100, VR43xx, and VR5xxx

Host Platforms

DAS9200, TLA5xx, TLA6xx, and TLA7xx logic analyzers

Support From The Ground Up

And not only the ground, but all of the other connections of your NEC VR Series processors!

Probing of VR4100 and VR43xx processors starts with a processor-specific SMT adapter which clips onto the QFP chip, allowing you to probe your existing designs without having to dedicate PCB real estate for debug connectors.
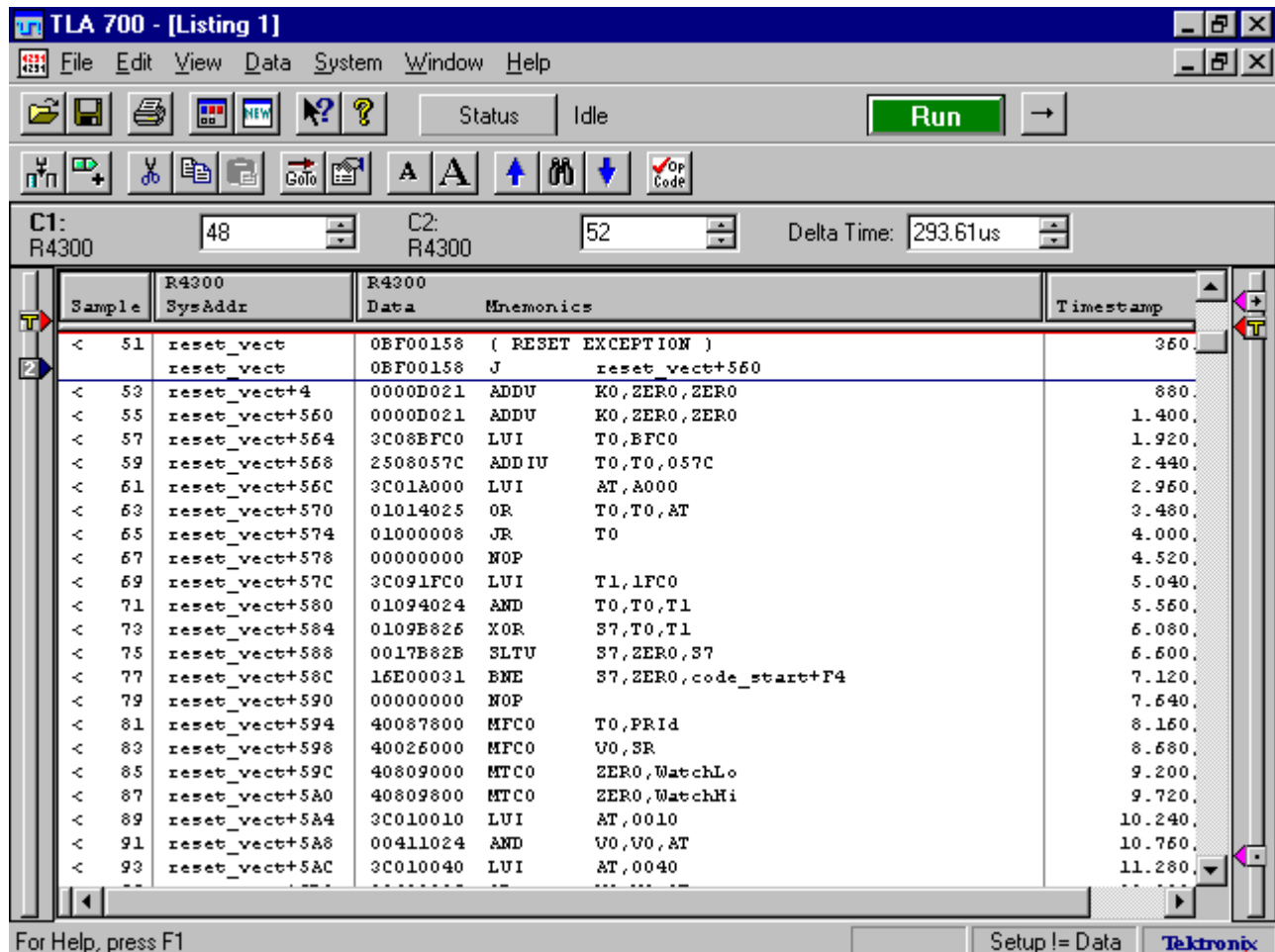
Connection of the logic analyzer probes happens at the probe adapter, which mounts on the top side of the SMT adapter.

Support software configures the logic analyzer acquisition channels and names them. Hardware development and debug benefits from the timing display, which shows high-speed asynchronous signal behavior.

Software development and debug benefits from the disassembly software, which runs on the logic analyzer and provides a mnemonic instruction display of the instruction stream fetched by the processor.

Optimal low-capacitance probing (as low as 2 pF per signal connection) of the VR5xxx high-performance bus may be accomplished by mounting on your PCB high-density Mictor (trademark of AMP, Inc.) connectors, to which the logic analyzer probes can mate. Probing of VR5xxx buses operating beyond 100 MHz can be accomplished reliably.

Our configuration and disassembly software provides full support for monitoring the signals of the external cache of the VR5000 and for decoding all bus transactions.

CRESCENT HEART SOFTWARE

```
TLA 700 - [Listing 1]                                                    _  ₧  ✕
    File  Edit  View  Data  System  Window  Help                         _  ₧  ✕

  ⌂ 🖫 🖨  ▦ NEW  ▧? ?      Status    Idle                    Run    →

  ▯▯ ▯▯  ✂ 🖹 📋  🔁 🖻  A A  ↑ 🔍 ↓  ✓Op
                                                                  Code

 C1:                    48    ↕      C2:        52    ↕    Delta Time: 293.61us  ↕
 R4300                                R4300

         R4300                 R4300
    Sample  SysAddr           Data      Mnemonics                    Timestamp

 <     51  reset_vect         0BF00158  ( RESET EXCEPTION )              360.
           reset_vect         0BF00158  J        reset_vect+560
 <     53  reset_vect+4       0000D021  ADDU     K0,ZERO,ZERO            880.
 <     55  reset_vect+560     0000D021  ADDU     K0,ZERO,ZERO         1.400.
 <     57  reset_vect+564     3C08BFC0  LUI      T0,BFC0             1.920.
 <     59  reset_vect+568     2508057C  ADDIU    T0,T0,057C          2.440.
 <     61  reset_vect+56C     3C01A000  LUI      AT,A000             2.960.
 <     63  reset_vect+570     01014025  OR       T0,T0,AT            3.480.
 <     65  reset_vect+574     01000008  JR       T0                  4.000.
 <     67  reset_vect+578     00000000  NOP                          4.520.
 <     69  reset_vect+57C     3C091FC0  LUI      T1,1FC0             5.040.
 <     71  reset_vect+580     01094024  AND      T0,T0,T1            5.560.
 <     73  reset_vect+584     0109B826  XOR      S7,T0,T1            6.080.
 <     75  reset_vect+588     0017B82B  SLTU     S7,ZERO,S7          6.600.
 <     77  reset_vect+58C     15E00031  BNE      S7,ZERO,code_start+F4  7.120.
 <     79  reset_vect+590     00000000  NOP                          7.640.
 <     81  reset_vect+594     40087800  MFC0     T0,PRId             8.160.
 <     83  reset_vect+598     40026000  MFC0     V0,SR               8.680.
 <     85  reset_vect+59C     40809000  MTC0     ZERO,WatchLo        9.200.
 <     87  reset_vect+5A0     40809800  MTC0     ZERO,WatchHi        9.720.
 <     89  reset_vect+5A4     3C010010  LUI      AT,0010            10.240.
 <     91  reset_vect+5A8     00411024  AND      V0,V0,AT           10.760.
 <     93  reset_vect+5AC     3C010040  LUI      AT,0040            11.280.

 For Help, press F1                                        Setup != Data  Tektronix
```

Additional Features

- Extensive controls are provided to select the types of cycles stored during acquisition, as well as the types of cycles displayed by the disassembler following acquisition.
- Time-stamping of all acquisition samples allows determination of the absolute or relative timing between events of interest.
- Display of block transfer items can be reordered from sub-block ordering to natural, sequential ordering.
- A search facility is provided to allow acquisition samples to be searched for which match or do not match particular values. The search facility also allows the mnemonic disassembly display to be searched for the occurrence of text strings of interest.

Performance analysis of memory access activity in histogram form can be displayed, as well as time-correlated display of instruction execution behavior linked directly to your high-level language source code.

Contact List

USA

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Crescent Heart Software is a member of the Tektronix Third Party Developer team.

Personal Line

Flexible Logic Analyzer Family for the Windows Operating System

Salient Features

▶ Disassembles without the need of preprocessor hardware for reverse assembly of processor code with detection and marking of jumps and non-executed instructions

▶ Easy-to-use graphical user interface operating under Microsoft Windows™ 3.1x, Windows 95, and Windows NT

▶ High Level Language Manager for debugging on source-code level and trigger on a source code line

▶ Software interface for user written control and data display programs

▶ Easy documentation through full compatibility with Windows programs like WinWord

▶ 32 to 192 channels with external clock rate of 100 MHz, configurable in 16-channel steps sharing either a single clock source or two time-correlated clock sources

▶ 32 KB memory depth with full channel count, 64 KB at half the channels

▶ Internal clock rates up to 1 GHz for 72 channels or 144 channels with 500 MHz

▶ High-impedance 16-channel active logic probes for easy adaptation and minimum loading

▶ Powerful 15-level trigger with physical trigger outputs to trigger external devices

CPUs Supported

V_R4300 (µPD30200), others on request

Host Platforms

PC: Microsoft Windows 3.1x, Windows 95, and Windows NT

Product Overview

The Personal Line (PL) Logic Analyzer Family features up to 192 channels per mainframe, a memory depth up to 32 KB, external clock rate up to 100 MHz, and internal clock rate up to 1 GHz. A full range of triggering capability with interactive data stimulus allows the system to work as an ideal ATE system for user-specific applications. The system can be stand-alone or slaved to a PC running as an application under the popular MS Windows.

Capabilities include full time-correlated dual processor tracing (expandable to 16 processors), powerful disassemblers and high-level language debugging, a software interface to control and operate the Personal Line from user-written programs, and a 10-ns time-stamp for time correlation of all buses (processors) being monitored.

Object Formats Supported

COFF, ELF/DWARF, IEEE-695, Intel OMF386

Member of Controlware Group

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Fax: +81 (0) 3 5205 2030
E-mail: kakurai@toyo.co.jp

proLine

Microsoft Windows-Based
Real-Time Debug Tool

Salient Features

▸ Connects to any Windows 95, 98, or NT PC

▸ Easy GUI with automatic setup

▸ Supports external bus speeds up to 180 MHz

▸ Supports multiprocessor systems

▸ Raw data bus disassemblers support state and timing recordings without preprocessor hardware

▸ High-level language manager for debugging on source-code level

▸ Link to software debuggers

▸ Rapid support service for new types of NEC-based ASICs and processors

▸ Remote control from UNIX and Windows workstations using VNC

▸ Records up to 4 million events in a single shot to find even the toughest problems

▸ Programmable event search finds the most complex events within the trace

▸ Flexible target connection technologies

CPUs Supported

NEC VR43xx and all processors with an external address bus

Host Platforms

Windows 95/98/NT

Product Information

proLine is the latest of dli's Windows-based high-end logic analyzer systems.

The hardware supports target speeds up to 180 MHz on the external bus, extremely deep memory for ultra-long traces, as well as most complex trigger and trace conditions at all system speeds.

The software allows easy handling of most complex situations, offers various time-correlated data views, supports easy system setup, and can be used on any PC, even without the instrument connected (e.g., for documentation purposes). VNC enables full remote accessibility via a local network or the Internet.

Intelligent high-level language support provides source code debugging of application programs, including break/trigger points of the logic analyzer on a source code line and correlating the real-time trace with the source code.

Object Formats Supported

COFF, ELF/DWARF, IEEE-695, Intel OMF386

Member of Controlware Group

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Fax: +81 (0) 3 5205 2030
E-mail: kakurai@toyo.co.jp

TLA 700 Series Logic Analyzers

Salient Features

▶ MagniVu™ acquisition technology provides 2 GHz timing resolution and 200 MHz state acquisition simultaneously on all channels, all the time, through a single probe

▶ Up to 16 M deep memory on all channels with hardware-accelerated data search and display

▶ Universal source code support for correlating high-level languages with real-time trace

▶ Performance analysis support for optimizing target system performance

▶ Remote control using Microsoft COM/DCOM technology supports advanced data analysis

▶ Open PC platform with Microsoft Windows 98 operating system

▶ Compatible with the widest range of "Best in Class" debug tools

▶ World-class four-channel 1 GHz, 5 GSa/s DSO provides high-fidelity acquisition of analog signals

▶ Modular logic analyzer mainframes that establish a platform for the future

▶ Extensive embedded tools partnership program

CPUs Supported

NEC VR5432

Host Platforms

Windows 95/98/NT

Product Overview

The TLA 700 Series is a new family of logic analyzers developed specifically to address the fast-changing needs of today's embedded developers. These products bring new technology to bear on the time and design pressures faced by the entire design team. The TLA 700 Series includes a wide selection of logic analyzer modules with measurement capabilities not seen in logic analyzers before.

The TLA 700 addresses the needs of digital design teams. Hardware developers, hardware/software integrators, and embedded software developers will all find that the TLA 700 provides solutions for those elusive problems that threaten their product development schedules.

The family consists of portable and benchtop mainframes, logic analyzer modules, DSO modules, and a full line of complementary support products for popular microprocessors and buses.

Additional support is under development.

Tektronix

Ordering Information

For more information, contact your local Tektronix sales
office or visit our Web site at http://www.tektronix.com/
Measurement/logic_analyzers/

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Fax: +81-3-3434-3897

In-Circuit Emulators

CodeTAP® Emulator for MIPS Processors

Salient Features

▶ Crash-proof run control

▶ Source-level debugging

▶ Hardware and software breakpoints

▶ Reliable, robust target debug connection with CodeTAP® emulator

▶ Integrated Development Environment promotes ease of use

▶ Graphical Project Manager provides easier, faster build process

▶ Exceptionally fast C and C++ compilers speed development

▶ Class and source browsers help reveal software interaction

▶ Source editor offers quick, easy navigation and editing

▶ High-speed Ethernet download shortens debug cycles

Applied Microsystems
C O R P O R A T I O N

CPUs Supported

NEC VR5432

Host Platforms

Windows 95/98/NT

Product Overview

High-performance MIPS development solutions from Applied Microsystems include the patented CodeTAP® compact in-circuit emulator and the award-winning CodeWarrior™ Integrated Development Environment (IDE). Integrating Applied's hardware-enhanced tool and the easy-to-use CodeWarrior IDE offers developers speed and productivity enhancements that let them build higher quality products more quickly.

The CodeWarrior IDE includes a graphical project manager, editor, fast compiler, linker, and graphical debugger, comprising all the tools needed to create, manage, compile, link, and debug fast, optimized C/C++ code. The class browser supports both object-oriented and procedural code, with view of inheritance and class hierarchy as well as classes and functions. Debugger displays make it easy to evaluate complex expressions and structures and a simple mouse-click on a calling function reveals its source. The debugger offers an expandable, editable display of local variables and parameters, and direct editing of processor registers.

The CodeTAP emulator fits seamlessly into the CodeWarrior IDE. Installation is accomplished with a simple plug-in to the MIPS processor debug port (N-Wire). Operating over fast and straightforward Ethernet communication, the tool provides high-speed code download and crash-proof run control. Software and hardware breakpoints can be set in RAM, ROM, or flash, and the target system can be reset remotely.

Instead of spending time on tasks such as managing the file system, maintaining make files, and dealing with tool compatibility problems, MIPS developers using this high-performance integrated solution can concentrate on actually developing and debugging embedded software.

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NetROM
500 Series Target
Communicator

Salient Features

◗ Source-level network debugging from any host

◗ Support for industry-leading source-level debuggers

◗ Support for RTOS task-aware and system-level debugging

◗ Works with most microprocessors, allowing use in multiple projects

◗ Network connectivity without Ethernet on the target

◗ Rapid code download over high-speed Ethernet connection between target and host

◗ Four virtual UART LAN channels for multiple-user NetROM™ or target sessions

◗ 1–4 MB emulation memory supports large code images—up to 16 MB with multiple units

◗ Automatic support for 3.3-volt and 5-volt memory devices

◗ Supports 8-, 16-, 32-, and 64-bit words

Applied Microsystems
C O R P O R A T I O N

◗ Eight user-asserted target command signals

◗ Supports writable memory for breakpoints in ROM space

CPUs Supported

All NEC MIPS CPUs

Host Platforms

Sun-4, HP 9000, MS Windows PC

Product Overview

NetROM is the backbone of a flexible embedded system debugging platform. It combines high-speed target communications and debugging capabilities. Linking your preferred debugger and target monitor, NetROM accelerates the development cycle through faster downloads and target communications, remote target control, and emulation of memory devices. NetROM requires almost no target resources and can be moved from project to project and processor to processor.

NetROM transforms any ROM/flash-based target into a network node, accessible from any host for all cross-development activities. Its virtual UART provides a high-speed link through which your source-level debugger communicates with a target-based monitor. NetROM provides eight programmable command lines that give programmers complete target control from any network host.

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NetICE™-5432

LAN-Based JTAG/ROM Emulator

Salient Features

◗ Real-time nonintrusive emulation of the VR5432 MIPS processor

◗ Optional support of VR5432 real-time trace via the JTAG port

◗ Integrates the power of a local-area network into the entire development process

◗ Powerful C/C++ source-level and assembler debugger

◗ Intuitive Windows 95/98/NT™ GUI

◗ Supports maximum processor clock speeds with zero wait states

◗ Requires no hardware or software resources from the target system

◗ Program download to target RAM

◗ Debug code in ROM, flash, and RAM

◗ Up to 8 MB ROM or RAM emulation option for very fast code downloads

◗ Compatible with the Corelis SCANTEST™ family of boundary scan test tools

CORELIS

CPUs Supported

NEC VR5432

Host Platforms

Windows 95/98/NT

Product Overview

The NetICE-5432 is an innovative LAN-based in-circuit emulator that provides a real-time, nonintrusive development environment for the NEC VR5432 MIPS processor.

The NetICE-5432 connects any VR5432 processor-based target into a network node that is accessible from any Windows 95/98/NT-based PC for all development and debugging activities. This capability is enabled by the NetICE-5432 full TCP/IP protocol stack. Downloading code from the host to the target through its JTAG interface is fast and is accomplished over the Ethernet using TCP/IP protocol that is available on most PCs that are connected to a LAN.

An optional ROM emulator allows very fast Ethernet code download to the target via its ROM sockets. It also allows the insertion of multiple software breakpoints into the ROM address space.

An optional real-time trace feature is available that allows a user to retrieve trace information via additional processor pins.

The Corelis NetICE-5432 emulator utilizes the industry standard IEEE-1149.1 (JTAG) boundary scan test port to access the internal debug resources available on the NEC VR5432 MIPS processor. Since the boundary scan logic of the VR5432 processor is separate from the core processor logic itself, this access mechanism allows complete, nonintrusive access to any processor resources. Thus, no interrupts, RAM, ROM, or registers must be assigned for debug purposes and no ROM-based debugger or loader program is required. At the same time, no peripheral resources such as serial ports are needed to communicate with the emulator/debugger. The NetICE-5432 allows users to debug high-speed, cached applications at the full speed of the target processor.

Windows 95/98/NT-based host software provides a complete symbolic C source-level debugging capability and is compatible with all popular cross-compilers that support ELF/DWARF or COFF files. The source-level debugger is a 32-bit Windows 95/98/NT application. Interaction with the source-level debugger is through resizable windows, context-sensitive user-programmable toolbars, menus, and dialog

boxes. There is no need to learn a command-line interface for interactive usage.

Programs and data can be downloaded to any part of the system RAM through the JTAG port without the need for a resident loader program. The JTAG interface is a simple interface that connects to the target system via a flexible ribbon cable and does not require removing the microprocessor. The JTAG interface is controlled by a Corelis-developed, high-performance, LAN-based boundary scan controller that can be easily connected to a network. Due to the unique nature of the NetICE-5432 emulator, the same hardware controller can be used for many different processors that have IEEE-1149.1 compatibility. Thus, a developer using a VR5432 processor can migrate to other processors as required and retain the investment in hardware tools by merely installing another version of the Corelis NetICE emulator software.

Supported functions include:

- Reset processor
- Start and stop program execution
- Real-time trace buffer access
- Set breakpoints in RAM
- Set breakpoints in ROM or flash using hardware breakpoints
- Single-step source or assembly lines
- Single-step into or over function calls
- Step into, over, or out of functions
- Display and modify processor registers
- Display, modify, and fill memory
- Disassemble memory using VR5400 mnemonics
- Download code
- Powerful macro capability

The NetICE-5432 JTAG emulator lets you modify information displayed in a window by typing new values directly into it. For example, this feature allows you to directly write to or modify a memory location.

Source and Assembler Debugging

The Corelis NetICE-5432 emulator includes a powerful source-level debugger. The debugger supports multiple windows, allowing the developer to view many different processor activities simultaneously. For example, multiple windows can be established to view source code, assembly code, variables, register locations, etc. When viewing source and assembly code, for example, the debugger can display

source code corresponding to a particular line of assembly code, and vice versa.

Real-Time Trace (Optional)

The NetICE-5432 is available with an optional feature that takes advantage of the trace capabilities in the VR5432 processor, providing nonintrusive reconstruction of application code execution flow. Trace information is retrieved via the four TrcData lines and 1 TrcCLK line in real time and then used with the contents of processor memory to reconstruct program flow. Trace data is valid whether the processor is running from memory or the instruction cache. A screen is provided to allow control and management of events that can initiate the trace collection activity.

NetICE-5432-JR ROM Emulation Option

The ROM emulation option is designed for users who want to debug targets that include processors with JTAG debug functionality—such as the VR5432—but want to enhance this functionality with additional features such as ROM space breakpoints, faster code download, code download into the real ROM space, etc.

The NetICE-5432-JR emulator has all the JTAG as well as ROM emulation features. This functionality is achieved by adding a ROM emulator card option to the JTAG emulator.

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NetICE-R™

LAN-Based ROM Emulator

Salient Features

◗ Integrates the power of a local-area network into the entire development process

◗ Adds fast code download capability to your JTAG emulator via Ethernet

◗ Up to 8 MB of ROM or RAM emulation

◗ Supports 8-, 16-, and 32-bit data bus widths

◗ Replaces the target flash, EPROM, or RAM memory during debug. Simple and easy to use.

◗ Target processor independent

◗ Requires no hardware or software resources from the target CPU

◗ Enables JTAG emulators and monitor programs to set software breakpoints in ROM space

◗ Retains ROM content after power is cycled to emulate the real-time power-up target boot environment

◗ Flash/EPROM emulation speed of up to 45 ns access time

CORELIS

◗ Connects via a standard ROM socket or a special test connector

◗ Assortment of standard ROM cables available

◗ Supports standard (5 V) and low-voltage (3 V) targets

◗ ROMLoad utility software for direct hex file download over the network

◗ ROMLoad software supports Windows 95/98/NT, HP-UX, and Solaris

◗ ROM function C Library for ROM setup and code download from remote applications

CPUs Supported

NEC VR5432

Host Platforms

Windows 95/98/NT, UNIX

Product Overview

The NetICE-R is an easy-to-use ROM emulator designed for fast download of ROM-based code over the Ethernet to the user's real-time/embedded target system.

The NetICE-R is a processor-independent tool that can be used with other development tools such as JTAG emulators, ROM monitor programs, embedded operating systems, etc. The NetICE-R adds fast download capabilities to inherently slow JTAG emulators, provides a remote host to target connectivity, and eliminates the need to program flash or EPROM devices every time new target software is generated.

The target board is connected to the ROM emulator via a cable. A standard cable plugs into the target ROM socket or a special cable is available that connects the address, data, and control signals of the target ROM device to the NetICE-R's 50-pin, SCSI-2-type connector.

Once connected to the target board, the user can download standard hex files quickly and easily over the Ethernet interface using the ROMLoad utility software that supports Windows 95/98/NT and UNIX host platforms.

ROMLoad Utility

The ROMLoad utility software is used for remotely setting up the NetICE-R memory configuration and for downloading

hex files from the PC to the NetICE-R memory. The software is provided with a graphical user interface for Windows 95/98/NT and as a command-line utility for HP-UX and Solaris.

Motorola S-Record format is a standard format for hex files and is generated by most software development tools such as C compilers and assemblers. S-Record files are typically used when programming EPROM/flash devices using a standard PROM programmer. The ROMLoad utility eliminates the need for EPROM/flash device programming during the development phase of the project and enables the user to download new hex files quickly and conveniently to the emulation memory.

ROM Function Library

For users who want to develop their own host application and not use the provided ROMLoad utility, the NetICE-R is shipped with a ROM Function Library (RFL) Dynamic Link Library for use with 32-bit Windows program development. A summary of the RFL functions is provided below:

JTAG_Connect()

This function will connect the client application with the NetICE-R. The socket number of the connection is returned as an informational item.

JTAG_Disconnect()

This function will disconnect the client application from the NetICE-R.

ROM_Configure()

This function configures the ROM emulation module.

ROM_Control()

This function controls the enabling of the host and target interfaces.

ROM_Download_File()

This function downloads a file into the ROM emulation memory.

ROM_Fill()

This function takes one item and writes it to a specified number of sequential locations in the ROM emulation memory.

ROM_Pod_Info()

This function returns binary data describing the pod configuration of the detected ROM emulator boards.

ROM_Read()

This function reads data from ROM emulation memory.

ROM_RFL_Version()

This function returns a zero-terminated ASCII string, which provides the version number of the ROM Function Library DLL.

ROM_Version()

This function returns a zero-terminated ASCII string, which provides the version level of the ROM emulator.

ROM_Write()

This function writes data to ROM emulation memory.

LAN Standards

The NetICE-R fully supports the popular TCP/IP protocol. It is possible to connect the NetICE-R to various networks as long as the connection between the user's workstation and the NetICE-R uses the TCP/IP protocol.

Configurations

The NetICE-R is available in four different emulation memory configurations. The user may order either one or two built-in ROM emulation pods with preconfigured emulation memory of one or two megawords. Bus width options are 8, 16, or 32 bits. Consult the factory for any other custom configurations.

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Fax: +81-3-3434-3897

MAJIC^{PLUS}™

Advanced JTAG Interface Controller

Salient Features

◗ Ideal for SOC-based applications

◗ 32 x 512 KB trace memory

◗ Nonintrusive: uses no target resources

◗ Execution tracing from embedded flash, ROM, or cache

◗ Supports a wide choice of on-chip debug interfaces

◗ Supports a wide variety of CPU cores

◗ Supports on-chip hardware breakpoints

◗ Unlimited software breakpoints

◗ Programmable JTAG clock (TCK = 0 to 40 MHz)

◗ Trigger-in and trigger-out connections

◗ Ethernet and serial I/O ports for fast, flexible host interface

◗ High-speed download (>200 KB per second) of application code

◗ Network compatibility allows shared and remote operation

◗ Flash memory for easy firmware updates to support additional CPU cores or on-chip debug interfaces

◗ Sleep mode support

◗ CE marked for operation within the EC

◗ LEDs display operation status

◗ Open API for debugger interface

CPUs Supported

NEC VR5432

Host Platforms

PC: Windows 95/98/NT; Sun-4: SunOS, Solaris

Product Overview

The MAJIC^{PLUS} emulator provides a high-speed hardware interface between processors with an on-chip debug interface and industry-standard debuggers. It is available with a choice of EPI debuggers and may be adapted for use with RTOS-aware debuggers from leading RTOS vendors. The unit is self-contained in a small case approximately 2 inches x 6 inches x 7 inches in size.
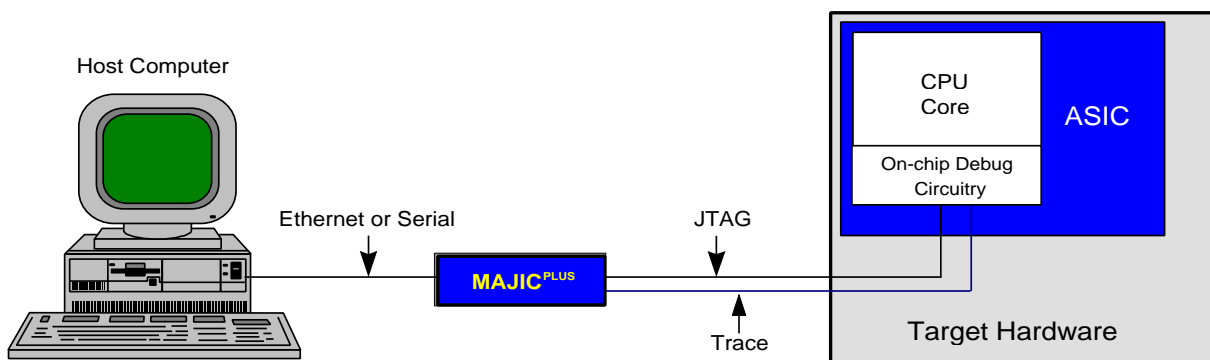
Now engineers using SOC devices can have the same level of control and visibility of the embedded CPU operations as with in-circuit emulators in traditional discrete CPU designs. The result is faster software integration, better testing, and improved time to market. The MAJIC's ability to expand to support additional cores, debug interfaces, or SOC devices eliminates the need to buy new emulators for each new project, thus reducing project costs.

Completely nonintrusive, the MAJIC^{PLUS} communicates to the CPU core by JTAG using the existing boundary scan pins. It uses no target memory and requires no porting to the target system.

Complete processor control means you can start, stop, and single-step execution; read and write to registers, memory, and system I/O; and download code to target RAM—all within most industry-standard debugger interfaces.

Host Computer

Ethernet or Serial

MAJIC^{PLUS}

JTAG

Trace

CPU
Core

On-chip Debug
Circuitry

ASIC

Target Hardware

Complete visibility means that you can now trace program execution on the deeply embedded CPU core. Using on-chip debug facilities such as PCTrace, N-Trace, and Real-Time Debug, the emulator provides real-time visibility into the program's behavior even when the CPU is executing from cache, flash, or ROM embedded within an SOC.

You may adapt the MAJIC^{PLUS} for plug-and-play operation with your specific processor or CPU core by selecting from a wide range of configuration kits. The kits contain the firmware and user license to match your CPU's on-chip debug facilities. Install multiple configuration kits, and the MAJIC^{PLUS} will support a variety of CPU types. The configuration kits also contain the adapters, accessories, and target interconnection cables required for the selected CPU.

The MAJIC^{PLUS} is ready to run with the EPI software tools and any development board that supports a connection to the on-chip debug interface. This tool combination will provide you with a proven working environment.

The MAJIC^{PLUS} is available as a stand-alone unit or as a complete emulation kit. The kit comes with serial and Ethernet cables, source-level debugger, documentation, and one year of free maintenance, support, and updates. Part number: MAJIC^{PLUS}-KIT.

Full development kits are also available that include a full compilation toolkit. See the *MAJIC Price and Configuration Guide* for full details of these development kits.

Specifications

Target control:	JTAG
JTAG clock (TCK):	0 to 40 MHz Programmable
Download speed:	>200 KB/second (typical)
Trace memory:	32 bits x 512 KB Configurable
Trace clock (DCK):	0 to 100 MHz
Trace control:	Trace disable BNC, TTL level
Target voltage:	2.4 to 5.0 V
Serial interface:	RS-232-C 1900-115.2 k baud
Ethernet interface:	10/100Base-T, TCP/IP
Triggers:	Trigger input, Trigger output
Trigger levels:	TTL
Indicator LEDs:	Power, Status, Run, Connect, Ethernet
Size:	2.0 H x 7.4 W x 6.5 L (inches)
Weight:	2.25 lbs
Input power:	5 VDC +/- 5%, 4.0 A
Power connector:	2.1 mm coaxial, center positive, male
Temperature:	Operating 0–40°C
Humidity:	Operating 15–95% RH
Safety/EMC:	CE

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SYS4K In-Circuit Emulator

Salient Features

- Up to 50 hardware breakpoints

- Up to 8 MB overlay memory

- 32 KB deep trace memory

- Optional real-time profiler

- Three-dimensional Trace Control™

- Single-step ROM and exception handlers

- Built-in memory tests and scope loops

- Download up to 3 MB per minute

- 16 external logic inputs

- Emulate without changes to code

- Assembly-level debugger

- Available source-level debugger

- Ethernet and serial interface to host

CPUs Supported

VR4300, VR4305, VR4310

Host Platforms

Sun-4: SunOS, Solaris; PC: Windows 95/NT; HP 9000: HP-UX

Product Overview

The SYS4K in-circuit emulator provides full-featured emulation for the NEC VR4300 series processors. EPI meets the critical demands of the RISC development environment by combining the features of a high-performance logic state analyzer and high-speed emulator with a fully integrated suite of software development tools supporting both 32-bit and 64-bit environments. This combination provides designers with an extremely powerful debugging environment that improves productivity throughout the development cycle, including bring-up of prototype hardware, debug of application software, and troubleshooting—in both development and production environments.

Debuggers– *Don't Wait to Get Your Code Working*

EPI offers two environments for debugging. EDB is a powerful windowed source-level debugger for C and assembly language programs. For rapid debug of your C code, EDB fully integrates C source-level debugging with the capabilities of the emulator, including synchronizing the source window with the trace display.

MONICE, a symbolic assembly-level debugger, offers features especially useful to hardware engineers for prototype debug, automated testing, and manufacturing test. It is source-language independent, making it equally useful debugging code written in assembly, C, Ada, or other languages.

Both debuggers employ the facilities of a host computer to manage the user interface, symbol tables, file systems, etc. This leaves the emulator free to manage and track the target system.

These debuggers also work with EPI's target-resident debug kernel (RSS-MIPS) to provide very low-cost debug stations. Without learning a new debugging interface, developers can easily access networked emulators when their power is needed to track down the elusive bugs that can kill a development schedule.

High-Speed Download– *Don't Wait to Say Go*

The SYS4K emulator can download code and data into your target at Ethernet rates or up to 600 KB per minute over serial RS-232. Downloading at these speeds dramatically increases the number of debug-fix-download-test cycles a software engineer can do every day, so you deliver your product sooner.

Overlay Memory– *Don't Wait to Burn PROMS*

With the overlay memory options you can map up to eight megabytes of memory into your target system. With it you can download code to target memory space that contains ROM. You will never have to burn a ROM again until your product is ready for final tests. When your code is executed from overlay memory you can set software breakpoints in ROM space. You can explicitly program initial accesses and block refill wait states or match your target's performance exactly by using its acknowledge.

Online Assembler– *Don't Wait to Test a Fix*

The debuggers' online assembler makes it easy to try a "fix" without waiting for a rebuild of your code. You can "patch" your code instantly, then Go to test the change. There is no need to compile and link the application.

Trace and Logic Analysis– *Don't Wait to Find the Bug*

The emulators combine a fully featured logic state analyzer with full-speed trace of the processor's activity. This combination means you can track the progress of your application, stop on virtually any event, and see a history of the processor's activity. With this power you can track down bugs in minutes that could take days or weeks without the emulator.

The emulator can record (trace) a frame of the target's activity once each clock cycle. In addition to the processor signals, a frame includes emulator status signals, a 46-bit time-stamp, and 16 general-purpose inputs. The emulator samples these signals using the same rules as the processor.

Find Complex Bugs in Real Time

The Three-Dimensional Trace and Execution Control language specifies the behavior of the trace mechanism and its controlling state machine. It directs the emulator, on a cycle-by-cycle basis, to perform actions such as trace one frame, stop execution, and trigger external instruments. Since the decision to trace a frame is made every cycle, you capture only the information needed, thereby optimizing the use of trace memory.

The application can be stopped on the occurrence of virtually any pattern or sequence of patterns. These hardware breakpoints do not require execution of specific instructions. For example, you can stop the processor when it writes a specified value to a specific address. This kind of breakpoint can easily find offending code when memory is being over-written.

Trace Display

Once trace frames have been captured, you can display the instruction and data accesses as disassembled instructions with symbolic references or in "raw" format of 1s, 0s, and hex values. With the C source-level debugger traced instructions may be displayed with the original C source code lines interleaved between the captured instruction flow.   Physical addresses are translated and displayed as virtual addresses.

Host Resource Access– *Don't Wait for Hardware*

The SYS4K emulator supports EPI/OS. Combined with EPI's full ANSI run-time library, EPI/OS makes it possible for your application code to use host computer resources. Now your code can display status information on the host monitor and even read or write files on the host file system, making it easy to simulate peripherals not yet implemented.

Target Memory Tests– *Don't Wait to Test Memory*

Not just software development tools, the TURBO emulators offer features to assist the hardware engineer to debug the design. The emulators offer six built-in memory tests, three scope loops, and the ability to trace its own accesses to target memory. Now you can thoroughly test the memory subsystem and peripherals even before the target is capable of loading and executing a program.

Additionally, the emulator's trace mechanism with 16 external signal inputs and its ability to trigger a scope can often eliminate the need to connect a logic analyzer.

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Modeling and Simulation

DeskPOD™

Salient Features

◗ Ideal for use by both hardware and software teams

◗ Coexists with both logic simulation tools and software development tools

◗ Convenient form factor with an Ethernet interface to host workstation

CPUs Supported

VR5432

Logic Simulators Supported

Verilog-XL™ and NC-Verilog™ from Cadence Design Systems, Inc.

ModelSim™ from Mentor Graphics Corporation

VCS™ from Synopsys, Inc.

MODELING FOR CO-DEVELOPMENT

Product Overview

Tired of using slow, incomplete, and inaccurate simulation models? Simpod is your source for the most accurate, highest performance simulation models available for NEC's family of MIPS microprocessors. Whether you are interested in simulation models for verification of ASICs, boards, or complete systems, or you want to take advantage of hardware and software coverification to start verifying your system interaction earlier in the design process, DeskPOD is the answer.

DeskPOD: Models Without Compromise

The solution to the difficult modeling problems of system verification is DeskPOD from Simpod. DeskPOD provides an innovative solution that addresses the key issues of time to model, accuracy, and performance. DeskPOD is patented technology that uses actual silicon devices to provide cycle-accurate models of microprocessors. These models can be coupled to logic simulators, software debuggers, or any other application of interest.

Creating models to run on the DeskPOD is as simple as defining the pinout of the device, the inputs, outputs, bidirectionals, and clocks. Modeling difficulty increases only linearly with pin count, not exponentially. All peripherals integrated on the microprocessor are immediately available. A DeskPOD model even incorporates the "errata" and "known limitations" of the device. The purpose of the DeskPOD is to enable its users to get a new chip and have a model running in one day.

There are no questions about the accuracy of the model with DeskPOD. Using DeskPOD saves engineering teams hours of wondering if a simulation error is in the model or in the embedded system design itself. There is nothing more accurate than using actual silicon to verify a design.

DeskPOD Delivers

Availability

DeskPOD models are available in days. Complete software models can take months or even years to create and verify.

Accuracy

DeskPOD uses the actual silicon to obtain model behavior. Why waste valuable time wondering if problems are in the model or in your design?

Performance

DeskPOD models are orders of magnitude faster than HDL models. Simpod's advanced modeling technology enables optimal run-time performance.

Hardware/Software

DeskPOD models are integrated with both the HDL simulation and the software debug environment, enabling the software to be verified against the hardware design before prototypes are available.

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Synopsys, Inc.

Introduction

Synopsys' Logic Modeling products are the leading source of simulation models to the electronic design industry. The models include ModelSource™ and LM-family™ hardware modeling, SmartModel® Library, the MemPro memory model generation tool, and VHDL and Verilog source code models.

Product Overview

The ModelSource 3000 series and the LM-family hardware model servers bring the benefits of hardware modeling accuracy, fully functional behavior, easy model development, and excellent simulation performance to the desktop. Hardware modeling systems use the actual physical device to model its own behavior during simulation.

Hardware models provide accurate and full device functionality, including any undocumented behavior. With hardware models, designers can execute actual code during simulation, improving design verification and accelerating software integration and debugging.

The SmartModel Library contains behavioral models of more than 11,000 devices from more than 40 semiconductor companies. Devices supported include microprocessors, DSPs, FPGAs, PLDs, and memories.

SmartModels offer expert assistance to the board and ASIC designer. Each model performs a series of usage and timing checks during simulation that look for undefined interrupts, uninitialized registers, illegal conditions, or any misuse of the component that is likely to slow or stall the design process. Any errors that are discovered are thoroughly documented, with the part instance, pin name, and time of occurrence specified.

The MemPro memory model generation tool creates HDL memory models based on industry standards for memory device functionality and features an advanced testbench interface and efficient workstation resource utilization essential for large system verification. Each model is generated from a common user specification, device template, and technology core to ensure that model behavior is consistent from one design level to another and provide confidence that the models are correct throughout the design flow.

Salient Features

- Comprehensive approach to simulation modeling needs

- Broadest device coverage: microprocessor, FPGAs, PLDs, DSPs, logic, and memories

- All models have intelligent error checking, full timing, and consistent unknown handling to improve simulation accuracy

CPUs Supported

NEC VR41xx, VR43xx, VR5000, VR54xx, VR10000/12000

SYNOPSYS®

MemPro's Windows™-based GUI makes it easy for designers to rapidly select memory device specifications, generate a model, and modify it as the design evolves. MemPro offers designers the ability to generate models for all existing types of memory while allowing them to choose the level of model abstraction needed to fit the verification process, from system block to fully accurate.

Logic Modeling Bus Interface Models help ease board and complex ASIC design challenges by giving designers access to preverified bus interface models that comply with the latest version of a specification. All Logic Modeling bus interface models are interoperable with one another and can be universally controlled through the Logic Modeling control bus.

Synopsys offers Logic Modeling bus interface models of the following specifications: PCI, AGP, USB, Ethernet, IEEE 1394, ISA, EISA, SCSI-2, PC Card, and VME.

Ordering Information

Products and worldwide support are available from Synopsys; contact your local Logic Modeling representative, call 1-800-34MODEL, or e-mail modelinfo@synopsys.com. To see which models are available, visit the Logic Modeling Model Directory at http://www.synopsys.com/products/lm/modelDir.html.

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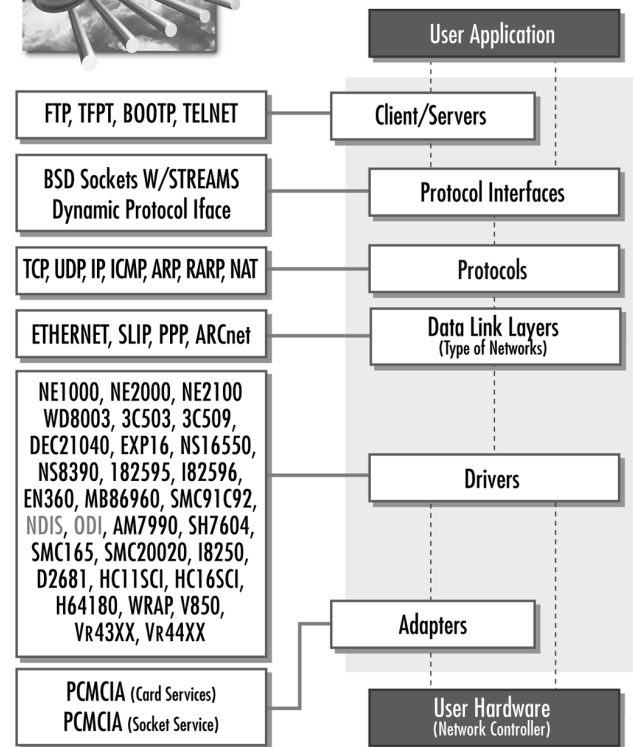Internet: http://www.synopsys.com

Network Support Tools

USNET
Real-Time Embedded Networking

Complete TCP/IP Protocol Suite

Salient Features

▶ Embedded TCP/IP

▶ Processor independent

▶ RTOS independent

▶ Royalty free

▶ Includes complete source code in ANSI C

▶ Small footprint (25 KB code space most processors)

▶ User configurable

▶ ROMable and reentrant

▶ TCP, UDP, IP, ICMP, ARP, RARP, IGMP, and NAT protocols supported

▶ Supports Ethernet, SLIP, and PPP

▶ BOOTP, DHCP, PING, Telnet, FTP, and TFTP supported

▶ SNMP agent and Internet access package with embedded Web server available as add-ons

	User Application
FTP, TFPT, BOOTP, TELNET	Client/Servers
BSD Sockets W/STREAMS Dynamic Protocol Iface	Protocol Interfaces
TCP, UDP, IP, ICMP, ARP, RARP, NAT	Protocols
ETHERNET, SLIP, PPP, ARCnet	Data Link Layers (Type of Networks)
NE1000, NE2000, NE2100 WD8003, 3C503, 3C509, DEC21040, EXP16, NS16550, NS8390, I82595, I82596, EN360, MB86960, SMC91C92, NDIS, ODI, AM7990, SH7604, SMC165, SMC20020, I8250, D2681, HC11SCI, HC16SCI, H64180, WRAP, V850, VR43XX, VR44XX	Drivers
	Adapters
PCMCIA (Card Services) PCMCIA (Socket Service)	User Hardware (Network Controller)

▶ Over 40 drivers supplied, including generic Ethernet and serial driver

▶ Training classes available

CPUs Supported

NEC VR43xx, VR44xx

Product Overview

USNET is processor and RTOS independent and is designed for use with real-time embedded applications. It is ROMable and reentrant to ensure compatibility with multitasking operating systems. Complete source code and test programs are provided. USNET is licensed per application and is royalty free.

USNET provides your choice of device drivers and link layers. Device drivers provide support for most popular network controllers, including Fast (100 MB) Ethernet

U S SOFTWARE
E M B E D D E D   E X C E L L E N C E

devices. USNET supports a variety of approaches. Included are a client/server function interface, a dynamic protocol interface (DPI), and BSD sockets.

USNET can be configured to use only the client/servers, protocols, device drivers, and link layers needed by your application. The TCP/IP protocol requires about 25 bytes on most processors.

Two add-on packages are available. These include Hyperlink Products, Simple Network Management Protocol (SNMP) (versions 1 and 2 support with MIB compiler), and Hyperlink products aip Internet access package. The latter includes a DNS resolver, e-mail supporting SMTP, POP, and MIME, and an embedded Web server. The embedded Web server is also available separately.

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Development Support Products

Services for MIPS Developers

Salient Features

◗ Dedicated to supporting MIPS developers

◗ GNU-based toolkit and reference board products

◗ Windows CE system integrators

◗ Active support for other OSs: VxWorks, Linux, OpenBSD

◗ Training, reviews, and other design team support

◗ Software and hardware customization

◗ Software porting

CPUs Supported

All NEC 64-bit RISC CPUs

Host Platforms

Our software tools run on Windows 95, Windows NT, Sun UNIX, HP UNIX, Linux, and BSDI BSD/OS.

Why Aren't There Any Pictures on these Pages?

All boards look the same—increasingly, even their block diagrams look the same. And all software packages look the same, too. So please imagine a picture of a CD ROM on a pile of English red and white roses, and we'll save the space to offer some more information about development tools.

About Algorithmics

Algorithmics operate from London, England to support MIPS developers all over the world - particularly by Internet.

Many companies offer reference boards, and many companies offer development tools - typically, to get a good-sized market they offer them for a range of CPUs. Other companies with brand-name tools or real-time OSs offer the best support they can for architectures other than Intel's or Motorola's, but their release schedules tell a story.

Algorithmics offer MIPS, and nothing else. If there's anything you need to develop a MIPS application, then we'll offer it ourselves, integrate someone else's product, tell you where to buy it, or tell you how to do without it.

Our customer base contains most companies that apply MIPS outside the workstation world—but we can't tell you about the best names. We can usually get some references in response to your inquiry.

You'll find pages here describing our compiler toolkit (built round GNU C—when the best compiler in the world is free, why reinvent the wheel?) and our reference boards. But for most of our customers it's the integration of those, and our ability to back it up with design, consultancy, and educational skills, which makes us most useful.

Experience and Track Record

We've been providing services to MIPS developers since 1988, but our MIPS experience goes back two years before that. We bring unequalled experience of solving problems with MIPS, backed up by partnerships with companies supplying critical components or software. We know the MIPS market backwards.

Whether you need guidance around the MIPS world, technology to reuse, access to "folklore," or even rescue— we're here to help.

Tools and Reference Boards

Algorithmics' SDE-MIPS product is a comprehensive toolkit including GNU C together with our own extensive target-system libraries and low-level utility software.

Algorithmics are the leading supplier of MIPS 64-bit RISC reference boards. P-4032 supports 32-bit bus CPUs like VR4300, and P-5064 handles high-end 64-bit CPUs like VR5000.

Both boards support many different CPU types, and we're committed to widening the range as required. They have

✦❄algorithmics

Ethernet for fast download, large memory expansion, PCI expansion, and an extensive range of PC-world I/O controllers. You can read about the boards elsewhere in this catalog.

Algorithmics provide software support for key OSs—notably Windows CE and VxWorks.

If your application is to be built without a separate OS, then the invaluable range of MIPS support software supplied in SDE-MIPS can be extended with a POSIX-oriented threads package; enquire.

Algorithmics as a Windows CE System Integrator

We think that Windows CE may well be very influential outside those headline application areas. It is the leading contender for a general-purpose embedded OS which would allow systems to exploit reusable software components. So we signed up with Microsoft in March; we've got CE 2.1 running on our reference boards; and are now open for business.

We expect to provide device drivers, OALs (that's the software which glues the OS to your hardware) and advice in integration.

Software Porting

Retargetting software to new hardware is often a good activity to subcontract. We've worked from OS (we did the first 64-bit MIPS version of VxWorks) to applications (the whole software suite for a laser printer).

Semicustom Software and Hardware

We have a large library of our own sources, available for license on sensible terms for a modest one-off fee. You can either take code as is, with basic support and training; or we can customize and port the software to your hardware.

This includes drivers, interrupt handlers, a complete FP emulator, a power-on self-test skeleton with many useful device tests, a kit to build BSD TCP/IP code into a stand-alone system, and more.

We also license the design of our reference board, in whole or in part, together with the services necessary to get them into your design.

Training

We offer general 1-, 2- and 3-day courses on MIPS hardware and software, as well as specialized in-depth sessions on particular subjects.

Designing for Performance

We can give authoritative advice on meeting your performance requirements, from choice of CPU and memory system through to getting the best from optimizing compilers. We have specialist tools running in-house which we can use to simulate the effect of different types and sizes of cache, for example.

Services to Hardware Designers

Algorithmics will review your hardware design, to avoid pitfalls, expose bottlenecks, and ensure that you are hospitable to a range of system software.

We offer on-site engineering support to get your design through its critical first phase.

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Design and Development Services

Salient Features

◗ Extensive expertise and experience with MIPS processors

◗ Development of embedded systems from concept to completion

◗ Board Support Packages (BSPs) and device drivers

◗ Hardware design, including FPGA and VLSI design

◗ Enhancements, porting, and systems re-engineering

◗ Outsourcing, consulting, and on-site programming

◗ Cost-effective offshore development

CPUs Supported

NEC VR41xx, VR43xx, VR5xxx

Host Platforms

Windows 95/98/NT, UNIX, Linux

BATON ROUGE INTERNATIONAL, INC.

BRI

The Global Information Technology Company

Excellence in Embedded Systems Design

Today's embedded systems industry faces growing pressures from all sides: increased global competition, shortened product cycles, and the need to "do more with less." Frequently, companies realize they can't tackle these issues alone and seek the energy, expertise, and efficiency of a reliable partner who can deliver an on-time, on-budget solution. BRI is that kind of information technology business partner.

Our mission is simple; we help our clients get better products to the market faster by providing:

• Consulting—on-site or offsite

• Fixed-price development services

• Turnkey solutions—from concept to completion

• Rapid establishment of a well-equipped offshore development center

With a global team of more than 175 professionals devoted to embedded systems, BRI is one of the largest embedded systems design and development services companies in the United States. A rock-solid and substantial infrastructure provides the right mix of skills and experience to help you meet performance objectives, time/schedule milestones, and budgetary goals for your project.

We design and develop a wide variety of embedded systems, from small microcontroller-based devices to large multiprocessor real-time systems and from 4-bit microcontrollers to 64-bit microprocessors.

Hardware Development

BRI designs and develops analog and digital hardware with various processor architectures. We have experience working with all interface technologies and bus architectures, making us job-ready for your next assignment.

BSPs and Device Drivers

BRI develops board support packages for custom or off-the-shelf hardware utilizing RTOSs. We also write device drivers for various peripherals and interconnection devices.

Firmware Development

BRI has extensive experience implementing, porting, testing, debugging, and maintaining firmware for a variety of business partners. BRI has expertise in programming in all assembly languages as well as high-level languages.

Embedded Systems-Concept to Completion

BRI has the expertise and experience to develop the entire system from concept to completion—generate specifications, identify the tool sets and hardware, architect, design and develop, test and document the complete system.

Our expertise in embedded technologies is well complemented by our experience in a number of application areas, such as:

- Communications/Internet infrastructure
- Consumer electronics
- Process control
- Industrial automation
- Defense/aviation
- Automotive electronics

Proven Models To Solve Customer Problems

BRI's wealth of experience setting up customer-specific development centers offshore has resulted in the development of proven models and procedures for executing projects, taking into account methodologies, coding standards, project and management structures, documentation standards, intellectual property rights, and customer confidentiality issues.

BRI's dedicated ISO 9001-accredited R&D center in India offers a cost-efficient offsite alternative to your in-house project setting. BRI consistently shortens development cycles, resulting in as much as a 50% overall project cost savings.

Known for well-managed development procedures, BRI has earned a reputation as a long-term, reliable, and high-performance partner.

A Single Source of Support for Companies That Use a Variety of Software Applications

In addition to the design and development of embedded software on various platforms, BRI has extensive experience in creating software applications on general-purpose platforms under operating systems such as UNIX and Windows. BRI's expertise extends to systems software, Internet/Web technologies, databases, and networking.

BRI can quickly assemble a cross-functional team that can provide a comprehensive technical approach to solving all of your IT problems. With a top-flight multidisciplinary team, we can tackle unique development challenges—even create a 24 x 7 development cycle, if necessary. Whether your customers are demanding better and more functionality or

your competition is "raising the bar" for ever-shorter delivery cycles, BRI can stand with you to deliver on time and on budget with dependable services and high-quality solutions.

For over a decade BRI has provided cost-effective solutions to complex embedded real-time problems for companies such as:

General Electric	Sun Microsystems
Harris	Telecordia
Lucent Technologies	Toshiba
NEC	TRW
Siemens	Wind River Systems

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NEC VR Series Training

Salient Features

▶ Highly targeted presentation

▶ Integrated hardware and software concepts

▶ In-depth understanding of the MIPS architecture

▶ Flexible seminar content

▶ Available at NEC or customer site

▶ Voice grade or video teleconferencing seminar option

Overview

This seminar is designed for hardware and software personnel who must become competent quickly. Both the VR Series microprocessors and interfacing chips are covered. An overview of each topic precedes the later in-depth presentation and discussion. Thus three types of attendees will benefit: 1) programmers and designers, 2) engineering managers, and 3) support personnel.

VR Series Course Contents

The Architecture

• Overview of reference materials and development environments

• General architecture of the VR4xxx and VR5xxx families

• Instruction set architectures (ISAs)

• Core—CPU (the integer processor)

— Pipeline
— Register set usage
— Multiply/Divide/Shift unit
— Instruction set

• CP0—System Control and Exceptions
— Hardware virtual to physical mappings
— Register set
— Setting up the environment

• CP1—Floating-Point Coprocessor
— 32-bit and 64-bit models
— Exception enabling vs. event recording
— Rounding modes

• Exception Processing
— Understanding and controlling interrupts
— Exception and error levels
— Exception processing registers
— Boot (start-up) vs. normal vectoring
— Coprocessor control

• MMU—Memory Management Unit
— Software control of virtual to physical addressing
— Address translation with even and odd pages
— Kernel/Supervisor/User mappings
— Address space ID vs. global accesses
— Write protection

• Cache Memory—Instruction and Data
— Cache organization—line size, tagging, and effect of the dirty bit
— Flushing
— How a write-back cache works
— Filling and indexing

The Software

• The Software Tool Chain
— Description of available software tools
— Demo of a build

• Assembly Environment
— Demo of an assemble and execution
— When must I use assembly language?
— Sections—code, small vs. large memory
— Pseudo opcodes
— Debugging—using .frame and .mask
— MIPS object file format—COFF

NEC

- C Environment
  - — Demo—compile and execution
  - — Compile options
  - — Preprocessor
  - — Interfacing with assembly language
  - — Libraries
- Linker
  - — Demo—linking and using the object tools
  - — Link editor
  - — Run-time linker
  - — Object file tools—size, dump, etc.
  - — Archiver
- PMON
  - — Installing PMON
  - — Controlling execution
  - — Display and modification of registers and memory
  - — Controlling and observing the environment—history
  - — Flushing the data and instruction caches
- Source-Level Debugging
  - — Invocation
  - — Breakpoints
  - — Compiling a program
  - — Building a command line
  - — History
  - — Recording and playback

The Hardware Interface

- Functional Overview of the Pinout Groups
  - — Interface functions
  - — Clock/control signals
  - — Interrupt signals
  - — JTAG
  - — Initialization
- System Interface
  - — Description—address, data, and issue cycles (handshaking)
  - — Interface protocols—master/slave states
  - — Processor and external agent requests
  - — Handling requests—misses, loads and stores, CACHE instructions
  - — Initial bus requests by the processor or external agent
  - — Subsequent requests—multiple reads, read followed by a write, etc.
  - — Discarding and re-executing commands—using the eok (external ready) signal
  - — Transfer of commands/data identifiers between processor and external agent

Support Chips

- Detailed operation of NEC support chips, including PCI

CPU-Specific Features

- 4300—Differences from other family members
  - — Caching and cache parity
  - — Status and Configuration registers
  - — System interface and clocking
  - — Buffering
- 5000—Secondary cache
  - — Probing validation and clearing
  - — Writing and reading
- 54xx—High-performance microprocessor
  - — Dual-issue superscalar pipeline
  - — Nonblocking loads/stores and split transactions
  - — Performance measurements and branch prediction
  - — Multiply/Accumulate and media instructions
  - — Cache line locking
- 41xx—Contact NEC for seminar information on this processor family.

Seminar Length

The seminar is designed to last three days. However, it can be tailored to individual customer needs.

Seminar Site

This seminar is offered periodically at NEC headquarters in Santa Clara, California and at customer sites if desired. Remote seminars from NEC to user sites are available via voice-grade telephone lines or video teleconferencing.

Information and Registration

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Design Services and HDL Models

About Papillon

Papillon is a hardware engineering company providing all aspects of product design for computer and industrial clients. There are many companies offering design services today. Some specialize in ASIC design, some in FPGA design. Others concentrate on VHDL or Verilog synthesizable models.

We believe in providing a full solution to hardware design, taking your concept from inception through design and into volume production. We provide not only ASIC, FPGA, and board-level design, but also analog, mechanical, and EMI design toward agency compliance.

Design Philosophy

During the initial stages of the architecture we work closely with our clients to gather the necessary design criteria. The design is then implemented in technology-independent VHDL or Verilog and synthesized to the target device. We use leading-edge tools to simulate the product at the chip, board, and full product level, the outcome of which is a working product. While most design houses stop at this point, we believe an integral part of the process is to aid in the introduction of the product into manufacturing. We do this because we take pride in our work and are not satisfied until the product meets or exceeds our clients' expectations. And we know that mutual success is the only way to develop long-term, working relationships with our customers.

ASIC and FPGA Device Design

Papillon has experience with numerous foundries and technologies, with gate-array and cell-based designs ranging from a few thousand to over 100,000 gates. We engineer new designs, as well as enhancements and cost reductions to existing designs. Our ASIC and FPGA designs are always implemented in technology-independent VHDL or Verilog, and are simulated with the surrounding elements in the system to ensure a first-pass success.

Full Product Design

The engineers at Papillon collectively have designed products for the communications, telephony, imaging, graphics, printer, and workstation industries, as well as many other specialized markets.

MIPS Products and Services

Papillon is well suited to the design of MIPS products and offers a support chipset for the IDT R3051 processor, as well as VHDL models for the R3051 family. Papillon's MIPS-powered designs are found in a variety of graphics, network, and communications products.

Papillon will develop custom behavioral or synthesizable VHDL and Verilog models, as well as license other models from a library of parts.

PAPILLON
Research

SPECIALISTS IN HARDWARE ENGINEERING

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Consulting Services

Salient Features

◗ Determine the technical feasibility of products and develop specifications

◗ Analyze and design the overall system architecture

◗ Provide all aspects of software and firmware development, including design, coding, testing, debugging, and documentation

◗ Review hardware designs and debug prototype hardware

◗ Perform limited digital hardware modeling and design

◗ Write internal and external documentation

◗ Perform software audits and walk-throughs

The Engineering Challenge

In today's fast-moving global marketplace, the engineering challenge is to design increasingly sophisticated products, more quickly, without compromising quality. Meeting this challenge requires a broad range of skills and a significant number of staff hours, yet with the current emphasis on lean organizations, in-house development staffs cannot always meet these requirements. With increasing frequency, companies are recognizing the advantages of using outside help to avoid compromising quality, timeliness, or cost.

The Probitas Answer

Probitas Corporation has provided computer development and consulting services to electronics and computer firms since 1981. We have extensive experience as designers, developers, and technical managers, and can tackle the most difficult technical problems associated with bringing high-quality computer and microprocessor-based products to market on time. Our success lies in:

• Our ability to learn new systems quickly; we are generalists, serving a broad range of clients with diverse needs. Clients use us even when we have no previous experience in a particular application, because they can count on our reputation for quality and our fast learning curve.

• Close cooperation with you throughout the project. We listen to your concerns, understand your system requirements and constraints, and help you choose the best overall solution.

• Thorough analysis and documentation, which results in products with a high degree of reliability and maintainability.

• Delivery of quality solutions at reasonable cost; we pride ourselves on our ability to complete projects in the shortest time consistent with your quality requirements and our standards.

• Continued availability from day to day and from year to year since 1981.

PROBITAS

Excellence in Computer Engineering

A. J. NICHOLS is the founder and president of Probitas Corporation. He has substantial technical expertise in designing and implementing computer architectures, operating systems, and microprocessor-based products. He has a PhD and an MS in Electrical Engineering from Stanford, and BS degrees with honors in both Business Management and Electrical Engineering from the University of Colorado.

Prior to establishing Probitas, Dr. Nichols was vice president of engineering at Millennium Systems, Inc.; held technical management positions at Intel Corporation, American Microsystems, Inc., Novar Corporation, and Lockheed; worked in engineering development, system design, database management, operating systems, and the design and application of microprocessors and related components; and taught graduate courses in switching theory, computer architecture, and logic design at Stanford in the Electrical Engineering and Computer Science departments. He has written numerous papers, holds three patents, was chair of the Special Interest Group on Microprogramming for the Association of Computing Machinery (ACM), and has been an ACM National Lecturer.

DAVID SIMON has twenty years of experience in all aspects of software development, including specification, design, coding, documentation, maintenance and quality assurance. His areas of emphasis include embedded systems, LAN software, AppleTalk, graphics, computer-aided design, and accounting. Mr. Simon has an MS degree in mathematics from the University of Chicago and a BS degree in mathematics from Stanford.

Prior to joining Probitas, Mr. Simon was vice president of software development at Vectron Graphic Systems, a firm specializing in software products for printed circuit board design. He has programmed in C, C++, various assembly languages, FORTRAN, and LISP, using the IBM PC/DOS, Windows, CP/M, VAX/VMS, and UNIX operating systems. He also has experience with various graphics devices. He is the author of three books on computer programming with more than 80,000 copies sold.

MICHAEL GRISCHY has over fifteen years of experience in all aspects of software development. Areas in which he has worked include embedded real-time systems, serial communication, Windows virtual device drivers, LAN protocols, and printed circuit board CAD. His work has also emphasized software design for portability.

Prior to joining Probitas, Mr. Grischy was a key architect of Teradyne's PCB layout software. He has programmed in C, C++, Pascal, FORTRAN, and Z80 assembler using PC/DOS,

Windows and Windows NT, VAX/VMS, and Sun/UNIX operating systems. He has a BSEE degree from San Jose State University.

RICHARD STEINBERG has over eighteen years of experience as a software developer and a professor of computer science and mathematics. His recent work includes radio network protocol development, SNMP driver extensions, and numerical analysis. He has programmed in C, C++, assembly languages, Pascal, and FORTRAN using DOS, Windows, and Windows NT. He has taught courses in data structures, programming languages, artificial intelligence, digital system design, compilers, analysis of algorithms, and formal languages and automata. Mr. Steinberg earned an MA degree in mathematics from the University of California at Berkeley and a BS degree in mathematics summa cum laude from MIT.

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SeaWind

Introduction

Seaweed Systems is a software house that specializes in X Window system products and services.

Seaweed's software products are geared for the real-time/embedded marketplace and offer aggressive performance, feature sets, support, and implementation schedules.

Consulting services are also available for custom and specialized needs.

Product Overview

SeaWind, Seaweed Systems' implementation of the X Window system, Version 11, provides a fully functional environment appropriate for real-time or embedded systems running either the pSOS or VxWorks real-time kernels. SeaWind includes both X and OpenGL server-side and client-side technology.

Server Side

On the server side, SeaWind can run on a variety of graphics processor options. SeaWind's X server connects to clients over the backplane, over the network, and locally.

Client Side

On the client side, SeaWind offers a variety of library implementations. These libraries can also connect to an X server over the network, over the backplane, or locally.

SeaWind's client-side libraries include Xlib, OSF/Motif, the intrinsics toolkit, the Athena widgets, support for various extensions, the Inter-Client Exchange library, the Session Manager library, the Xmu library, and the X Imaging Extension library.

The libraries are reentrant and can therefore support multiple simultaneous local clients. In addition, various clients, including xterm, mwm, and twm, are offered.

SeaWind's X server implementation supports all the standard R6 extensions, including XIE.

All products are available in either source or object form.

SeaWind supports Wind River's gcc-based tool chain and the tool chains endorsed by Integrated Systems.

Contact Seaweed about target information for server-side support.

Salient Features

◗ OpenGL + X11R6 + Motif 2.0 client and server environment for VxWorks and pSOS

◗ Includes a garbage collector for memory and file descriptors

◗ Highly efficient

◗ Libraries and clients are reentrant

◗ Custom graphics accelerator ports available

CPUs Supported

All CPU boards running VxWorks or pSOS for client-side support

Host Platforms

Any system appropriate as a development platform for VxWorks or pSOS

Seaweed Systems

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Application Conformance Test Suite (ACTS)

Salient Features

⬧ Verification testing tool for UNIX System V applications running on MIPS processors

⬧ Tests compliance of applications to the Application Binary Interface (ABI) binary compatibility standard for MIPS

⬧ Generates detailed compliance reports

CPUs Supported

NEC VR4100, VR4300, VR5000, VR10000

Host Platforms

UNIX

Introduction

The ACTS™ is provided to application vendors to allow them to check that their applications conform to the requirements of the ABI. Of necessity, the ACTS is processor specific, though the task of porting to a new processor is far simpler than generating a product of the complexity of the ACTS.

Product Overview

The ACTS provides two tools, a static checker and a dynamic checker.

ACTS Static Checker

The ACTS Static Checker checks the set of binaries (executables, archives, dynamic shared objects, etc.) that constitute an application. These tools verify conformance of the binary formats and ensure that the binary only makes use of valid external services (processor instructions, system calls, etc.).

The Static Checker checks the format and content of each binary file that forms an application and ensures that the application only makes use of available library interfaces.

The Static Checker checks each of the binaries supplied for:

• ELF header format and contents
• Program header format and contents
• Section header format and contents
• Symbol table format and contents
• Relocation table format and contents
• Instruction set usage
• Stack frame conventions
• System service usage
• Shared library requirements

ACTS Dynamic Checker

The ACTS Dynamic Checker modifies the binaries to allow run-time inspection of external service call arguments. The modified binary can then be executed against the application vendor's quality assurance plan in order to identify any miscreant call usage.

Both of these tools make use of a common database that describes the facilities a conforming application can use. Many aspects of this database are common across different processor architectures. This database can be used to distinguish features available to base applications and to identify limitations on instructions available for little-endian applications. The database is extensible to cater for changes that may arise as a result of changes in the PowerPC™ processor architecture.

Experienced with Test Suites

UniSoft has been working closely with the ABI (Application Binary Interface) Group for the MIPS processors for several years, providing the group with the Application Binary Interface Verification Test Suite (ABIVTS). UniSoft has also written test suites for X/Open, UNIX International, and Novell-USG.

UniSoft Experience

UniSoft was founded in 1980 as a UNIX porting house, initially concentrating on adapting UNIX Version 7 to Motorola 68000-based microcomputers and expanding its focus to verification testing in 1986.

Today UniSoft specializes in the supply of products and services in custom implementation of verification test suites for industry-standard Application Programming Interfaces (APIs) and Application Binary Interfaces (ABIs) as well as conformance and verification testing services. UniSoft continues to provide UNIX-based software engineering services as well.

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Articles

Device I/O Drivers Basics

by: David Kalinsky, Wind River Systems, Inc.

The bad news is that device drivers are critical software—get that wrong and nothing works. The good news is that writing device drivers does not have to be a mysterious Black Art, full of "bit-bashing and register-twiddling." True, the focus in writing I/O device drivers is generally at the nuts-and-bolts level. But it is also possible to take a higher architecture-level view of device input/output driver software: to break down the fundamental I/O driver types and see just how they work. And thus to remove much of the mystery of writing I/O drivers.

In most cases, developers do not have to create their I/O device drivers from scratch. Nowadays embedded systems software developers take advantage of the services of a real-time operating system (RTOS) to structure their device driver software. For example, the pSOSystem RTOS supports tasks, Interrupt Service Routines (ISRs), and mechanisms for reliable communication and synchronization among them, as well as an API for device drivers. An RTOS will be used in the driver architectures shown here.

The table shows some of the general I/O driver types. These include synchronous and asynchronous drivers, as well as serial and general spooler drivers. These types cover most of the I/O driver Cases.

General I/O Driver Types		
Synchronous Driver	Input	Popular, basic architecture
Asynchronous Driver (Queued Inputs)	Input	Requesting task runs in parallel with hardware device
Latest Value Only Asynchronous Driver	Input	Old values are discarded
Serial Data Spooler	Input	For free-running hardware device
Serial Data Spooler	Output	For tasks preparing more outputs (assuming outputs always ready)
General Data Spooler "Priming the Pump"	Output	Tolerant of unavailable output

Mutual Exclusion Access

One basic OS truism that a device driver designer may encounter is the need to ensure that only one application task at a time can request an input or output operation on a specific device. For example, if an application task needs a temperature measurement in units of degrees Celsius and another needs degrees Kelvin, the driver architect had better make sure that only one task at a time can ask for a temperature measurement.

An easy way to ensure this is to use the mutual exclusion mechanisms available in an RTOS. In pSOSystem, for example, the simplest such mechanism is a semaphore, operating in binary fashion. The driver programmer must make sure that each application task obtains the semaphore's token before initiating a temperature measurement. And the semaphore's token must be returned at the end of the temperature measurement.

For devices that may be thought to be session-oriented, it is not sufficient to guarantee exclusive access of a task to a device for a single I/O operation. Exclusive access must be granted for an entire session, which may consist of many individual I/O operations. For example, a single task might want to print an entire page of text, whereas the printer driver's output operation prints only a single line of text. In such a case, the printer driver must offer application tasks an "open session" operation-and the corresponding "close session" operation.

In this kind of driver architecture, the "open session" operation would request the (binary) semaphore token. And the "close session" operation would return the semaphore token. (The "session" semaphore would initially contain one semaphore token, to indicate "session available.") Any other task attempting to "open session" while the semaphore's token is unavailable would be denied access. In pSOSystem RTOS, for example, these session opening and closing operations are called de_open() and de_close().

Synchronous vs. Asynchronous

A much larger question in architecting a device driver is that of synchronous versus asynchronous driver operation. To put it another way: Should the application task that called the device driver wait for the result of the I/O operation that it initiated? Or should the application task continue to run while the device driver is doing its I/O operation?

Most real-time operating systems typically support both alternatives. But the device driver's architecture will be of vastly differing structure for each of these alternatives.

Synchronous I/O Drivers

In a synchronous driver architecture, the application task that called the device driver will wait for the result of the I/O operation that it asked for. This does not mean that the entire application will stop and wait while the driver is working to perform the I/O operation. Other tasks will be allowed to continue working at the same time that the I/O hardware is working. Only the task that actually called the driver will be forced to wait for the completion of its I/O operation.

Synchronous drivers are often simpler in their architectures than other drivers. They are built around an RTOS mechanism for preventing the requesting task from executing while the driver and I/O hardware are working, and then releasing the requesting task for continued execution when the driver and I/O hardware have completed their work.

This can be done with a (binary) semaphore. (Note that this is a different semaphore than the binary semaphore described earlier for purposes of mutual exclusion of tasks. So a synchronous driver might actually contain 2 or more binary semaphores.) At driver initialization time, this new semaphore would be created but not given any semaphore tokens. An attempt to get a semaphore token when none is available would force the requesting software to stop executing.

In the pSOSystem RTOS, this is done by having the entry-point area of a driver behave essentially like a subroutine of the requesting task. So, for example, if a task calls a driver via a de_read() call, the entry area of the driver implementing the de_read() would act much like a subroutine of the task. And if the entry area of the driver attempts to get a semaphore token that is not present, the entry area of the driver would be blocked from continuing execution, and the requesting task would be put into the blocked state.

This can be seen in Figure 1. The requesting task is shown on the upper left as a rectangle with rounded corners. Beneath the semaphore is an ellipse representing an ISR. The "lightning" symbol represents the hardware interrupt that triggers execution of the ISR.
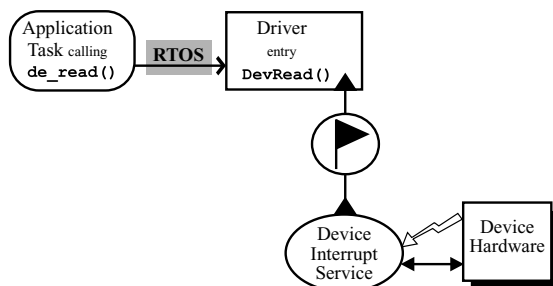
Figure 1. Hardware Interrupt

The ISR is considered part of the driver. Its job is to execute when an interrupt arrives announcing that the hardware has completed its work. In this example, the interrupt announces that the hardware has completed reading a new input. When the ISR executes, its main function is to create a new semaphore token (out of "thin air") and to put it into the semaphore upon which all the rest of the software here is waiting. The arrival of the semaphore token releases the software on the upper left from the blocked state; when it resumes executing, it can take the final results of the hardware I/O operation and begin processing.

The entry area of the driver (shown as a rectangle in the upper center of the diagram) does the logic described in the following pseudocode when called by a task:

```
DevRead_entry:
    BEGIN
        Start IO Device Read Operation;
        Get Synchronizer Semaphore Token
        (Waiting OK);
        /* Wait for Semaphore Token */
        Get Device Status and Data;
        Give Device Info. to Requesting Task;
    END
```

The ISR has very simple logic:

```
DevRead_ISR:
    BEGIN
        Calm down the hardware device;
        Put a Token into Synchronizer Semaphore;
    END
```

Now let's complicate the situation...

Asynchronous I/O Driver

In an asynchronous driver, the application task that called the device driver may continue executing without waiting for the result of the I/O operation it requested. This is true parallelism, even in a single-CPU hardware environment. The task continues to execute while that hardware executes the requested I/O operation.

Asynchronous drivers are more complex in their design than other drivers. In some cases, an asynchronous driver might be "overkill." You need to ask yourself the question, "If my task requests an I/O operation through a driver, then what work can it usefully do before that I/O operation is done?" Occasionally the answer may be "No, I need the I/O completed before my task can usefully do anything else." Such an answer says than asynchronous driver is overkill.

Sometimes an asynchronous driver can be architected so that every time a task asks the device driver for a new input, two things happen: (1) The driver asks the I/O hardware to start getting a new input; and (2) The driver gives the requesting task the last previous input to work on in the meanwhile. Sometimes this may be a useful way to work. Figure 2 shows what the driver would look like.
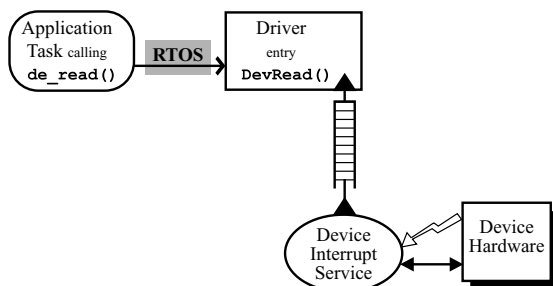

Figure 2. Message Queue

The ladder-like symbol in Figure 2 represents a message queue. It's a place to store information about a previous input.

The entry area of the driver can get a previous input from the queue, to give to the requesting task. And the ISR puts new input into this queue as it comes in. The entry area of the driver does the logic described in the following pseudocode when called by a task:

```
DevReadAsync_entry:
   BEGIN
      Get Message from the Queue (Waiting OK);
      /* Wait if Queue is Empty */
      Start new IO Device Read Operation;
      Give old Device Info. to Requesting Task;
   END
```

The ISR has this logic:

```
DevReadAsync_ISR:
   BEGIN
      Calm down the hardware device;
      Get Data/Status Info. from Hardware;
      Package this Info. into a Message
      Put Message into the Queue;
   END
```

In order for this to work, a driver initialization operation needs to create the Message Queue, which is at the heart of this driver. If the hardware input device never delivers an input unless it is requested to do so by software, the maximum length (depth) of this queue will be one message. In some RTOSs, such a single-message-length queue is termed a Mailbox.

Latest Input Only

If a hardware input device is free to deliver inputs even when not explicitly requested by software, the asynchronous design described would be inappropriate. The problem is that old inputs would queue up in the Message Queue. Requesting tasks would be fed very old inputs, while newer inputs would languish in the message queue. For a free-running input device, a better driver architecture might be that shown in Figure 3.

This design shows a protected shared data area at its center. The shared data store, shown as a pair of parallel horizontal lines, always contains the latest input value. It is protected from data corruption and access collisions by its associated (binary) semaphore.

Whenever the ISR is triggered by a new interrupt, it gets new input data from the hardware, and overwrites the previous content of the shared data area. In order to do this cleanly, the ISR must obtain access permission from the associated semaphore.

Whenever a task requests input data from the driver, the driver entry software reads it from the shared data area, after obtaining access permission from the associated semaphore. Since old input data is overwritten by the ISR, the data being read and fed to the requesting task is always the "freshest" data available. The entry area of the driver does the following when called by a task:

```
DevReadLatest_entry:
   BEGIN
      Get Shared Data Access Semaphore (Waiting OK);
         /* Wait for Semaphore Token */
      Read latest input from Shared Data area;
      Return Shared Data Access Semaphore;
      Pass input data on to requesting task;
   END
```

The ISR does this:

```
DevReadLatest_ISR:
   BEGIN
      Calm down the hardware device;
      Get Shared Data Access Semaphore (No Waiting);
         /* ISRs should never wait */
      IF Semaphore OKs access
        THEN
         Get Data/Status Info. from Hardware;
         Write latest input to Shared Data area;
         Return Shared Data Access Semaphore;
        ELSE ...
      ENDIF
   END
```

In rare instances, this ISR will be unable to obtain the semaphore it needs to access the Shared Data area. These will be instances of the two "sides" of the design trying to access the Shared Data area simultaneously. In these instances, the ISR should not attempt to write into the Shared Data area, as that would very likely cause corrupted data to be delivered to the requesting task. The device driver architect will need to decide how the ISR will handle unavailability of access to the Shared Data Area.
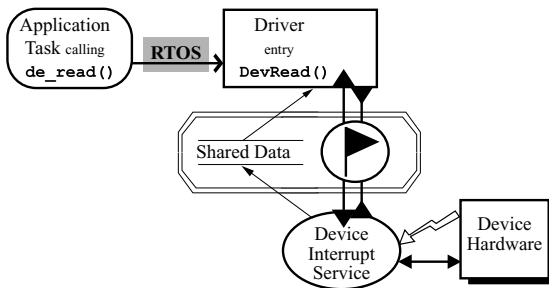

Figure 3. Protected shared data area

Serial Input Data Spooler

Very often a hardware input device can deliver inputs freely to a computer without its being explicitly requested by software. The driver is required to capture and process all of the incoming information without losing any -- even if it is arriving in irregular bursts. An example of this is the arrival of character strings from a serial line. Every character is a byte of incoming data, announced to the CPU by an interrupt.

Message queues are good for buffering irregular bursts. However, a message queue might impose too much performance penalty on a driver if it were to hold each arriving character in a separate message. So perhaps it would be better to use a message queue to hold pointers to larger buffers which would contain complete character strings. If the serial line never delivers strings of length greater than "S" characters, then buffers of length "S" bytes can be used for all strings.

Many RTOSs such as pSOSystem have a Memory Partition dynamic allocation facility that can manage buffers of standard sizes. The ISR part of the driver could "borrow" a buffer from a Partition of appropriate buffer size, and fill that buffer with a character string. And then put a pointer to that buffer into the Message Queue, for transfer to the non-ISR part of the driver. We see this pictured in Figure 4.

The entry area of the driver does the following when called by a task:

```
DevInSpool_entry:
    BEGIN
        Get Message from the Queue (Waiting OK);
            /* Wait if Queue is Empty */
        Extract string information from message;
        Give string to Requesting Task;
        Return buffer to its Partition;
            /* When buffer no longer needed */
    END
```

The ISR has this logic:

```
DevInSpool_ISR:
    BEGIN
        Calm down the hardware device;
        Get new character from Hardware;
        IF in the middle of a string
         THEN Put next character into buffer
          ELSE /* Need to start on a new string
          */
          Put buffer pointer into a message;
          Put character count into this message;
          Put this message into Queue;
          Request new buffer from Partition;
          /* ISRs should never wait */
        ENDIF
    END
```

In some instances, this ISR will be unable to obtain the memory buffer it needs from the Partition for a new character string. The device driver architect needs to decide how to handle unavailability of buffer memory. In other instances, the ISR will be unable to send its message since the Queue may be full. The device driver architect needs to design a solution to this as well.
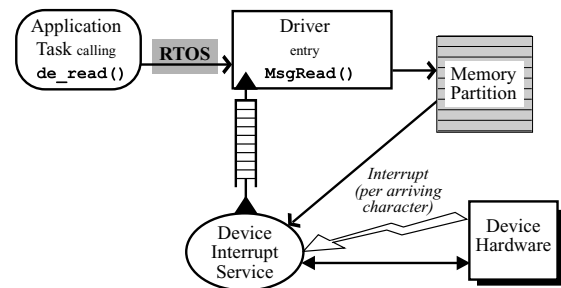

Figure 4. Memory Partition managing the buffers

Output Data Spooler

For many output devices, asynchronous drivers have clear advantages over synchronous drivers. While the asynchronous driver is working with its I/O device hardware to complete one output operation, the requesting task can already be preparing for the next output operation.

For example, a task may be preparing strings of text for printing while at the same time the printer driver is printing out previously prepared strings. This sort of driver is often used to allow numerous tasks to prepare and queue up their outputs. Queuing of outputs is typically in FIFO order.

The architecture shown in Figure 5 for an asynchronous printer driver, is quite similar to the device input spooler shown earlier. Two differences are the directions of access to the Message Queue and Memory Partition.
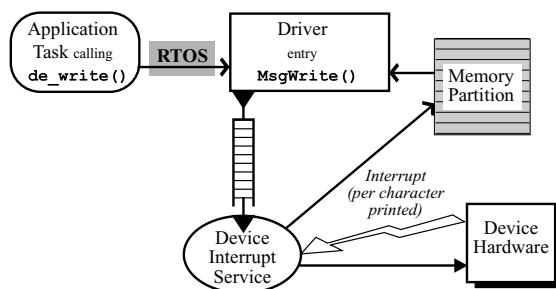
Figure 5. Using an asynchronous driver

The entry area of the driver does the following when called by a task:

```
DevOutSpool_entry:
   BEGIN
      Request new buffer from Partition;
      Fill buffer with string for printing;
      Put buffer pointer into a message;
      Put character count into this message;
      Put this message into Queue;
   END
```

The ISR has this logic:

```
DevOutSpool_ISR:
   BEGIN
      Calm down the hardware device;
      IF in the middle of the string
      THEN Send the next character to printer
      ELSE /* Need to start on a new string */
      Return previous buffer to its Partition;
          /* When old string no longer needed */
        Get Message from the Queue;
          /* ISRs should never wait */
        Get new string pointer from message;
```

```
        Get character count from message;
        Send first character to printer;
      ENDIF
   END
```

This driver design pretty much follows the pattern set by the previous driver designs. Unfortunately, it will fail miserably. It's got a built-in assumption that is probably not going to always be true in a typical embedded system: that the Message Queue that brings new buffers to the ISR always has one or more messages in it. In other words, it's assuming that there's always something new that needs to be printed.

What will go wrong if there's nothing new that needs to be printed? Well, after printing the last character that needs to be printed, the ISR will try to get the next message from the queue. But the queue will be empty since there's no "next message" waiting. So the ISR will exit without sending a new character to hardware. And so the hardware won't deliver another interrupt. (On output devices, an interrupt usually means "done doing the previous output and ready for a new one.") And so the interrupt service routine will never get to run again.

Even if new messages get queued up for printing, the ISR won't run again. The new messages will not get handled by the ISR. And printing will never get started again, if the driver is structured in this way. A small change is needed to fix this driver design, which will provide a similar driver architecture which does in fact work properly.

Priming the Pump

The Output Data Spooler driver design just described can be corrected by breaking the ISR apart into two pieces. The first piece of the ISR is the part previously described as "Calm down the hardware device." This contains all sorts of device hardware-specific activity which needs to be done upon each interrupt occurrence to make sure that the device is working properly and will work properly on the next output operation.

The second piece of the ISR is all of the remaining ISR logic. It relates to sending out a character to hardware, and also to making sure that the proper characters are being readied for subsequent output. This second piece might be called the "Character Handler." Normally while characters are being printed, the first piece of the ISR can simply call the second piece every time it runs. This was the driver design presented in the previous section. The "Calm Down" part of the ISR calls the "Character Handler" each time it runs. But that design ran into trouble. And the trouble was that there was no way to run just the "Character Handler" if an interrupt didn't arrive to run the "Calm Down" part of the ISR first.

Breaking the ISR's logic into two pieces can help, because it will allow us to call the "Character Handler" to be called from "Calm Down" when interrupts are coming in. And it will allow the "Character Handler" to be called in some other ways when interrupts are not coming in.

Driver architects refer to calling the "Character Handler" in these other ways as "Priming the Pump," since as soon as "Character Handler" is called when there's a message queued up to be printed, the "Character Handler" will send the first character to the printer and (as if by magic) the hardware will come alive and respond with an interrupt (to announce that it finished printing that first character). Once that first new interrupt arrives, the ISR begins to run in normal fashion again, with "Calm Downs" calling the "Character Handler" exactly as originally designed.

But a question remains: How does another chunk of software know whether or not it needs to call the "Character Handler"? The answer is that the "Character Handler" can detect when no more interrupts will be arriving and the driver is about to "die." It detects this indirectly, by detecting that the Message Queue which feeds it character strings for printing is empty at a time when a new character is needed to continue printing.

If "Character Handler" is usually run as part of an ISR, it can not wait for messages on this Queue. So it's got to do something else. One thing it can do is to put a semaphore token into a Semaphore set up especially for this purpose. This is an indication to any other interested chunk of software that no interrupts are expected. And so this chunk of software needs to call the "Character Handler" directly in order to "Prime the Pump."

An example of such a driver architecture is shown in Figure 6. It's an output data spooler, where the entry area of the driver may sometimes need to call the "Character Handler" in order to "Prime the Pump."
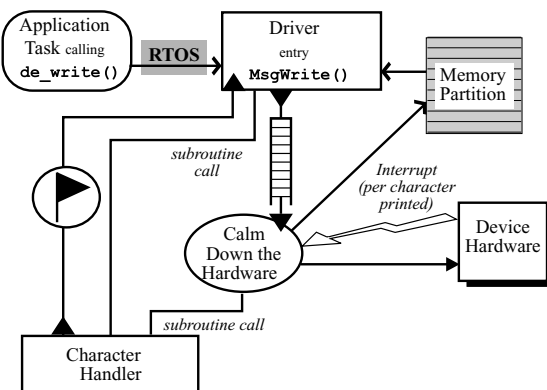
Figure 6. A semaphore token in a semaphore set up

The entry area of the driver does the following when called by a task:

```
DevOutSpoolBetter_entry:
   BEGIN
      Request new buffer from Partition;
      Fill buffer with string for printing;
      Put buffer pointer into a message;
      Put character count into this message;
      Put this message into Queue;
      IF semaphore is set
         /* Interrupts may be stalled */
       THEN call 'Character Handler' directly
      ENDIF
   END
```

The ISR has this very simple logic:

```
DevOutSpoolBetter_ISR:
   BEGIN
      Calm down the hardware device;
      Call 'Character Handler'
   END
```

And the 'Character Handler' itself looks like:

```
Character_Handler:
   BEGIN
      IF in the middle of the string
        THEN Send the next character to printer
        ELSE /* Need to start on a new string */
         Return previous buffer to its
            Partition;
          /* When old string no longer needed */
        Get Message from the Queue;
           /* ISRs should never wait */
        IF there is no message queued
           THEN set the semaphore
                /* Interrupts may soon stall */
           ELSE
           Get new string pointer from message;
           Get character count from message;
           Send first character to printer;
        ENDIF
      ENDIF
   END
```

This driver will recover from situations where there's nothing to print for a while. The semaphore added here gives the signal to "Prime the Pump."

Important Factors in Choosing a Real-Time Development System

Choosing a Real-Time Operating System

Today the biggest challenge facing real-time application developers seems not to be the application problem itself, but rather the real-time operating system (RTOS) and associated development environment on which to develop. Developers who at one time built their own system to accommodate their needs are now opting for one of the many commercial, off-the-shelf solutions in order to save time and money. The only problem is that now they must decide which solution best suits their application needs.

Choosing a real-time system can be a tricky matter, especially if developers must rely solely on what vendors tell them about the functionality and performance of their products. Ideally, developers could test their application, or at least key components of their application, on the various real-time operating systems to see which system best meets the application's needs. Unfortunately, few developers have the time or the resources that this is likely to require. Instead they typically use evaluation copies of the software and vendor or independent benchmarks to make a rough assessment of what is available.

Key Considerations

Knowing what to avoid is almost as important as knowing what to look for when choosing a real-time system. Key considerations can be overlooked or neglected in the process of making feature checklist or performance benchmark comparisons.

These considerations can include functionality issues such as flexibility in application design, or benchmarking pitfalls such as missing data or comparing dissimilar functionality.

Failure to take these factors into account may lead to a less than optimal or even wrong decision in choosing the best real-time system for an application. Developers may not realize their mistake until it is too late.

This paper highlights important considerations that are often neglected in standard benchmark and functionality comparisons. The first section discusses preemptive latency—what it is and why it can undermine the performance of your application. The second section discusses a well-known independent benchmark study—what the numbers mean and how they relate to application design and performance. Including these factors into the decision-making process will help developers ensure that they are indeed making a well-informed choice.

Preemptive Latency

Real-time operating systems have evolved from the monolithic entities of the past into multi-leveled hierarchies in which the lowest level is a real-time kernel. Multitasking, preemptive scheduling, high-speed context switching, low-interrupt latency, and fast, flexible intertask communication mechanisms are standard requirements of a real-time kernel. The benchmarks commonly used to compare existing kernels measure interrupt latency and context switch time, but an important metric often overlooked is the worst-case preemptive latency of the system.

Preemptive latency is the length of time between when a task context switch is required and when the task context switch is actually performed. Disabling context switching, commonly referred to as a preemptive lock, is a common mutual exclusion method for protecting critical structures. As with interrupt disabling, it is vital that the duration and use of preemptive locks is minimized. The ability of a system to guarantee a constant-time context switch (independent of the number of tasks) of 50 microseconds is meaningless if the system disables context switching regularly for hundreds of microseconds.

Minimizing Preemptive Latency

Minimizing preemptive latency in tasks is the responsibility of the developer. This is accomplished through judicious use of context switch disabling as a means of protecting critical code sections. Wherever possible, a semaphore should be used as an alternative to disabling preemption for the purpose of mutual exclusion. This has the advantage of allowing higher priority tasks uninvolved with the critical section to have continued access to the CPU.

Avoiding preemptive latency in the kernel is more difficult. In any multi-tasking system, the bulk of the application takes

place within the context of one or more tasks. However, there are times when the CPU is not in any task context at all. These times occur when the kernel is effecting changes to the internal queues or deciding what task to dispatch. During these times, we say the CPU is at *kernel* level instead of *task* level. With no task context associated with kernel level, the kernel cannot use a semaphore to guard internal structures, but rather must rely on the broader mechanism of disabling preemption to achieve mutual exclusion.

In order to minimize preemptive latency in the kernel, it is imperative that the kernel itself consist of the smallest number of orthogonal primitives sufficient to construct the higher levels of the real-time system. To illustrate this, imagine if a real-time system considered all functions as kernel functions (one popular real-time system actually does) and performed these functions at kernel level. This means that while a low priority task is making a call to allocate memory, get task information, etc., all higher priority tasks are locked out from preempting this task!

Minimizing Preemptive Latency-An Example

As an example, consider the user-callable subroutine **malloc()**, which allocates and returns a pointer to a block of memory of some requested size. The real-time system that performs the **malloc()** operation at kernel level will lock out preemption for the duration of the function. Simplified pseudo-code for this function might appear as follows:

```
malloc (size)

    {

    trap to kernel level

    find memory in the free list

    return to task level

    }
```

In this system a higher priority task will have to wait for a lower priority task to finish its memory allocation before it obtains the CPU. See Figure 1.
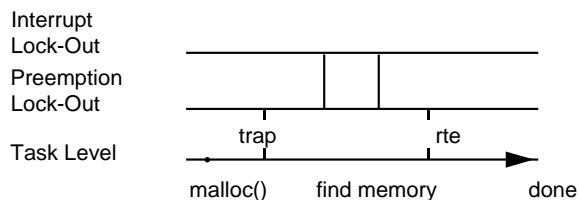
Figure 1. Standard Approach—
Preemptive Latency During Memory Allocation

By contrast, consider the real-time system that uses semaphores to avoid preemption lockout and executes the function at task level. Simplified pseudo-code in this case might be:

```
malloc (size)

    {

    semTake (memoryQueueMutex)

    find memory in free list

    semGive (memoryQueueMutex)

    return pointer to block

    }
```

If a low priority task begins a **malloc()**, and a higher priority task becomes ready, the higher priority task will immediately get the CPU if it is not also performing a **malloc()**. This means that preemptive latency is kept to a minimum. See Figure 2.
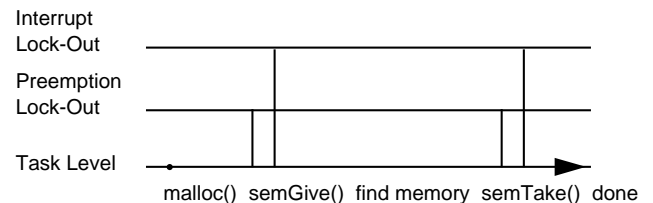

Figure 2. VxWorks Approach—
Preemptive Latency During Memory Allocation

Look for a Minimal Kernel

When choosing a real-time operating system, look for a minimal kernel that is designed to minimize preemptive latency. This is an especially important consideration since preemptive latency is very difficult to measure effectively and is rarely even mentioned in most benchmark specifications. High preemptive latency can even invalidate many benchmark timings and have ill effects on application performance.

The VxWorks® Development Environment is based on the fundamental principle of forming networked partnerships between the user's host development system and real-time targets. VxWorks offers a real-time operating system, extensive networking facilities and high-level development tools, all designed to work together with a developer's host computing environment. Both sides of the system do what they do best - the host operating system for workstation-based development, file handling, compiling, linking, loading and applications building and VxWorks for real-time control, testing and debugging.

Built on the lean and efficient **wind**® kernel, VxWorks provides a broad range of real-time system facilities including

interrupt handling, a real-time I/O and file system, memory allocation and a rich set of intertask communications facilities. In addition, the fast and complete networking facilities in VxWorks have made Wind River Systems a recognized leader in supporting distributed real-time environments.

VxWorks development facilities include an interactive shell, run-time linking, symbolic and source language debugging and performance monitoring. These tools are integrated with the operating system and networking facilities to provide developers with an efficient environment for quick development cycles. VxWorks component-level integration and modularity provide a seamless, turn-key real-time environment from development to deployment.

VxWorks is available on a wide variety of target architectures and processors and supports a number of different hosts. To provide developers with a comprehensive solution for real-time and embedded applications, Wind River Systems continuously adds to its portfolio of hardware and software support. In expanding its offering, Wind River System strives for full functionality and interoperability for all languages, processor architectures, development platforms and target environments supported by VxWorks.

Real-Time Benchmark Comparison

Benchmarks are often used by developers to estimate how an application will perform using a particular real-time operating system. While effective for simple timings such as context switching and interrupt latency, benchmarks usually do not reflect the complex environments present in most real-time applications. This means that benchmarks in and of themselves should not be used as a basis for choosing a real-time operating system. Design factors such as preemptive latency and optimizing features should also be taken into account.

Wind River System's real-time operating system VxWorks has proven that by keeping kernel functions to a minimum - an efficient calling interface, task management, and extremely fast synchronization primitives - preemptive latency can also be kept to a minimum. VxWorks extensive functionality beyond the kernel further demonstrates the strength and value of this design. Any facility built on top of the kernel executes at task level, thereby avoiding both preemptive and interrupt latency.

Developers need to match specific application needs to what a real-time operating system can provide.

In this section we examine a widely distributed independent benchmark study developed by an end user of real-time

operating systems. This study was created by the Superconducting Super Collider Laboratory (SSC) in May of 1991 and compares basic kernel and operating system performance among several commercial real-time offerings.

SSC Benchmark Overview

The SSC benchmark timings are based on a Motorola MVME 147S with a 25MHz 68030 processor. Interrupt and task response times are measured using an on-board timer with a resolution of 6.25 microseconds to time a single iteration. All other timings use the system clock to time a number of iterations to achieve the desired accuracy.

The original SSC benchmark tested four real-time operating systems. These include VxWorks, pSOS+, VRTX32 and LynxOS. Recently, Eyring Corporation published timings for its PDOS product. All are included in this paper for the sake of completeness.

Since the original SSC benchmark tested a now outdated version of Wind River System's VxWorks real-time operating system (v4.0), the benchmark source code was obtained and the tests were rerun with the latest version of VxWorks (v5.1). The tests and algorithms used in the original benchmark remain the same.

SSC Benchmark Results and Analysis

A true minimal kernel consists of an efficient calling interface, task management, and fast synchronization primitives. The SSC Benchmark professes to test kernel features, but in VxWorks features such as message queues and memory allocation are facilities built on top of the kernel and do not operate at kernel level. This is an important distinction when considering the potential preemptive latency in a system, especially since the SSC Benchmark does not take this factor into account. Developers should distinguish kernel versus task-level functionality when comparing the performance of real-time operating systems.

In order to give developers a more complete understanding of VxWorks design and performance, the following analysis presents both SSC results and additional information specific to VxWorks.

SSC Interrupt Service Response

The SSC benchmark defines interrupt service response as the amount of time required for the first instruction of a "C" interrupt service routine (ISR) to begin executing. For this test, the auxiliary clock is used to generate interrupts at regular intervals to the CPU. The "C" ISR immediately gets the value of the auxiliary timer. Since each interrupt resets the timer value, this timestamp minus the start count is used to represent the interrupt response time. Figure 3 shows the minimum, maximum and average times for this test.
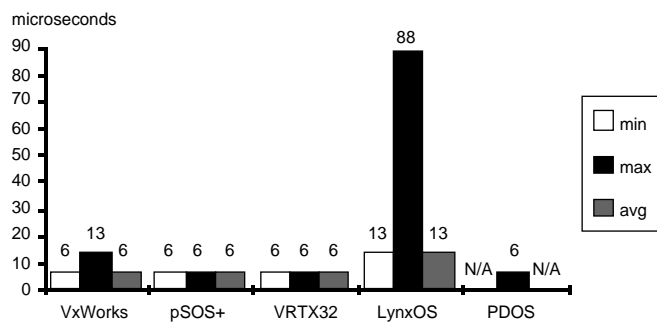
Figure 3. SSC Interrupt Response Times

Since the resolution of the timer used in this test is only 6.25 microseconds, the variations in minimum and maximum values noted are likely to be less dramatic than implied.

VxWorks Interrupt Service Response

In a separate study conducted by Wind River Systems, a different methodology is used to obtain a more precise interrupt response timing for VxWorks. This methodology takes advantage of the VxWorks shared memory backplane driver and rich interrupt handling facilities to instrument and time the interrupt path.

The shared memory backplane driver is used to allow the MVME-147 board to access a shared memory location into which a second CPU with a 1 microsecond resolution timer chip continually writes its timer value. This allows the MVME-147 board to perform timestamps with 1 microsecond resolution. The overhead in performing the timestamps is calibrated so that this time is not reflected in the final results.

VxWorks' extensive interrupt handling facilities are used to instrument the interrupt handling path in the VxWorks operating system. In VxWorks, system hardware interrupts other than those used by VxWorks are available for use by application developers. VxWorks allows C functions to be connected to any interrupt. Since interrupts cannot actually vector directly to C functions, VxWorks builds a small amount of code that saves the necessary registers, sets up the

stack with the argument to be passed, and calls the connected function. This code comprises the overhead to the C function that is incurred when an interrupt occurs.

In this benchmark, the code is modified to first take a timestamp before calling the C function, which immediately takes a second timestamp. VxWorks interrupt handling facilities are used to set the auxiliary clock vector to the address of this modified code. The interrupt response time is then calculated as the difference between the two timestamps plus the kernel interrupt latency, which is the time the kernel itself disables interrupts. This ranges between zero and 8 microseconds on an MVME-147 board. See Figure 4 for a graphical representation and results.
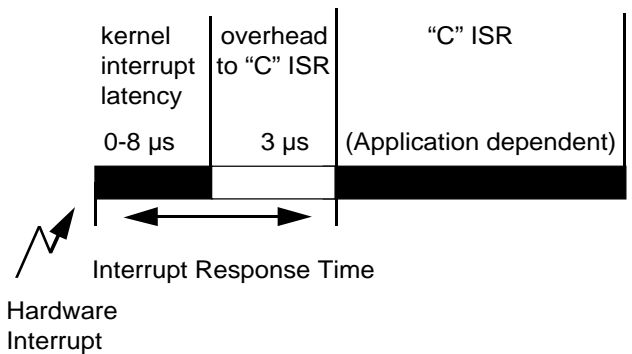

Figure 4. VxWorks Interrupt Response Time

Thus, the minimum interrupt response time for VxWorks is 3 microseconds, and the maximum is 11 microseconds. These fast response times are due in part to the fact that interrupt service code in VxWorks runs in a special context outside the context of other tasks. This means that handling an interrupt does not involve a task context switch.

SSC Task Response Time

The SSC Task Response Time benchmark measures the time it takes for a task to begin execution after an interrupt has occurred. It uses the same timing methodology as the SSC Interrupt Response Time benchmark. The highest priority task in the system blocks on a semaphore. When an interrupt occurs, the "C" ISR makes this semaphore available, unblocking the highest priority task. The time noted by the task when it resumes execution is the task response time. The results are shown in Figure 5.
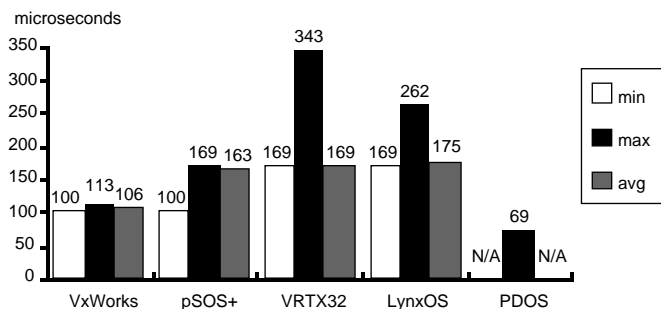
microseconds

Figure 5. SSC Task Response Times

As noted in the Eyring article featuring PDOS, the closer the minimum, maximum and average times are to each other the more deterministic the system is in its response to an interrupt. Remember, however, that these timings do not reflect preemptive latency in the kernel, which could have drastic implications on performance in systems without a minimal kernel, like PDOS.

VxWorks Task Response Time

Using the methodology described in the VxWorks Interrupt Response Time benchmark, the task response time for VxWorks can also be measured. The task response time actually includes the interrupt response time plus the time for the "C" ISR execution, rescheduling, and resuming the interrupted task. As in the SSC benchmark, a semaphore is used to block a high priority task. The "C" ISR releases the semaphore, and then the resumed task immediately performs a timestamp. Figure 6 presents a graphical representation of the results.
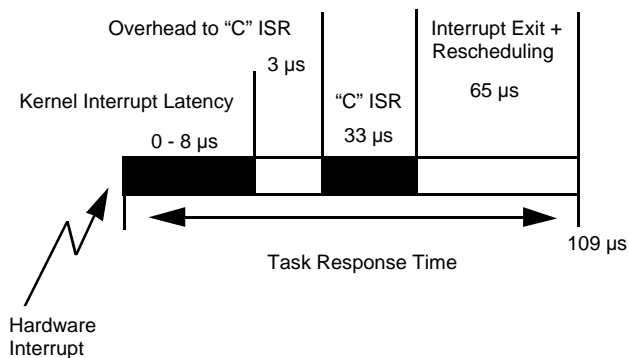
Figure 6. VxWorks Task Response Times

Thus, the overhead for handling an interrupt is a minimum of 68 microseconds and a maximum of 76 microseconds. The time for the "C" ISR is strictly application dependent. In this example, the "C" ISR takes 33 microseconds, resulting in a total task response time of 109 microseconds.

Task Context Switching

An important metric in benchmarking real-time performance is the time it takes for a high priority task to preempt a lower priority task and start executing. In general, the time it takes to switch between tasks is known as the task context switch time. This time includes saving the context of the preempted task, loading the context of the new task, and rescheduling to allow the new task to begin execution.

The SSC Benchmark uses two timings to describe the task context switch time. Both use the system clock to time a number of iterations of the test until a desired accuracy is obtained. It should be noted that many loop tests often lean toward a higher-than average execution speed on cached systems. In these tests, the number of cache hits is usually higher than the expected hit rate.

SSC Ping Suspend/Resume Task

The first SSC test uses a typical real-life scenario to measure task context switching. In this test, a low-priority task resumes a suspended high-priority task. The high priority task immediately suspends itself again, causing the cycle to repeat. The cycle itself includes two context switches, plus a task suspend and task resume. Results are shown in Figure 7.
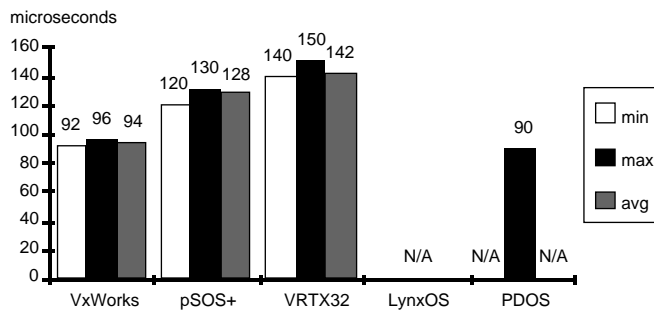
microseconds

Figure 7. SSC Ping Suspend/Resume Times

The SSC Benchmark report notes that there is no way to perform a task suspend or resume in LynxOS without using signals, therefore no times are provided.

SSC Suspend / Resume Task

The second SSC test times a task suspend and a task resume of a low-priority task that never actually executes. In this way, context switching is prevented. Subtracting this time from the SSC Ping Suspend / Resume Task test yields the time it takes to perform two task context switches. Dividing by two will provide a measurement of a single task context switch. The suspend / resume times are given in Figure 8.
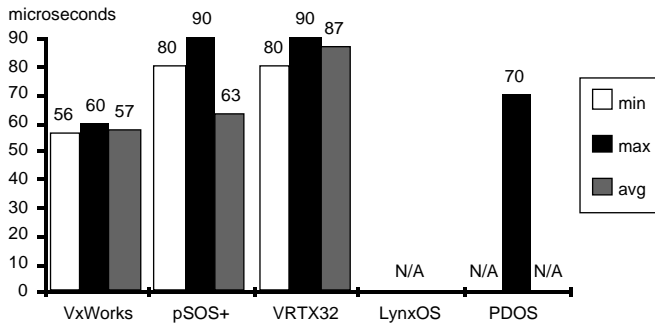
Figure 8. SSC Suspend/Resume Times

Thus, using the maximum values shown, the maximum time for a VxWorks context switch may be computed as follows:

(SSC Ping Suspend/Resume Time - SSC Suspend/Resume) ÷2
or
(96 - 60) ÷2 = 18 microseconds

Note that these timings vary depending on the particular board used. On a 25 MHz MVME-167 board, for example, a VxWorks context switch takes only 4 microseconds.

Task Synchronization

Fast synchronization among tasks is imperative in a real-time operating system. Binary semaphores are the fastest and most common mechanism for synchronizing access to critical resources among multiple tasks. Developers should realize, however, that while binary semaphores are vital for performance, they are limited in functionality. They do not address issues such as priority inversion, deletion safety, or recursive access to resources.

Priority inversion arises when a low-priority task holding a semaphore is preempted by a high-priority which then blocks trying to take the same semaphore. This results in the high-priority task being blocked for an indeterminate amount of time; any task with priority higher than the low-priority task can preempt it and delay the release of the semaphore. *Deletion safety* prevents a task from being unexpectedly deleted while holding a critical resource. Finally, *recursive access* to a semaphore is often needed by a set of routines that need access to the same resource, but also need to call each other.

VxWorks addresses all of these issues by providing two additional types of semaphores - mutual exclusion and counting semaphores. Mutual exclusion semaphores prevent priority inversion while providing deletion safety and recursive access. Counting semaphores are useful for guarding resources with multiple copies. Counting semaphores keep track of the number of times a semaphore

has been given and allow the semaphore to be taken the same number of times. Both types of semaphores give developers added flexibility and protection when designing applications.

In addition, all higher level facilities in the VxWorks operating system -- including message queues, networking, I/O system, etc. -- use mutual exclusion semaphores. This means that the entire VxWorks operating system is guaranteed to be priority inversion free with resource deletion safety. This is another important consideration for developers when comparing real-time operating systems.

SSC Ping Semaphore

The SSC Ping Semaphore test measures the time it takes for two tasks to alternate ownership of a semaphore. This includes task context switching between the two tasks. Results are shown in Figure 9.
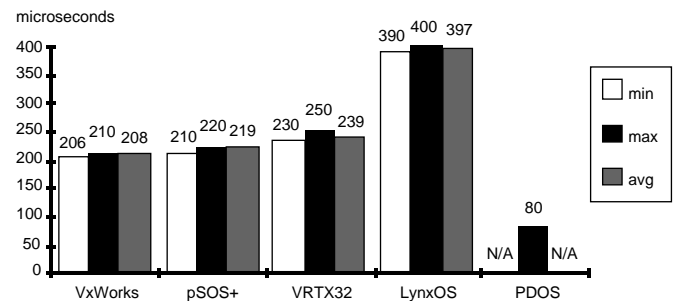

Figure 9. SSC Ping Semaphore Times

SSC Getting / Releasing Semaphore

This test simply times a give and a take of a semaphore from within the same task, thereby avoiding task context switching. See Figure 10 for timings.
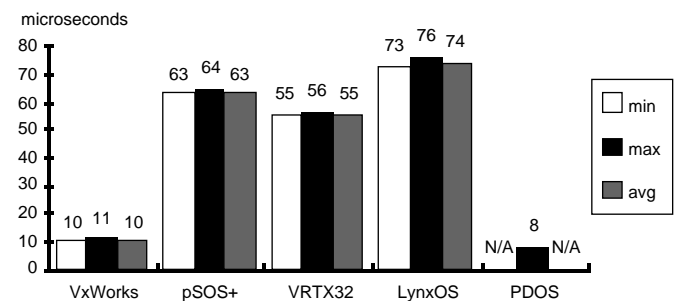

Figure 10. SSC Getting/Releasing Semaphore Times

Message Queues

Intertask communication is another important requirement of a real-time application. As noted earlier, VxWorks' message queue facilities are built on top of, rather than included in, the

kernel in order to avoid preemptive latency. In the original SSC Benchmark, the VxWorks message queue testing is done using ring buffers and semaphores to simulate fixed length message queues since no message queue facilities were available at that time. VxWorks now supports fully functional message queues capable of handling variable length messages. Most real-time operating systems provide only fixed length message queues, requiring multiple send and/or receive operations for larger messages.

With VxWorks, developers may choose either the fixed length ring buffer / semaphore method or the variable length message queue facilities. In order to maintain the integrity of the SSC Benchmark results, the original tests using ring buffers and semaphores are used to time fixed length message queues.

SSC Ping Message Queue

This SSC test measures the time it takes for two tasks to communicate with each other via a fixed length message queue. Figure 11 shows the results.
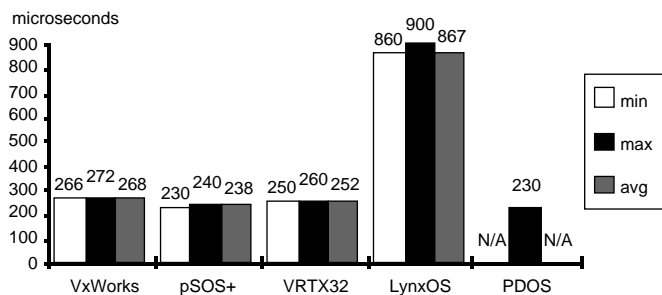
Figure 11. SSC Ping Message Queue Times

SSC Message Queue Tests

The SSC Benchmark then measures several variations of message queue operations, including the time to fill a message queue, drain a message queue, fill a message queue with priority messages at the head of the queue, and then fill and immediately drain a message queue. Results are presented in Figure 12.
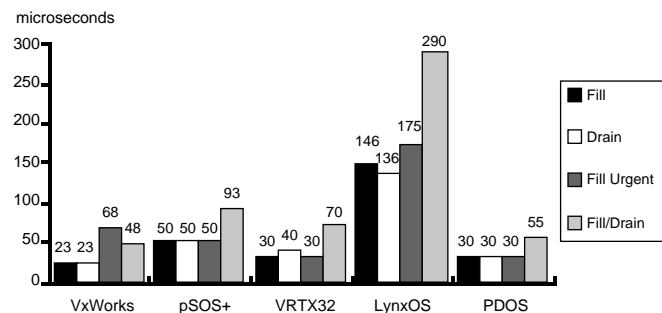

Figure 12. SSC Message Queue Tests

SSC Memory Allocation / Deallocation Tests

Memory allocation and partitioning is useful for developers wishing to exercise greater control over memory usage by an application. The VxWorks version of **malloc()** allows developers to obtain variable size blocks of memory from the system memory pool. This is an important distinction from many systems which allow for allocating only a fixed size block of memory. As with fixed length message queues, this may require multiple calls to **malloc()** to allocate all the desired memory. As this functionality has a direct effect on performance, careful consideration of variable versus fixed capabilities should be taken into account when comparing such benchmarks.

The SSC Benchmark measures the time required to allocate a number of buffers from a memory partition and return those buffers to the same partition. Results are shown in Figure 13.
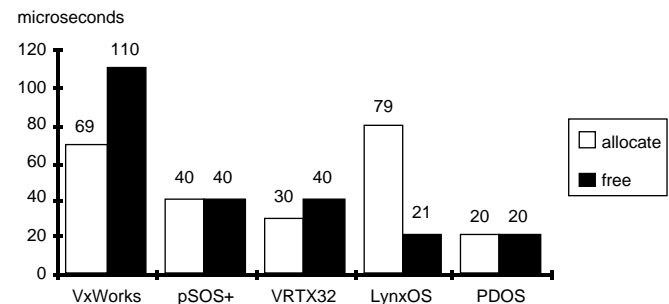

Figure 13. SSC Memory Allocation/Free Times

As a development note, many real-time developers choose to perform functions such as memory allocation during initialization to avoid affecting the performance of an application during run-time.

SSC Task Creation / Deletion

As with memory allocation, the initialization of tasks is another function which is best done during startup of an application. The SSC Task Create/Delete Benchmark measures the time it takes to create a high priority task that immediately deletes itself. The test involves context switching between the low priority task doing the creating and the high priority task that gets created. See Figure 14 for the results.
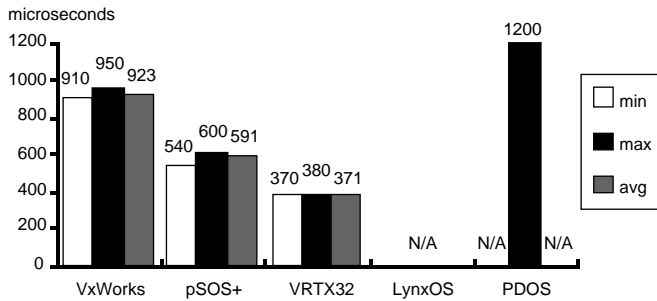
microseconds

Figure 14. SSC Task Create/Delete Times

VxWorks Task Initialization / Activation

In VxWorks, developers can use special task functions to initialize tasks before an application is ready to run. This optimizes the performance of an application which then needs only to activate the pre-initialized tasks to begin execution. The savings potential is illustrated in Figure 15.
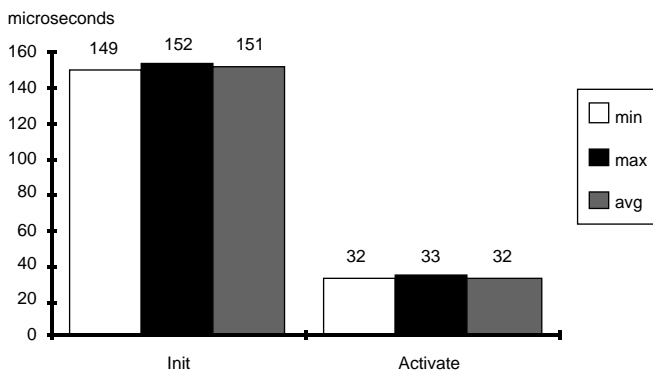
microseconds

Figure 15. VxWorks Task Init/Activate

As you can see, by initializing tasks before an application is started, the savings are significant. A task activation requires only 33 microseconds - much faster than any of the task creation times noted in the SSC Task Create/Delete Benchmark!

SSC Benchmark Conclusions

Benchmarks such as the SSC Benchmark do provide developers with some basis of performance comparison among well-known real-time operating systems. Developers, however, should consider much more than what benchmarks reveal when choosing a system. As illustrated here, considerations such as preemptive latency, kernel design, and flexibility of functionality all factor into how well a real-time operating system will perform for any given application.

VxWorks Network Throughput

In addition, developers wishing to use networking capabilities may find that kernel or basic operating system performance does not guarantee similar results in a networked environment. In VxWorks, the importance or networking tasks may be set relative to other tasks in an application, giving developers greater control over application performance.

This serves to enhance the already superb network throughput performance of VxWorks, especially in an application that must also handle multiple interrupts quickly and efficiently.

VxWorks network throughput can reach close to theoretical maximums as illustrated in Figure 16. The values represent the average throughput of a networked target using TCP/IP in kilobytes/second. A SPARCstation host continuously writes a specified buffer size to the target under test, which continuously reads the data sent.
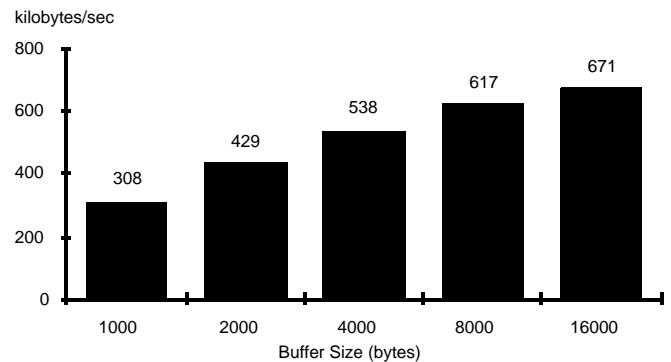
kilobytes/sec

Figure 16. VxWorks Network Throughput (kilobytes/second)

Conclusion

Choosing a real-time operating system requires developers to consider many different factors and sources of information. What is the right choice for one application may not be the correct choice for another. The only way to ensure a good match is to evaluate the needs of a particular application while at the same time considering how a real-time operating system will contribute to the design and performance of that application.

VxWorks is an example of how superb design and flexibility can improve both the performance and the overall design of any real-time application. VxWorks allows developers to choose from several alternative implementation methods in order to balance needs such as functionality versus performance. In this way, the developer controls the design of an application instead of being confined to the limits of the real-time operating system upon which it is built.

Additional Benchmark Information

Wind River Systems also makes available to customers additional sources of performance information in the form of benchmark code suites and various independent benchmark reports. Additional assistance for specific customer benchmark requests is also provided on a case by case basis, dependent on resource availability. Consult your local Wind River Systems Sales Representative for more information.

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The VxWorks Real-Time Kernel

Abstract

Real-time operating systems have evolved from monolithic entities, in the early days of embedded systems, to multi-leveled hierarchies, in which the lowest level is a real-time kernel. Multitasking, preemptive scheduling, high-speed context switching, low interrupt latency, and fast, flexible communication mechanisms are standard requirements of a modern real time kernel. Section One details kernel requirements, Section Two presents the functional details of the VxWorks® kernel, and Section Three examines VxWorks kernel benefits. Finally, Section Four contains kernel performance timings.

SECTION ONE

The Structure of Real-Time Operating Systems

The most primitive form of an operating system (OS), developed mostly during the early days of computing, is a *monolithic* entity. In such a system, modules serving different functions, such as processor management, memory management, I/O, etc., are generally independent. Their execution, however, is with the same coarse granularity with respect to one another no matter which of these modules is in use.

Due to the many different functions that need to be performed in a modern real time environment, and the inherent asynchronous and nondeterministic nature of the concurrent activities that occur in such an environment, OSs have become more complex. As a result, the monolithic organization of early OSs have been rejected in favor of a more refined internal structure.

The Hierarchical Approach– Begin with the Kernel

The best model for the internal structure of an OS consists of a hierarchy of levels, of which the lowest is the *kernel*. These levels can be viewed as an inverted pyramid, with each layer building on the functionality of the layers below. The kernel consists of only the most vital low-level functions performed by an OS. Like a monolithic OS, it provides a level of abstraction between higher levels of software and the underlying machine. However, it provides only a minimal set of operations from which the rest of the operating system can be constructed.

Requirements of a Real-Time Kernel

A kernel for a real-time OS has a number of basic requirements, dictated by the specialized real-time environment. These include:

Multitasking

Because of the asynchronous nature of events in the real world, it is important to have the ability to run a number of concurrent processes, or *tasks*. Multitasking offers a better match to real world events because it allows for multiple threads of operation corresponding to multiple discrete external events. It is the kernel's job to achieve concurrency by allocating the CPU to these tasks.

Preemptive Scheduling

Real world events have an inherent precedence; it is vitally important that this precedence be observed when allocating the CPU. In priority-based preemptive scheduling, tasks are prioritized, and the highest priority task that is ready to run (not suspended or waiting for something) at any given time is allocated the CPU. In other words, when a high-priority task becomes ready, it immediately preempts any lower-priority task that is currently running.

Fast, Flexible Intertask Communications and Synchronization

In a real-time system, there may be many tasks working as components of the same application. It is therefore important that the system provide fast, powerful communications mechanisms for communications between tasks. The kernel must also provide a synchronization mechanism for effective sharing of non-preemptible resources, or critical regions.

Easy Communications between Task and Interrupt Levels

Although real world events often arrive as interrupts, it is usually desirable to handle the associated work at task level, in order to provide effective queueing, prioritization, and reduced interrupt latency. Therefore, it is important that

mechanisms exist for communications between task level and interrupt level.

Bounded Performance

A real-time kernel must be optimized for worst-case performance, rather than throughput. A system that performs a function in 50μs consistently may be more desirable than one that averages 10μs for the function, but occasionally takes 75μs.

Special Considerations

As demands on a real-time kernel increase, it is important to consider the impact of kernel requirements to support increasingly complex facilities. These include multiprocessing, Ada, and newer, more powerful processor architectures such as RISC.

A Kernel By Any Other Name

Many commercially available "kernels" support far more than the requirements outlined above. In this respect, they are not truly kernels but rather tiny monolithic operating systems, because they include such functionality as simple memory allocation, timing and perhaps even some I/O system calls.

This classification is not just a disagreement over semantics. Later, this paper will show that it is vitally important to limit the kernel's activities and to optimize those functions.

SECTION TWO

The VxWorks Kernel: *wind*®

The VxWorks operating system is the most fully featured of any processor-independent real-time system available today. However, VxWorks is structured hierarchically, with a true kernel that is extremely small. The kernel provides only a multitasking environment, interprocess communication, and synchronization facilities. These building blocks, though, are sufficient to support the demands of VxWorks' rich set of higher level features.

In general, the kernel's operation is invisible to the user. There are several calls that the application might make for task management or synchronization that involve kernel work, but this process is invisible to the calling task. The application simply links with the appropriate VxWorks routines (normally using VxWorks' dynamic linkage facilities) and makes the calls like any other subroutine. This interface is unlike systems that require clumsy jump table interfaces which require a user to specify a kernel function by means of a small integer.

Multitasking

The fundamental role of the kernel is to provide a multitasking environment. Multitasking creates the appearance of many programs executing concurrently when, in fact, the kernel interleaves their execution on the basis of a scheduling algorithm. Each apparently independent program is called a task. Each task has its own context, which comprises the CPU environment and system resources that the task sees every time the kernel schedules it to run.

Task States

The kernel maintains the current state of each task in the system. State transitions take place as the result of kernel function calls made by the application. The following *wind* kernel states are defined as follows:

- *ready*—A task, which is not waiting for any resource other than the CPU.
- *pended*—A task, which is blocked due to the unavailability of some resource.
- *delayed*—A task, which is asleep for some period of time.
- *suspended*—A secondary state used primarily for debugging. Suspension inhibits task execution.

Upon creation, tasks enter the suspended state. Activation is necessary to make a created task enter the ready state. The activation phase is extremely fast, enabling applications to pre-create tasks and activate them in a timely manner.

Scheduler Control

Multitasking requires a scheduling algorithm to allocate the CPU to ready tasks. Priority-based preemptive scheduling is the default algorithm in VxWorks, but applications may optionally utilize round-robin selection as well.

Preemptive priority scheduling. With a preemptive priority-based scheduler, each task is assigned a priority and the kernel ensures that the CPU will be allocated the highest priority task that is ready to run. The scheduling is preemptive in that if a task becomes ready to run that has higher-priority than the current task, the kernel will immediately save the current task's context and will switch to the context of the higher priority task.

VxWorks has 256 priority levels, numbered 0 through 255. Tasks are given a priority during creation; during the course of execution a task may dynamically change its priority in order to track precedence changes in the real world. External interrupts are given precedence over any task priority, and are thus capable of preempting a task at any time.

Round-robin selection. Preemptive priority scheduling may be augmented with round-robin scheduling. A round-robin scheduling algorithm attempts to share the CPU fairly among all ready tasks of the same priority. Without round-robin scheduling, when multiple tasks of equal priority share the processor, a single task can usurp the processor, never blocking until preempted by a higher priority task and thus never giving the other equal-priority tasks a chance to run. If round-robin is enabled, the executing task's run-time counter is incremented on every clock tick. When the specified timeslice interval is completed, the counter is cleared and the task is placed at the tail of the queue of tasks at its priority. New tasks joining a given priority group are placed at the tail of the group with a run-time counter initialized to zero.

Basic Tasking Functions

Basic tasking functions for state control include the ability to create, delete, suspend and resume a task. Also, a task may make itself ineligible for execution for an arbitrary period of time by means of a sleep function.

Numerous other tasking routines provide state information gathered from a task's context. These routines include access to a task's current processor register control.

Task Deletion Problem

The *wind* kernel provides a mechanism to protect a task from unexpected deletion. Frequently, a task executing in a critical region or engaging a critical resource will be particularly important to protect. Consider the following scenario: a task obtains exclusive access to some data structure. While executing inside the critical region, the task is deleted by another task. Because the task was unable to complete the critical region, the data structure may have been left in a corrupt or inconsistent state. Furthermore, assuming the task did not get a chance to release the resource, the resource is now unavailable for use by any other task; it is essentially frozen.

Any task that tries to delete or terminate a task while deletion protection is engaged will block. When finished with its critical resource, the protected task can make itself available for deletion by disengaging the deletion protection, which unblocks any pending deleting tasks.

As demonstrated by the above scenario, task deletion protection is often coupled with mutual exclusion. Thus, for convenience and efficiency, mutual exclusion semaphores include a deletion protection option. (See "Mutual Exclusion Semaphores" for more information.)

Intertask Communication

To fully harness the power of a multitasking system, the *wind* kernel provides a rich set of intertask communication and synchronization mechanisms. It is these communication facilities that allow independent tasks of an application to coordinate their actions.

Shared Address Space

Underlying the *wind* kernel's intertask communications mechanisms is the shared address space in which all tasks exist. With shared address space, tasks may communicate freely by consulting pointers to shared structures. Pipes need not map a special piece of memory into the address space of two communicating tasks.

Unfortunately, with the benefits of shared address space come the dangers of errant accesses to unprotected memory. The UNIX operating system isolates processes to provide such protection, but currently at too great a performance cost for a real time operating system.

Mutual Exclusion

While a shared address space simplifies exchange of data, interlocking access to avoid contention is crucial. Many mechanisms exist to obtain exclusive access to a resource differing only in the scope for which the exclusion applies. Methods of mutual exclusion include disabling interrupts, disabling preemption, and resource locking with semaphores.

Interrupt locks. The most powerful mutual exclusion method is disabling of interrupts. Such a lock guarantees exclusive access to the CPU. While this certainly solves problems involving mutual exclusion, it is largely inappropriate for real time because it prevents the system from responding to external events for the duration of the lock. High interrupt latency is unacceptable in applications for which deterministic response is a must.

Preemption locks. Disabling preemption offers a somewhat less restrictive form of mutual exclusion. While no other task will be allowed to preempt the current executing task, interrupt service routines will be accepted. This may also lead to poor real time response, as interrupts that unblock tasks can fall prey to large preemptive latencies; as a result, high priority tasks that are eligible to execute may be forced to wait an unacceptable period of time before executing. To avoid this situation, semaphores should be used for mutual exclusion whenever possible.

Mutual exclusion semaphores. Semaphores are the primary means to interlock access to some shared resource. Unlike disabling interrupts or preemption, semaphores limit the

scope of the mutual exclusion to only the associated resource. In this technique, a semaphore is created to guard the resource. Semaphores in VxWorks are modeled after Dijkstra's P() and V() operations.

When a task takes a semaphore, P(), one of two things happens, depending on whether the semaphore was set or reset at the time of the call. If the semaphore was set, then the semaphore is reset and the task continues execution immediately. If the semaphore was reset, then the task is blocked and enters the pended state, waiting for that semaphore.

When a task gives a semaphore, V(), one of several things happens. If the semaphore was already set at the time of the call, then giving the semaphore has no effect at all. If the semaphore was reset and no task was waiting to take it, then the semaphore is simply set. If the semaphore was reset and one or more tasks are pended trying to take it, then the highest priority task is unblocked and the semaphore is left reset.

By associating a semaphore with some resource, mutual exclusion can be assured. When a task wants to access the resource, it must first take that semaphore. So long as the task keeps the semaphore, all other tasks seeking access to the resource will be blocked from taking the semaphore. When the task is finished with the resource, it gives back the semaphore, which allows another task waiting for that semaphore to gain access to the resource.

The wind kernel has tailored a binary semaphore to address problems inherent in mutual exclusion. These problems are deletion protection of resource owners, and priority inversion resulting from resource contention.

*   *Deletion protection*. A rarely addressed problem of mutual exclusion involves task deletion. Within a critical region guarded by semaphores, it is often desirable to protect the executing task from unexpected deletion. Deleting a task executing in a critical region can be catastrophic. The resource could be left in a corrupt state and the semaphore guarding the resource left unavailable, effectively shutting off access to thie resource. Often deletion protection goes hand-in-hand with mutual exclusion. For this reason, the mutual exclusion semaphore offers an option which enables an implicit use of the task deletion protection mechanism described earlier.

*   *Priority inversion/priority inheritance*. Priority inversion arises when a higher-priority task is forced to wait an indefinite period of time for the completion of a lower-priority task. Consider the following scenario:

T1, T2, and T3 are tasks of high, medium, and low priority, respectively. T3 has acquired some resource by taking its associated semaphore. When T1 preempts T3 and contends for the resource by taking the same semaphore, it becomes blocked. If we could be assured that T1 would be blocked no longer than the time it normally takes T3 to finish with the resource, the situation would not be particularly problematic. After all, the resource is non-preemptible. However, the low-priority task is vulnerable to preemption by medium-priority tasks; a preempting task such as T2 will inhibit T3 from relinquishing the resource. This condition could persist, blocking T1 for an indefinite period of time. This condition is called priority inversion because, despite the priority-based scheduler, a higher priority task is waiting for a lower priority task to finish.

The mutual exclusion semaphore has an additional option which enables a priority inheritance algorithm. Priority inheritance solves the problem of priority inversion by elevating the priority of T3 to the priority of T1 during the time T1 is blocked waiting for T3 to finish. This protects T3, and indirectly T1, from preemption by T2. Stated more generally, the priority inheritance protocol assures that a task that owns a resource will execute at the priority of the highest task currently blocked on that resource. When execution is complete, the task gives up the resource and returns to its normal, or standard, priority. Hence, the "inheriting" task is protected from preemption by any tasks of intermediate priority.

Synchronization

The other common use of semaphores is as a task synchronization mechanism. In this case, a semaphore may represent a condition or event for which tasks may wait. Initially the semaphore is reset. A task or interrupt service routine may signal the occurrence of an event by giving the semaphore. A dedicated task waiting for the semaphore will block until the event occurs and the semaphore is given. Once unblocked, the task can perform whatever event handling is appropriate.

Note that the synchronization application of semaphores is particularly useful in offloading an interrupt service routine of lengthy event handling, thus improving interrupt response times.

Message Queues

Message queues provide a low level facility to exchange variable length messages from a task or interrupt service routine to another task. This facility is similar to pipes in function, but with slightly less overhead.

Pipes, Sockets, Remote Procedure Calls, and Beyond

Numerous higher-level VxWorks facilities provide even higher abstractions of intertask communications including pipes, TCP/IP sockets, remote procedure calls (RPCs), and more. In keeping with design goals of crafting the kernel as a minimal set of functions sufficient to support higher level facilities, these features are based on the kernel synchronization methods described above.

Kernel Design Benefits

The key design feature of the *wind* kernel is a minimal preemptive latency. Other major design benefits include an unprecedented level of configurability, extensibility for unanticipated application requirements, and portability for quick utilization of cutting-edge microprocessor developments.

Minimizing Preemptive Latency

As discussed earlier, disabling preemption is a common way to achieve mutual exclusion during critical sections of code. The undesirable side effect of this technique is a high preemptive latency, which can be minimized by using this mechanism judiciously as well as keeping critical sections compact. Whenever possible, a semaphore should be used as an alternative to disabling preemption for the purpose of mutual exclusion. Unfortunately, even extensive use of semaphores does not address all the sources of preemptive latency. The kernel itself is another source of preemptive latency. To understand why, we must better understand the mutual exclusion needs of the kernel.

Kernel Level Versus Task Level

In any multitasking system, the bulk of the application takes place within the context of one or more tasks. However, there are times when the CPU is not in any task context at all. These times occur when the kernel is effecting changes to the internal queues or deciding which tasks to dispatch. During these times, the CPU is at *kernel level*, instead of *task level.*

Preemptive Latency

In order for the kernel to safely access its internal structures, mutual exclusion must be achieved. With no task context associated with kernel level, the kernel cannot use a semaphore to guard the internal lists. Instead, the kernel uses a technique of work deferral as a means of mutual exclusion. When the kernel is engaged, functions arriving from interrupt service routines are not invoked directly, but rather the work is deferred by queueing the job to the kernel work queue. The

kernel work queue is emptied once the kernel has finished performing the initial request.

In effect, the system will not react to functions that arrive at the kernel while it is busy performing some already-initiated service. A simpler way to view this situation is to view the kernel state as analogous to disabling preemption. As discussed earlier, preemptive latency is undesirable in a real time system because it slows reaction time to events that call for rescheduling of application tasks.

Although it is impossible for an operating system to completely avoid time spent at kernel level, during which preemption is locked out, it is vital to minimize such time. This demonstrates the major reason to minimize the functions performed by the kernel alone, and is a strong argument against the monolithic approach. In one popular real time OS, for example, every single function acts at kernel level. This means that while a low priority task is making a call to allocate memory, get task information, etc., all higher priority tasks are locked out from preempting.

A Minimal Kernel

Having stated the benefits of a minimal kernel, and described the necessary building blocks suitable for higher-level OS facilities, we now utilize these primitives to implement a traditional kernel level facility that is implemented as a task level facility in VxWorks: the memory manager.

In this example, consider the user-callable subroutine *malloc*, which allocates and returns a pointer to a block of memory of some requested size. Assuming that the free memory is found by traversing a queue of free blocks, a semaphore must be used to guard this non-preemptible multiuser resource. The operations to allocate memory are:

- Obtain the mutual exclusion semaphore
- Search list for free block
- Release the mutual exclusion semaphore

The important point to notice is that the potentially lengthy search for a large enough free block takes place within the calling task's context. It is all fully preemptible by higher priority tasks (except for a small window of time within the semaphore calls).

Contrast this with the memory allocation procedure for a more standard, monolithic real time kernel. Using this model, the operations to allocate memory are:

- Enter the kernel
- Search list for free block
- Leave the kernel

The entire memory allocation process takes place at kernel level, with task preemption locked out. If a higher priority task becomes ready during that time, it must wait until the kernel completes the memory allocation for the lower priority task. Worse, many kernels even lock out interrupts for some of this time.

Task-Level Operating System Services

Wind River Systems' real-time operating system, VxWorks, demonstrates that a minimal kernel of this design is sufficient. The VxWorks operating system—the most fully featured of any processor-independent real-time system available today— is structured hierarchically, with a true kernel that is extremely small.

VxWorks provides an enormous amount of functionality beyond the kernel. It includes memory management; a complete port of the BSD 4.3 network package; TCP/IP; Network File System (NFS); Remote Procedure Calls (RPC); a UNIX compatible linking loader; a C language interpretive shell; various types of timers; performance monitoring utilities; debugging tools; additional communications tools such as pipes, signals, and sockets; I/O and file systems; and hundreds of utility routines. However, none of these run at kernel level, and therefore none of them lock out interrupts or task preemption.

Configurability

Real time applications have divergent kernel requirements. No kernel will ever have perfect design tradeoffs that will satisfy everyone. A kernel can, however, be configurable to allow tuning of certain performance characteristics—in effect, allowing tailoring of the runtime system to best suit the needs of an application. Unprecedented kernel configurability is provided to applications in the form of user-selectable kernel queuing algorithms.

Queuing Strategy

Queuing libraries in VxWorks are implemented separate from the kernel queue facilities that use them, thus providing flexibility for the future implementation of new queuing methods.

There are a variety of kernel queues in VxWorks. The ready queue is a priority-sorted queue of all tasks eligible for scheduling. The tick queue is used by functions involving timing. The semaphore is the list of blocked tasks waiting for a semaphore. The active queue is a FIFO (first-in-first-out) list of all tasks in the system. Each of these specialized queues requires a different queuing algorithm. Instead of

burying the algorithms deep in the kernel, they have been extracted into autonomous, interchangeable queuing libraries. This flexibility forms the basis for special-purpose configuration needs.

Extensibility

The ability to support unanticipated kernel extensions is just as important as the configurability of existing functionality. The simple kernel interface and mutual exclusion methods make extensions of kernel level facilities extremely easy; in some cases, applications need only to take advantage of kernel callouts or hooks to realize a particular extension.

Internal hooks. To allow additional task-related facilities to be added to the system without modifying the kernel, VxWorks provides task create, switch, and delete hooks. These enable additional routines to be invoked whenever a task is created, a context switch occurs, or a task is deleted. These hooks may utilize spare fields within the context of a task to embellish the tasking features of the *wind* kernel.

Future Considerations

There are a number of system functions which are now becoming important, and which have implications for kernel design with regard to preemptive latency. Although a complete discussion of these issues is beyond the scope of this paper, it is worth noting some of them briefly.

RISC/CISC. Designing a CPU-independent operating system is always a challenge. With the new RISC (reduced instruction set, such as SPARC, MIPS, or 80960) processors now becoming popular, these difficulties are aggravated. In order to work effectively in the RISC environment, kernels and operating systems need the flexibility to implement radically different strategies.

For example, consider the procedure the kernel follows during a task context switch. On a CISC (complex instruction set, such as the 680x0 or 80386) CPU, the kernel saves a complete register set for each task, and swaps those registers in and out with the running task. With a RISC machine, this might not be reasonable because of the large number of registers involved. Therefore, the kernel might need a more sophisticated strategy, such as caching registers for tasks, allowing the application to dedicate some registers to particular tasks, for example.

Portability. In an effort to make the wind kernel readily available on architectures as they appear, a portable version of the kernel exists. This facilitates any porting effort by getting a functional, while not optimal, solution "off the ground."

Multiprocessing. Internal facilities to a real-time kernel are required to support "tightly coupled" multiprocessing needs. Such facilities would include, in the ideal case, the ability to make any kernel call remotely, from one processor to another. This would include semaphore calls (for interprocessor synchronization) and tasking calls (to control tasks on other CPUs). This complexity will undoubtedly add overhead to kernel-level facilities, but many services such as object naming and identification could be executed at task level. One principal advantage of retaining a minimal kernel in a multiprocessing system is the ability for fine-grain interlocking of processors. Larger kernels spend excessive time at kernel level and are only capable of coarse-grain interlocking.

Important Metrics of a Real-Time Operating Kernel

Many performance characteristics are used to compare existing real-time kernels. These include:

High-speed context switch

Because of the intense multitasking nature of real-time systems, it is important that the system be able to switch from one task to another quickly. In time-sharing systems such as UNIX, context switch times are in the many-ms range. The wind kernel performs a raw context switch in 17 µs.

Minimal synchronization overhead

Because the synchronization method is the primary means to obtain mutual exclusion to a resource, it is important that the overhead involved in these operations is minimized. Under VxWorks the time to give a binary semaphore and take it back it 8 µs.

Minimal interrupt latency

Because events from the outside world generally come in as interrupts, it is important that the OS handle those interrupts promptly. A kernel must disable interrupts during the manipulation of some critical structures. To reduce interrupt latency, it is vital that these times are minimized. The interrupt latency of the wind kernel is than 10 µs.

Effect of Preemptive Latency on Benchmarks

With a myriad of real-time solutions being offered to the application engineer, benchmarks are playing an increasing role in the evaluation of a vendor's products. Unlike context switch time and interrupt latency, preemptive latency is very difficult to measure. For this reason it is rarely even mentioned in most specifications. But consider how worthless a claim of a constant-time context switch (independent of the number of tasks) of 50 µs is when the same kernel regularly disables the ability to context switch for hundreds of µs. Apart from being difficult to gauge, preemptive latency can therefore undermine the validity of many benchmarks.

The primary design goal of the wind kernel was to keep preemptive latency as low as possible by reducing the kernel to its core minimum. Kernels that include ornate facilities at the kernel level will be particularly vulnerable to high preemptive latency.

Conclusion

To meet the increasing requirements for real-time kernels to satisfy the needs of new areas of interest such as alternative scheduling algorithms, multiprocessing, Ada, and RISC architectures, the wind kernel was designed from the outset with flexibility and configurability in mind. Its uncompromising leading-edge performance will define a new standard for real-time application requirements.

Tornado Development Environment

The embedded systems industry is in crisis. Driven by several factors—including the emergence of new low-cost, application-specific, 32-bit embedded microprocessors at an astounding rate—this crisis is affecting both the traditional embedded system software engineer and the unsuspecting automotive, telecom, or printer engineer who suddenly finds himself relying heavily on software to add value to his product. More embedded system applications, increasingly complex software, and the need to deliver feature-rich applications under tremendous technical constraints all add to this industry-wide dilemma. Through it all, the embedded community shares one overriding goal—to bring more competitive products to market faster and within budget.

The key to achieving this time-to-market goal is in the selection of appropriate tools to shorten the development cycle through improved productivity. Ideally this would mean a turnkey development solution to allow quick startup, with a wide variety of powerful coordinated tools and a rich runtime system.

While most tools vendors and developers have been keenly aware of this need, the nature of the embedded environment has presented obstacles previously considered insurmountable: poor communication between the host development system and the target system where the code actually runs, limited target resources (such as memory and I/O), and a multitude of specialized microprocessors which are complex to program. Most tools remain primitive and text-based, limited to compilers and source level debuggers. Integration among tools, if present at all, is poor. The net result has been an inadequate development environment for embedded applications, with crippled productivity and valuable time wasted in the creation of infrastructure and forcing integration.

Recent advances in the embedded market have begun to address these issues. Wind River Systems' introduction of the WindPower™ development tools in the early 1990s—WindView™, the industry's first system visualization tool for detecting and solving system-level problems; StethoScope, a real-time data visualization, profiling, and debugging tool for analyzing applications; and Wind C++ Gateway for ObjectCenter, a link between the VxWorks® real-time operating system and the user-friendly ObjectCenter C++ development environment—is one example of how vendors are responding to developers' needs.

However, even these graphically-oriented tools are not usable in all environments, and their capabilities are limited by the target resources and connection bandwidth.

To address the embedded developer's needs more fully, Wind River Systems introduces Tornado™—the next-generation development environment for embedded applications. Completely integrated and intuitive, Tornado is a cross-development environment ideal for the embedded market. For the first time, developers have a turnkey solution that is completely open and extensible—and available for both UNIX- and Microsoft Windows-based hosts.

Tornado Design Goals

Tornado is scalable across a wide variety of products from small, resource-constrained embedded targets to large-scale multi-processing systems. The Tornado architecture allows powerful tools to be utilized independent of resources on the target or the communication mechanism. The embedded system developer can finally use any tool with any target over any connection.

Tornado's design focuses on the developer, providing a visual and intuitive environment that is easily extended and customized. The powerful array of fully integrated tools helps shorten the development cycle by improving developer productivity.

Finally, Tornado is a completely open environment which is designed to be customized and extended by the developer. Its open interfaces make it easy to integrate other development tools, both hardware and software, to further improve productivity.

Tornado Design Philosophy

Tornado consists of three highly integrated components: the Tornado suite of tools, a set of powerful cross-development tools and utilities; the VxWorks run-time system, a high performance scalable real-time operating system which executes on the target processor; and a full range of host-target communications options such as Ethernet, serial line, in circuit emulator (ICE) or ROM emulator.

With the introduction of Tornado, Wind River has eliminated many of the dependencies between the host and target that characterize a traditional cross-development environment. The development environment can now support any connection strategy necessary for effective host-target communication, and the available tool functionality is the same regardless of the connection type.

To solve the problems of limited host-target communication and limited target resources, Wind River Systems migrated the traditional target-dependent development tools to the host system, including the shell, loader and symbol table. (For developers with sufficient target resources, these tools can still be used on the target). By shifting these tools to the host, the system no longer needs additional time and bandwidth to send and retrieve information between the target and host systems—thus alleviating the requirement for a high bandwidth connection. In addition, the target system has more resources available for the application as memory is not consumed by these tools nor by a potentially very large symbol table.

The technology which enables this independence of communication mechanism and target resource lies in two key Tornado components: the target agent and the target server. These two facilities partner to provide high-end development functionality to low-end target systems.

All Tools for All Targets: The Target Agent

This migration of tools from target to host is made possible by the insertion of a scalable agent on the target. The target agent is the critical component that connects the Tornado host-resident tools to the target run-time system. All Tornado tools are represented on the target by the target agent. The target agent gives the target an unprecedented level of independence from the host system. It is a highly compact implementation of the core services necessary to respond to requests from the Tornado tools. These requests include memory transactions, notification services for breakpoints and other events on the target, virtual I/O support, and task control. The agent responds to requests transmitted by the target server, and replies with the results.

The agent synthesizes two breakpoint strategies: task-specific breakpoints and system-wide breakpoints. The agent can execute in either mode and switches between them on demand. This greatly simplifies debugging (thus shortening the development cycle) of any aspect of an embedded application—be it a task, an interrupt service routine, or the kernel itself.

The agent is independent of the VxWorks run-time system, interfacing with run-time services indirectly so that it can take advantage of kernel features when they are present, but without requiring them. The agent's driver interface is also independent of the run-time, because it avoids the VxWorks I/O system. Drivers for the agent are raw drivers that can operate in either a polling or an interrupt-driven mode. This run-time independence means that the target agent can execute before the kernel is running, simplifying the bring-up of the operating system on custom hardware.

A key capability of the agent is to service the requests of the host-resident object-module loader. Given the incremental loading capabilities of Tornado, it is quite common to configure the target with the agent linked into the run-time and stored in ROM. When started, the target server automatically bootstraps the target symbol table with the symbol table of the target executable. From this point on, all downloads are incremental in nature, greatly reducing startup and download time.

The agent itself is scalable; one can minimally configure the agent to exclude virtually all features (including breakpoint support) for creation of final-production configurations that still allow field testing. In such a configuration, the target server dynamically loads target agent functionality "on demand."

Even configured with all available functionality, the target agent is minimally intrusive during normal development and leaves as many resources as possible on the target for use by the application.

All Tools for All Targets: The Target Server

In much the same way that the target agent gives the target independence from the tools, the host-based target server allows the tools to be independent of the target system. The target server is the centerpiece of the Tornado architecture on the host system, and the foundation of the host-based Tornado tools. There is one server per target; all host tools access the target through this server, whose function it is to satisfy the tool requests by breaking each request into the necessary transactions with the target agent. The target server manages the details of the target connection—whatever method is

chosen—so that individual tools need not concern themselves with host-to-target transport mechanisms. The target server is also outfitted with features specifically intended to improve the performance of the cross-development structure. These features include a target memory cache, host-based target memory management, and a streamlined host-target protocol to reduce communication traffic.

In some cases, the server passes a tool's service request directly to the target agent. In other cases, requests can be fulfilled entirely within the target server on the host. For example, when a target-memory read hits a memory region already cached in the target server, no actual host-to-target transaction is needed.

The target server also allocates target memory from a pool dedicated to the host tools, and manages the target's symbol table on the host. This permits the server to do most of the work of dynamic linking (address resolution) on the host system, before downloading a new module to the target— resulting in a large reduction in total target requests. The management of a separate pool of memory for host-tool requests avoids degrading a target application's real-time performance by avoiding fragmentation of the target application's memory pool.

A target server need not reside on the same host as the Tornado tools, as long as the tools have network access to the host where the target server is running. In this way, target servers can be located on a host best suited to serve the target because of the availability of appropriate peripheral hardware, or because of geographical constraints.

The target server is essentially a "tools broker." With it, the tools are both self-aware and environment-aware—making it possible for tools to work together automatically. Before Tornado, it was very difficult for tools from different sources to "talk" to each other. Now, not only are tools are aware of other tools connected to the system, they can also take advantage of their capabilities. For instance, a system visualization tool like WindView can collect data that can then be used by the PERTS tool from TriPacific for rate-monotonic scheduling.

The target agent and the host-based target server, along with the Tornado registry which keeps track of all available target hardware at a particular site, form the basis of the Tornado framework. With these three pieces, Wind River was able to expand the development environment by removing the barriers of limited host-target communication, limited target resources, and poor inter-tool coordination.

Open Environment

To fulfill the need for a visual and intuitive development foundation that can be easily extended and customized, Tornado is an open environment. This was accomplished through a variety of means including the adoption of Tool Command Language (Tcl) for easy extensibility, the use of dynamically linked libraries (DLLs) for loading and unloading of object files, and the publication of all the Tornado Application Programming Interfaces (APIs).

The published APIs provide for an unparalleled amount of extensibility and customization. Every aspect of Tornado, from the overall look-and-feel, to the object module formats (OMFs) supported, is accessible to Tornado users and partners. Much of Tornado is implemented in Tcl; source code is automatically included because Tcl is an interpreted language. By virtue of their Tcl implementation, Tornado facilities for target inspection and manipulation are available for customization, extension, or simply for their educational value. This allows customers to add new commands and facilities, or to change the way existing features work to better fit their needs. And Tornado goes further yet: all aspects of the user interface are under user control. From forms to buttons to menu items, everything about the Tornado environment can be customized.

Plug and Play Framework

The open environment is one of the greatest advantages of Tornado. By making it easy to manipulate the system, Tornado facilitates the integration of a wide variety of third-party and customer tools as well as the customization of Tornado tools provided by Wind River Systems. A testament to the ease of integration, a diverse array of third-party tools were available at launch from companies including The MathWorks, ObjecTime Limited, Real Time Innovations, TriPacific, and XLNT Designs.

The overall result of this "plug and play" environment is the long-awaited arrival of high-level, more powerful tools in the embedded market. Third parties and developers can now concentrate on raising the level at which the product is built. These new tools will leverage the expertise of both the software engineer and the application engineer.

Wind River Tools

The most visible part of the Tornado development environment is its rich collection of host-resident tools that allow developers to build, manage, and visualize the application on the target development system. These tools focus on the developer's need for interactive response,

interpretive interfaces and incremental application development. The Tornado architecture provide the mechanism to make the tools available even to the most resource-restricted target system.

With a high level of integration, these tools give the developer a feeling of being close to the target system, reducing the cycle time between the development of an idea and the receipt of feedback on an implementation. The following paragraphs provide more detail on each of these tools. In combination, the Tornado tools suite provides a comprehensive high-level solution to the broadest range of embedded and real-time development challenges.

The Launcher

The Tornado launcher lets the developer start, manage, and monitor a pool of target servers, and connects any of the interactive Tornado tools to the target server of choice. When a particular target server is selected, the launcher shows information about the hardware and software environment on the target, as well as monitoring and reporting on any Tornado tools currently attached to that target. Targets can be reserved for private use or shared with others.

In many ways, the launcher is the central Tornado control panel. Besides providing a convenient starting point for activating Tornado tools, the launcher also ties the Tornado user community together by providing access to Wind River Systems publications on the Internet, as well as customer support, user group functions, and third-party news and information. The extensive worldwide network of developers provides a wealth of knowledge and expertise to all Tornado users, including Wind River developers themselves.

The GNU Toolkit

Tornado includes the GNU compiler for C and C++ programs, as well as a collection of supporting tools that provide a complete development tool chain: cpp, gcc, make, ld, as, and binary utilities.

These tools are enhanced, commercial versions of the leading-edge GNU tools originally developed by the Free Software Foundation. Users of the GNU tools benefit from the dynamic FSF development environment as well as from Wind River Systems' full productization, support, and integration. By using the world's most exercised compiler, users also benefit from the most widely supported host-target combination— allowing unprecedented mobility from one platform to another.

CrossWind: The Source-Level Debugger

The remote source-level debugger, CrossWind™, is an extended version of the popular GNU Source-Level Debugger (GDB). The most visible CrossWind extension to GDB is its straightforward graphical user interface which provides easy access to the considerable power of the GDB backend. CrossWind also includes a comprehensive Tcl scripting interface that allows the developer to create sophisticated debugger macros or extend CrossWind for specific application requirements. For maximum flexibility, the CrossWind command panel synthesizes both the GDB command-line interface and the facilities of WindSh™, the Tornado shell.

Using CrossWind on the host, the developer can spawn and debug tasks on the target run-time system. CrossWind can also be attached to already-running tasks spawned from an application or from either the Tornado shell or the target-resident shell. CrossWind supports both application breakpoints and system breakpoints. Application code can be viewed as high-level C or C++ source, as assembly-level code, or in a mixed mode that shows both the high-level source code and the corresponding assembly code.

CrossWind incorporates a variety of display windows for source, registers, locals, stack frame, memory and so on. As a key development tool, CrossWind is packed with powerful yet easy to use features, such as the capability to "escape" from a loop by dragging and dropping the program counter indicator.

WindSh: The Shell Interpreter

WindSh is a command shell that provides interactive access from the host to all run-time facilities. The shell provides a simple but powerful capability: it can interpret and execute almost all C-language expressions. It also supports C++, including "demangling" to allow developers to refer to symbols in the same form as used by the original C++ source code.

The shell is a versatile and powerful tool. It can be used to call run-time system functions, to call any application function, to examine and set application variables, to create new variables, to examine and modify memory, and even to perform general calculations with all C operators. The shell also provides the essential debugging capabilities, including breakpoints, single stepping, stack checking, and disassembly. All interaction with the shell is symbolic in nature, since the shell has access to the symbol table managed by the target server.

From the shell, the developer can incrementally download application libraries, display system and task status, and

debug tasks, device drivers, and interrupt service routines. This interactive environment with incremental linking allows for a highly productive "fix and go" development cycle, where the application can be built and tested piece by piece.

The interpreter maintains a command history and permits command-line editing. The shell can also redirect standard input and standard output, including the input and output to the virtual I/O channels supported by the target agent.

For even more versatile shell scripting and target control, the Tornado shell includes a complete Tcl interpreter as well as the C interpreter. This allows the shell to be extended and customized: new commands can be added, display mechanisms can be changed, and even new tools can be written on the shell infrastructure.

The Tornado shell illustrates the revolutionary capabilities of the Tornado architecture, by making a phenomenal amount of power available to even the most resource-restricted target system.

Browser

The Tornado browser is a graphical companion to the Tornado shell. Where the shell includes "show routines" to retrieve information on system objects, the browser allows graphical inspection. The browser provides visibility into memory allocation and all system objects including tasks, message queues, semaphores, and so on. The information on these objects is updated either periodically or on demand.

In its main window, the browser summarizes active tasks (classified as system tasks or application tasks), memory consumption, and the current executable's memory map. Using auxiliary browser windows, the developer can also monitor the state of particular tasks, including register usage, priority, and other task attributes; comparative CPU usage by the entire collection of tasks; stack consumption by all tasks; the structure of loaded object modules; and operating-system objects including semaphores, message queues, memory partitions, and watchdog timers.

The browser makes it simple to monitor the state of the runtime system and applications. As inspected objects change, their windows are updated with highlights to reflect new values. Objects are displayed in an intuitive manner, often with collapsible "treeviews" to hide or show information.

Much of the browser is written in Tcl, allowing considerable customization. For example, the developer could choose a special mechanism to display a new object type, or write a

script to perform some error recovery function whenever margins were exceeded on stack or memory usage.

WindConfig: Target System Configuration

The VxWorks operating system is designed to be reconfigured by the developer to include the set of facilities which are appropriate for the application. WindConfig speeds and simplifies this process of reconfiguring and rebuilding by offering a graphical interface to the operating system configuration mechanism. WindConfig allows selection from over one hundred scalable features that make up the VxWorks run-time environment, and generates and archives a configuration of the board support package to match this selection.

WindConfig describes configurable features dynamically, displays parallel lists of included and excluded features, and makes the process of assembling the right collection of features a simple point-and- click activity. WindConfig also manages an archive of alternative configurations, and allows the developer to attach to each configuration a list of any application object modules that are to be linked statically with the run-time. This allows multiple configurations to be maintained, such as low and high end versions, or separate builds for debugging and production.

VxWorks

The Tornado development environment includes the industry-standard VxWorks real-time operating system. Introduced in 1987, VxWorks incorporates a state-of-the art, object-oriented microkernel design which is fast, efficient, and highly scalable. The rich, 1100+ function API provides a wide array of facilities, from real-time kernel functions to networking to utility routines such as buffer and list management. The high degree of modularity allows developers to configure the operating system to include just the set of facilities required, with over 100 functional "granules" to choose from.

Via the target agent, all development tools remain fully functional as the operating system is scaled down. This means that even a 20K operating system retains full use of the shell, browser, and debugger.

Despite the radical shift in the Tornado tools architecture, the VxWorks API remains unchanged, and retains complete backward compatibility with previous releases.

C and C++ Support

Tornado incorporates full support for both C and C++ languages, with bundled compilers and tight integration throughout the development environment. Full run-time support for C++, loader support for static constructors and destructors, and C++ debugging features are all provided in the base package.

To support object-oriented development and accelerate application development, a set of optional C++ class libraries is available. Collectively entitled the Wind Foundation Classes™, this set of C++ class libraries packs commonly-needed functionality into a form that can be easily used in applications. It includes VxWorks wrapper classes (which encapsulate VxWorks objects such as modules, tasks, message queues, and semaphores), Tools.h++ and C++ Booch components from RogueWave Software, and the iostreams class library.

The Internet

Tornado uses the Internet to help shorten the development cycle. Developers can take advantage of on-line documentation, on-line licensing and registration, on-line support, dedicated Web pages, on-line code examples, and remote access to embedded targets. Third-party and customer tools can also utilize these Internet features.

Turnkey Development

The issues discussed earlier—limited host-target communication, limited target resources, and poorly integrated tools have historically made it very difficult for an embedded system developer to maximize productivity. Tornado not only removes these barriers, but provides a complete, turnkey environment to cut startup costs and allow development to begin quickly.

In summary, Tornado is the most dramatic advance in the embedded systems industry since the introduction of Wind River's VxWorks, the current cross-development standard, in 1987. Tornado is a new model for embedded systems development: a powerful framework of productivity enhancing tools, easy to port, easy to configure, easy to extend and customize—and free at last from target resource constraints.

Appendixes

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Agilent Technologies

Algorithmics Ltd.

Apogee Software, Inc.

Applied Microsystems Corporation

Baton Rouge International, Inc.

Cogent Computer Systems, Inc.

Corelis, Inc.

Crescent Heart Software

Cygnus Solutions

DENSAN Systems, Inc.

digital logic instruments gmbh

Embedded Performance, Inc.

Express Logic, Inc.

Galileo Technology, Inc.

Green Hills Software, Inc.

Insignia Solutions

JMI Software Systems, Inc.

Microsoft Corporation

NEC Electronics Inc.

Viosoft Corporation

Wind River Systems, Inc.

Accelerated Technology, Inc. ....http://www.atinucleus.com

Agilent Technologies.. http://www.agilent.com

Algorithmics Ltd. .... http://www.algor.co.uk

Apogee Software, Inc..http://www.apogee.com

Applied Microsystems Corporation .... http://www.amc.com

Baton Rouge International, Inc. ....http://www.bri.com/embed.htm

Cogent Computer Systems, Inc. .... http://www.cogcomp.com

Corelis, Inc. ....http://www.corelis.com

Crescent Heart Software ....http://www.c-h-s.com

Cygnus Solutions..http://www.cygnus.com

DENSAN Systems, Inc. .... http://www.densan.com

digital logic instruments gmbh .... http://www.dli-usa.com

Embedded Performance, Inc. ....http://www.episupport.com

Express Logic, Inc. .... http://www.expresslogic.com

Galileo Technology, Inc. ....http://www.galileoT.com

Green Hills Software, Inc. ....http://www.ghs.com

Insignia Solutions...http://www.insignia.com

JMI Software Systems, Inc. .... http://www.jmi.com

Microsoft Corporation ....http://www.microsoft.com/windowsce/embedded

NEC Electronics Inc. .... http://www.necel.com

Papillon Research Corporation...http://www.papillonres.com/~papillon

Peerless Systems Corporation .... http://www.peerless.com

Probitas Corporation.. http://www.probitas.com

QNX Software Systems Ltd. .... http://www.qnx.com

Simpod, Inc.. http://www.simpod.com

Synopsys, Inc. ....http://www.synopsys.com

Tektronix, Inc. .... http://www.tek.com/measurement/logic_analyzers

UniSoft Corporation .... http://www.unisoft.com

U S Software..http://www.ussw.com

V3 Semiconductor Corporation.. http://www.vcubed.com

Viosoft Corporation...http://www.viosoft.com

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