

RSB-4210 Product Change Notification

SBC with Freescale i.MX53 Series Processor

a. Affected Models for the Changes:

To distinguish new revision from the old, the finished good part number of RSB-4210 will be changed with new product models accordingly. Below is the comparison table of new rev. and old rev. finished good part number:

| Original P/N | New P/N |
|-------------------|-------------------|
| RSB-4210CB-A60AAE | RSB-4210CB-A60BAE |
| RSB-4210CV-A78AAE | RSB-4210CV-A78BAE |
| RSB-4210CH-A78AAE | RSB-4210CH-A78BAE |
| RSB-4210CF-A78AAE | RSB-4210CF-A78BAE |
| RSB-4210IF-A78AAE | RSB-4210IF-A78BAE |
| RSB-4210WF-A78AAE | RSB-4210WF-A78BAE |

b. Summary of Changes:

The table listed as below illustrates the main changes for the new revision of RSB-4210. (To detail introduction of the changes, please check Sec. (c) for further reference.

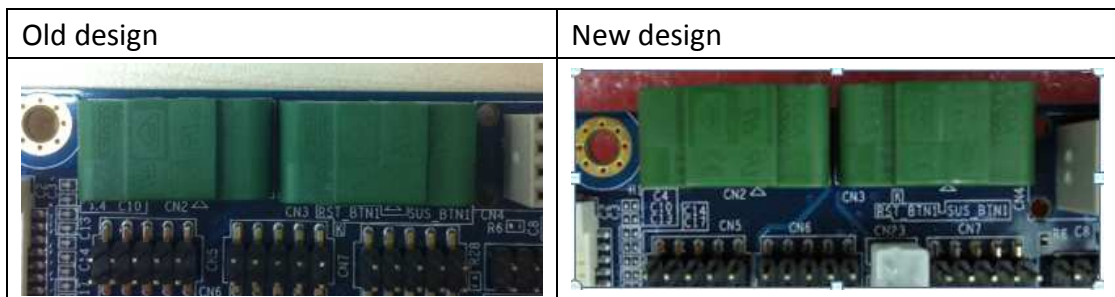
| Item | Topic | Description | Schematics, BOM or Layout change | Impact component | New component P/N |
|------|----------------------------------|--|----------------------------------|------------------|--------------------------|
| 1 | Shift Phoenix connector position | Shift out 3mm phoenix connector position.(CANbus and RS-485) | Layout | PCB | 19C2421002-01 |
| 2 | Power consumption solution | 1. Reduce power consumption under normal mode 2. Suspend mode added | Schematics, BOM,Layout | PCB | 19C2421002-01 |
| 3 | iNAND flash upgrade | Change iNAND solution from SanDisk 2GB to Kingston 4GB | BOM | iNAND flash | 1410022199 2080003734 |

| | | | | | |
|---|---|---|----------------------------|-----------------------------|-----------------------------------|
| 4 | Support backlight 5V & 12V panel | Add 0 ohm R | BOM | R | 105A700004 |
| 5 | Add Power LED pin header | Add SYS_3V3 Pin header | Layout Schematic BOM | Pin header | 1655302020 |
| 6 | Support AUO Panel G070VW01 V1, need to reserve the pull low R | Reserve the pull low R | Layout Schematic BOM | R | 105A700004 |
| 7 | HDMI/VGA output support bypass mode | 1.Removing R397/ R490 / U24 2.Removing R447 and Add R446 | BOM | R | 1000000432 (R446) |
| 8 | Advanced booting process | Conduct new loader to separate uboot from SPI NOR flash independently | BOM | SPI NOR flash (Boot loader) | 1420030672 (256MB/CB) |
| | | | | | 1420030671 (512MB/CV/CH/CF/IF/WF) |

c. Descriptions of Changes:

1. Shift Phoenix connector position :

To avoid cable connected against with the chassis, we shift out phoenix connector 3mm.



2. Power consumption solution:

With layout modification, the power consumption of RSB-4210 new revision has been reduced significantly under suspend mode. The table shows the detail power consumption of RSB-4210 as below:

| Old design | | New design | |
|-------------|-----------|-------------|-----------|
| Current(mA) | Power(mW) | Current(mA) | Power(mW) |

| | | | |
|----|-----|------|-----|
| 51 | 969 | 12.3 | 240 |
|----|-----|------|-----|

※OS is under WEC7 as reference.

3. iNAND flash upgrade:

iNAND flash solution has been upgraded from 2GB to 4GB.

4. Support backlight 5V & 12V panel :

In order to support most panel backlight power, schematic needs to be add a 0 ohm Resistor.

5. Add Power LED pin header :

For system assembly, we have reserved a pin header for power LED cable connected.

6. Support AUO Panel G070VW01 V1, need to reserve the pull low R :

We used AUO 7" Panel G070VW01 V0 in RSB-4210 evaluation kit for customer evaluating.

G070VW01 V1 panel is the next version and the spec was different from old one on Pin3, Pin4 and Pin17. Old panel defined these pins "pull high" but the new one needs to be "pull low".

| V1 | | | V0 | | |
|---------|----------|---|---------|----------|---|
| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
| 1 | VDD | Power Supply, 3.3V (typical) | 1 | VDD | Power Supply, 3.3V (typical) |
| 2 | VDD | Power Supply, 3.3V (typical) | 2 | VDD | Power Supply, 3.3V (typical) |
| 3 | UD | Vertical Reverse Scan Control, When UD=Low or NC → Normal Mode. When UD=High → Vertical Reverse Scan. <small>Note</small> | 3 | UD | Vertical Reverse Scan Control, When UD=High or NC → Normal Mode. When UD=Low → Vertical Reverse Scan. <small>Note</small> |
| 4 | LR | Horizontal Reverse Scan Control, When LR=Low or NC → Normal Mode. When LR=High → Horizontal Reverse Scan. <small>Note</small> | 4 | LR | Horizontal Reverse Scan Control, When LR=High or NC → Normal Mode. When LR=Low → Horizontal Reverse Scan. <small>Note</small> |
| 5 | RdIN1- | LVDS differential data input Pair 0 | 5 | RdIN1- | LVDS differential data input Pair 0 |
| 6 | RdIN1+ | | 6 | RdIN1+ | |
| 7 | GND | Ground | 7 | GND | Ground |
| 8 | RdIN2- | LVDS differential data input Pair 1 | 8 | RdIN2- | LVDS differential data input Pair 1 |
| 9 | RdIN2+ | | 9 | RdIN2+ | |
| 10 | GND | Ground | 10 | GND | Ground |
| 11 | RdIN3- | LVDS differential data input Pair 2 | 11 | RdIN3- | LVDS differential data input Pair 2 |
| 12 | RdIN3+ | | 12 | RdIN3+ | |
| 13 | GND | Ground | 13 | GND | Ground |
| 14 | RxCLKIN- | LVDS differential Clock input Pair | 14 | RxCLKIN- | LVDS differential Clock input Pair |
| 15 | RxCLKIN+ | | 15 | RxCLKIN+ | |
| 16 | GND | Ground | 16 | GND | Ground |
| 17 | SEL 6/8 | LVDS 6/8 bit select function control, High or NC → 6 Bit Input Mode. Low → 8 Bit Input Mode. <small>Note</small> | 17 | SEL 6/8 | LVDS 6/8 bit select function control, Low or NC → 6 Bit Input Mode. High → 8 Bit Input Mode. <small>Note</small> |
| 18 | NC | NC | 18 | NC | NC |
| 19 | RdIN4- | LVDS differential data input Pair 3. | 19 | RdIN4- | LVDS differential data input Pair 3. Must be tied to Ground in 6 bit input mode. |
| 20 | RdIN4+ | | 20 | RdIN4+ | |

! : "Low" stands for 0V. "High" stands for 3.3V. "NC" stands for "No Connected."

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7. HDMI/VGA output support bypass mode :

Bypass mode is an output alternative that the output resolution will be determined by default timing settings of your panel. Hardware need to be removed I2C buffer related signals.

8. Advanced booting process:

In the new revision, an advanced loader will be conducted and the u-boot could be separated from SPI NOR flash. As depicted in the figure as below, the booting process will be begin from (b1), which means a new loader will be executed firstly and u-boot could be placed to SATA HDD, onboard flash or SD card rather than SPI NOR flash. After executing the loader, the system will load the kernel automatically to complete the booting process as shown in (b2). Therefore, users could customize their u-boot independently based on this new booting architecture, which will also help them manage the u-boot and related follow-up maintenances.

(The new booting sequence will be listed as follows: New loader →SD→SATA→Onboard flash.)

